**Gabriel Jared**

**Vinícius Viana**

Sistema Somador e Subtrator de 12bits

**Descrição:**

Mux2x12:

Mux 2x12 , ou seja, 12 mux 2x1;

Entradas: Soma = {A0...A11}, Sub = {B0...B11};

Saída : Resultado = {Z0...Z11};

Seletor de operação.

Somador / Subtrator:

Somador de 1bit repetido 12 vezes.

Componente para realizar inversão de bit MSB em caso de subtração;

Componente para sinalizar Overflow;

Entradas: X , Y ,Cin;

Saída : Z, Cout.

**Tabela verdade:**

Mux 2x12:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Sit | Soma | Sub | Sel | Saida |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 0 | 1 | 1 | 1 |
| 4 | 1 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 | 0 |
| 6 | 1 | 1 | 0 | 1 |
| 7 | 1 | 1 | 1 | 1 |

Somador/Subtrator:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Sit | A | B | Cin | Cout | Z |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 2 | 0 | 1 | 0 | 0 | 1 |
| 3 | 0 | 1 | 1 | 1 | 0 |
| 4 | 1 | 0 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 | 1 | 0 |
| 6 | 1 | 1 | 0 | 1 | 0 |
| 7 | 1 | 1 | 1 | 1 | 1 |

**DVK**:

Mux12x2:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | ~Sub | | Sub | |
| ~Soma | 0 | 0 | 1 | 0 |
| Soma | 1 | 0 | 1 | 1 |
|  | ~Sel | Sel | | ~Sel |

Saida = Soma and Sel

Saida = Sub and not(Sel)

Somador/Subtrator:

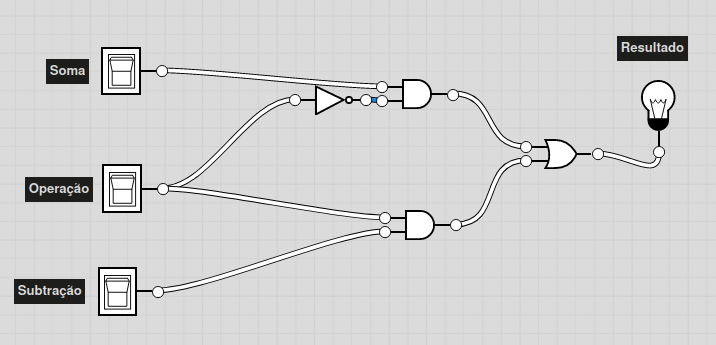
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | ~B | | B | |
| ~A | 0 | 1 | 0 | 1 |
| A | 1 | 0 | 1 | 0 |
|  | ~Cin | Cin | | ~Cin |

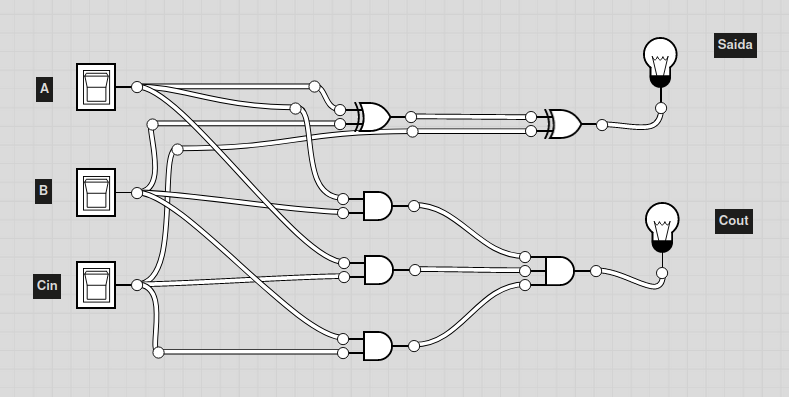
Saída = (A xor B) xor Cin

Cout = (A and B) or (A and Cin) or (B and Cin)

**Circuitos:**

Mux2x1:



Somador/Subtrator 2x1:

Inversor de bit:

