Consecutive Summation of Counter Output

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Abstract - This is a circuit to perform consecutive summation of the output of the counter to the current value of the summation output. This circuit performs the summation as given by equation $\sum_{a=0}^{n} a$, where the value of a can be in any sequence as designed by the user.
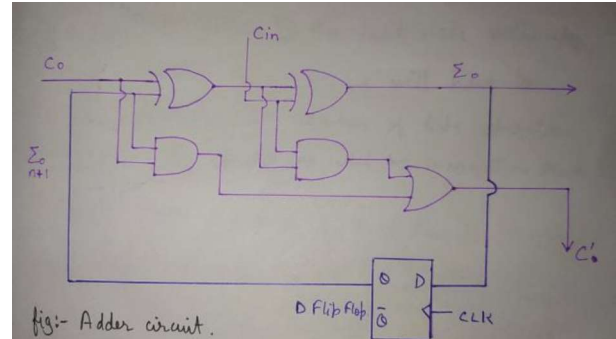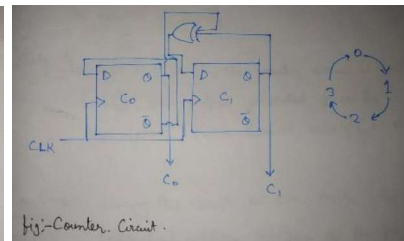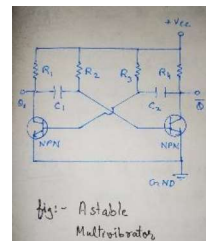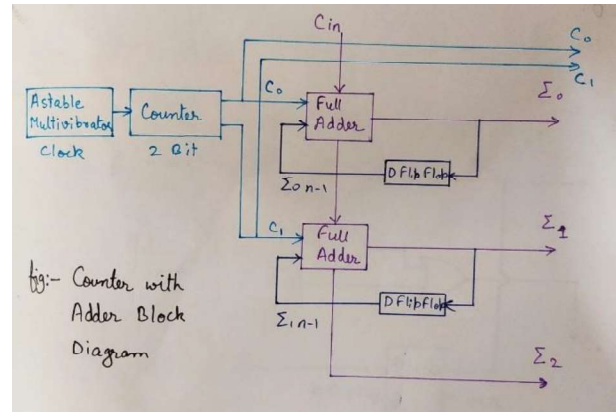
CIRCUIT DETAILS

Astable multivibrator is used to generate the clock pulse. The clock pulse is fed to 2-bit D counter. The output of the counter is fed to one of the inputs of parallel adder circuit. The second input of parallel adder is the previous value of the adder block, which was stored in a D flip-flop.

- Stage 1 - Clock pulse is given to the counter, and it starts this stage with binary $[c_0 = 0, c_1 = 0]$. In this stage the summation block is at zero position, which results in output as $[\sum 0 = 0, \sum 1 = 0, \sum 2 = 0]$.
- Stage 2 - Now the counter value becomes binary [0 1]. The previous state of the summation block gets added to the counter output. Hence the output becomes binary [0 0 1].
- Stage 3 - In the next stage counter value becomes binary [1 0]. The summation block performs its operation to give output as binary [0 1 1].
- Stage 4 - For this stage, the output of the counter is binary [1 1]. The output generated from the submission block becomes binary [1 1 0].

Conclusion - Using this circuit, we can design the sequential addition of the previous state values to the next state value. For doing so, we will have to increase the number of bits operation in the counter block as well as summation block.

Reference - Book on Digital Electronics by Morris Mano

fig:- Counter with Adder Block Diagram

fig:- Astable Multivibrator

fig:- Counter Circuit.

fig:- Adder circuit.

Stage	C_0	C_1	Σ_0	Σ_1	Σ_2
I	0	0	0	0	0
II	0	1	0	0	1
III	1	0	0	1	1
IV	1	1	1	1	0

fig:- Output