

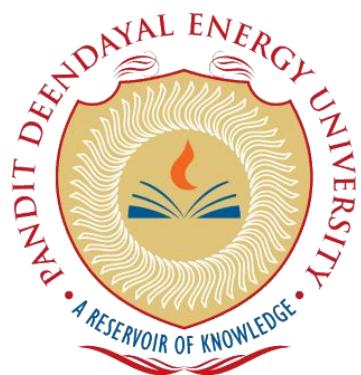
Project Report

for

RTL to GDSII Workshop

Conducted at

Pandit Deendayal Energy University, Gandhinagar



Bachelor of Technology
in
Information and Communication Technology

Submitted by -

Vinit Kumar Gupta (23BIT089)

Submitted to -

Puneet Mittal Sir

Department of Information and Communication Technology
School of Technology

Aim:

To design an 8-bit magnitude comparator using Verilog HDL and Generate GDS-II layout of the design using Synopsys flowscripts.

Initial Setup:

Don't use cells: **FADD, HADD, AO**

Compile method: **Compile Ultra**

run_dc.tcl file:

```
source -echo -verbose ./rm_setup/dc_setup.tcl
set RTL_SOURCE_FILES ../../rtl/comparator_8bit_rtl.v

define_design_lib WORK -path ./WORK
set_dont_use [get_lib_cells */FADD*]
set_dont_use [get_lib_cells */HADD*]
set_dont_use [get_lib_cells */AO*]
#set_dont_use [get_lib_cells */OA*]
#set_dont_use [get_lib_cells */NAND*]
#set_dont_use [get_lib_cells */XOR*]
#set_dont_use [get_lib_cells */NOR*]
#set_dont_use [get_lib_cells */XNOR*]
#set_dont_use [get_lib_cells */MUX*]

analyze -format verilog ${RTL_SOURCE_FILES}
elaborate ${DESIGN_NAME}
current_design

read_sdc ../../CONSTRAINTS/comparator_8bit.sdc

#compile
compile_ultra
report_timing > ./reports/timing.rpt
write -format verilog -hierarchy -output ${RESULTS_DIR}/${DCRM_FINAL_VERILOG_OUTPUT_FILE}
```



Constraints:

comparator_8bit.sdc file:

```
create_clock -period 3 [get_ports clk]

set_input_delay -max 0.5 -clock clk [all_inputs]
set_input_transition 0.5 [all_inputs]

set_output_delay -max 0.5 -clock clk [all_outputs]

set_clock_uncertainty -setup 0.300 [get_clocks clk]
set_clock_uncertainty -hold 0.100 [get_clocks clk]
set_max_transition 0.250 [current_design]
set_max_transition -clock_path 0.150 [get_clocks clk]
```

Library used: **saed32rvt_tt0p78vn40c.db**

common_setup.tcl file:

```
puts "RM-Info: Running script [info script]\n"
#####
# Variables common to all reference methodology scripts
# Script: common_setup.tcl
# Version: N-2017.09-SP4 (April 23, 2018)
# Copyright (C) 2007-2017 Synopsys, Inc. All rights reserved.
#####

set DESIGN_NAME          "comparator_8bit" ;# The name of the top-level design
set PDK_PATH              "./ref/" ;# to set the PDK path for the design
set DESIGN_REF_DATA_PATH  "" ;# Absolute path prefix variable for library/design data.
                                # Use this variable to prefix the common absolute path
                                # to the common variables defined below.
                                # Absolute paths are mandatory for hierarchical
                                # reference methodology flow.

#####
# Hierarchical Flow Design Variables
#####

set HIERARCHICAL_DESIGNS    "" ;# List of hierarchical block design names "DesignA DesignB" ...
set HIERARCHICAL_CELLS      "" ;# List of hierarchical block cell instance names "u_DesignA u_DesignB" ...

#####
# Library Setup Variables
#####

# For the following variables, use a blank space to separate multiple entries.
# Example: set TARGET_LIBRARY_FILES "lib1.db lib2.db lib3.db"

set ADDITIONAL_SEARCH_PATH   "$PDK_PATH $PDK_PATH/tech/milkyway $PDK_PATH/tech/star_rcxt" ;# Additional search path to be added to the default search path
set TARGET_LIBRARY_FILES      "$PDK_PATH/lib/stdcell.rvt/saed32rvt_tt0p78vn40c.db" ;# Target technology logical libraries
set ADDITIONAL_LINK_LIB_FILES "" ;# Extra link logical libraries not included in TARGET_LIBRARY_FILES
```

Part	Meaning
saed32rvt	SAED (Synopsys Academic Enablement Design) 32nm Regular-Vt (threshold voltage) standard cell library
tt	Typical-Typical process corner (both NMOS and PMOS at <i>typical</i> speed)
0p78v	Supply voltage = 0.78V
n40c	Temperature = 40°C , "n" for nominal

This library is used by **Design Compiler** during:

- ✓ Synthesis
- ✓ Static Timing Analysis (STA)
- ✓ Power estimation
- ✓ Generating gate-level netlist

> **NOTE:** For this project, we chose the clock period to be **3ns** to meet the slack requirements (**+ve and < 1**) and the **DESIGN_NAME** = “**comparator_8bit**”.

1. RTL Simulation and Debug using VCS and Verdi

Objective:

Simulate and functionally verify the Verilog RTL description of the 8-bit magnitude comparator using Synopsys VCS, followed by waveform analysis and debugging using Verdi.

Workflow Steps:

- The process begins with writing the Register Transfer Level (RTL) description of the desired functionality using Verilog HDL. In this case, the design implements an 8-bit magnitude comparator.
- The module is parameterized with two 8-bit input ports A and B, a clock input (clk), and three output registers:
 - a_gt_b — asserted high ('1') when $A > B$
 - a_lt_b — asserted high ('1') when $A < B$
 - a_eq_b — asserted high ('1') when $A == B$
- The design is synchronous and driven by a positive-edge triggered clock. Logic for comparison is evaluated on each rising edge of the clock.
- A corresponding testbench is written in Verilog to provide stimulus to the comparator module and observe output behaviour under various test scenarios.
- The simulation is executed using Synopsys VCS to ensure functional correctness.
- The output waveforms and signal transitions are examined using Verdi to visually verify logic correctness and debug any potential issues.

RTL code (**comparator_8bit_rtl.v**):

```
module comparator_8bit (
    input clk,
    input [7:0] a,
    input [7:0] b,
    output reg a_gt_b,
    output reg a_lt_b,
    output reg a_eq_b
);

reg [7:0] a_reg, b_reg;

always @(posedge clk) begin
    a_reg <= a;
    b_reg <= b;

    if (a > b) begin
        a_gt_b <= 1;
        a_lt_b <= 0;
        a_eq_b <= 0;
    end else if (a < b) begin
        a_gt_b <= 0;
        a_lt_b <= 1;
        a_eq_b <= 0;
    end else begin
        a_gt_b <= 0;
        a_lt_b <= 0;
        a_eq_b <= 1;
    end
end

endmodule
```

Testbench code (**comparator_8bit_tb.v**):

```
'timescale 1ns/1ns
`include "comparator_8bit_rtl.v" // includes the module definition for the full adder
module testbench;
    reg clk;
    reg [7:0] a, b;
    wire a_gt_b, a_lt_b, a_eq_b;

    comparator_8bit dut (
        .clk(clk),
        .a(a),
        .b(b),
        .a_gt_b(a_gt_b),
        .a_lt_b(a_lt_b),
        .a_eq_b(a_eq_b)
    );

    // Clock generation
    always #5 clk = ~clk;

initial begin
    $fsdbDumpvars();
    //Tool specific command. Creates novas.fsdb file. Used for waveform generation

    $display("Starting Testbench for 8-bit Comparator");
    a <= 0; b <= 0; clk <= 0;
    // Reset inputs

    // Test 1: a > b
    #20; a = 8'd150; b = 8'd100;
    $display("a=150, b=100 => gt=%b lt=%b eq=%b", a_gt_b, a_lt_b, a_eq_b);

    // Test 2: a < b
    #20; a = 8'd60; b = 8'd180;
    $display("a=60, b=180 => gt=%b lt=%b eq=%b", a_gt_b, a_lt_b, a_eq_b);

    // Test 3: a == b
    #20; a = 8'd200; b = 8'd200;
    $display("a=200, b=200 => gt=%b lt=%b eq=%b", a_gt_b, a_lt_b, a_eq_b);

    #100 $finish;
end

endmodule
```

Next, run these bash commands one by one:

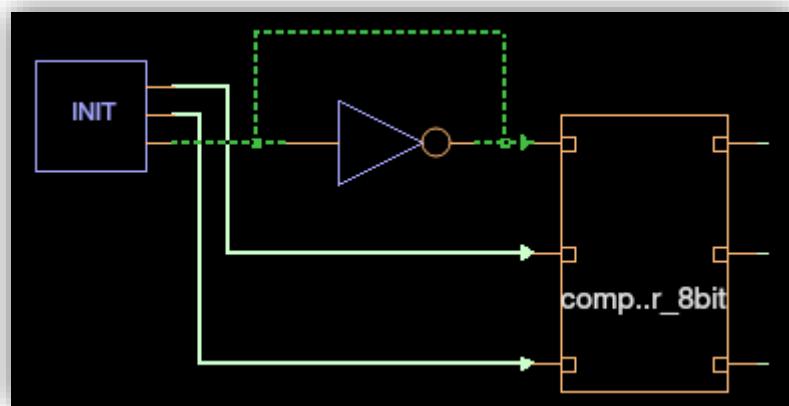
```
vcs -full64 comparator_8bit_rtl.v -debug_access+all -lca -kdb  
vcs -full64 comparator_8bit_tb.v -debug_access+all -lca -kdb  
./simv Verdi  
verdi -ssf novas.fsdb -nologo
```

What This Actually Does:

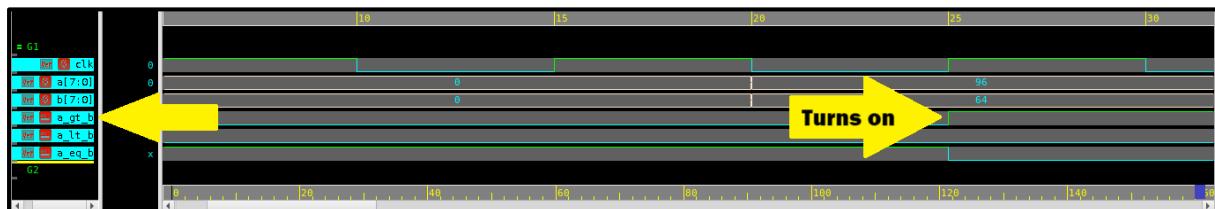
Step	Tool	Outcome
vcs compile (first two)	VCS	Compiles the RTL + TB into simulation binary
./simv	VCS	Ran the simulation, produced novas.fsdb waveform
verdi -ssf novas.fsdb	Verdi	Opens GUI to view waveform and verify functionality

Results:

Simulated the RTL (behavioral-level).



Verified that inputs and outputs work as expected on the waveform in Verdi.



2. Logic Synthesis with Design Compiler (dc_shell)

This is where we:

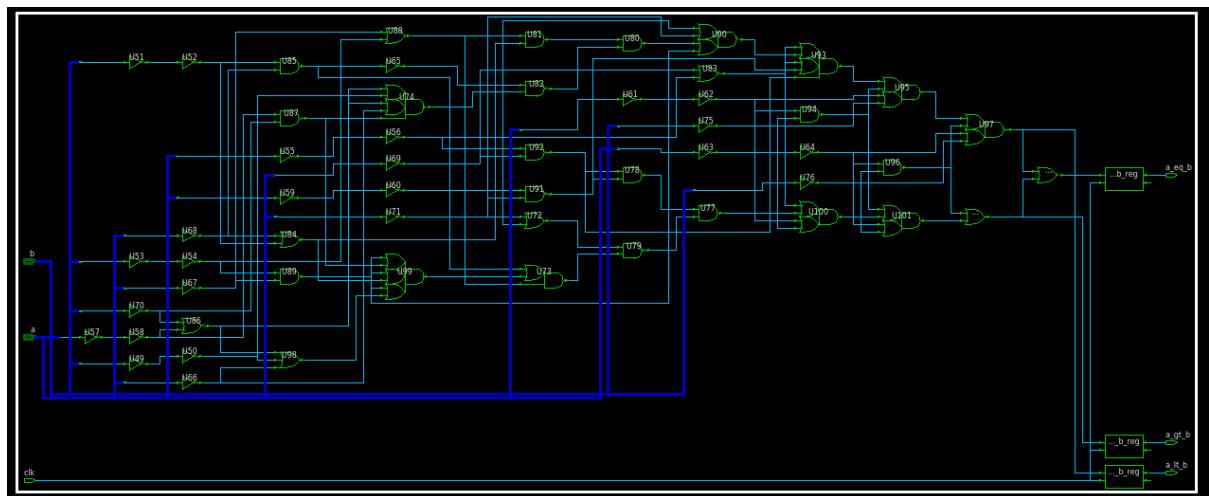
- Convert RTL → Gate-Level Netlist
- Use your .v file + .db + clock constraints in .sdc
- Output: .mapped.v, .rpt, etc.

➤ Steps:

- Cd to RTL2GDSII/DC/ in terminal
- Enter the command `dc_shell` to enter into Design compiler shell.
- Type: `start_gui` to open the GUI for Design Compiler.
- Type `source run_dc.tcl` to run the TCL script to get the design and results. (Uncommented “don’t use cells” have been shown earlier in the run_dc.tcl file image)

Output:

(Gate-Level Netlist in Design Compiler)



To verify the synthesized gate-level netlist:

1. Update your DC script to use the SDC

```
> read_sdc comparator_8bit.sdc
```

2. Then, enter the following two commands:

```
> report_qor
```

```
>report_timing
```

```
Cell Count
-----
Hierarchical Cell Count:      0
Hierarchical Port Count:      0
Leaf Cell Count:              58
Buf/Inv Cell Count:           25
Buf Cell Count:               0
Inv Cell Count:               25
CT Buf/Inv Cell Count:        0
Combinational Cell Count:     55
Sequential Cell Count:        3
Macro Count:                  0
-----

Area
-----
Combinational Area:          100.132737
Noncombinational Area:        19.823233
Buf/Inv Area:                 31.768000
Total Buffer Area:            0.00
Total Inverter Area:          31.77
Macro/Black Box Area:         0.000000
Net Area:                     10.472996
-----

Cell Area:                   119.955970
Design Area:                  130.428966

Design Rules
-----
Total Number of Nets:          75
Nets With Violations:         16
Max Trans Violations:          16
Max Cap Violations:            0
-----
```

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
input external delay	0.50	0.50 f
a[1] (in)	0.00	0.50 f
U57/Y (INVX0 RVT)	0.21	0.71 r
U58/Y (INVX0 RVT)	0.09	0.79 f
U86/Y (NOR2X0 RVT)	0.16	0.95 r
U74/Y (OAI221X1 RVT)	0.17	1.12 f
U82/Y (NAND2X0 RVT)	0.07	1.19 r
U80/Y (AND2X1 RVT)	0.09	1.28 r
U90/Y (OAI221X1 RVT)	0.11	1.39 f
U93/Y (OA221X1 RVT)	0.15	1.55 f
U95/Y (OA22X1 RVT)	0.15	1.70 f
U97/Y (OAI22X1 RVT)	0.18	1.88 r
U103/Y (NOR2X0 RVT)	0.11	1.99 f
a_eq_b_reg/D (DFFX1 RVT)	0.01	2.00 f
data arrival time		2.00
clock clk (rise edge)	3.00	3.00
clock network delay (ideal)	0.00	3.00
clock uncertainty	-0.30	2.70
a_eq_b_reg/CLK (DFFX1 RVT)	0.00	2.70 r
library setup time	-0.08	2.62
data required time		2.62
data required time		2.62
data arrival time		-2.00
slack (MET)		0.61

report_qor: Stands for “Quality of Results” report. This is a high-level summary report that gives the key metrics of our synthesized design, as shown in first image. It is used to get a quick overview of how good synthesis results are in terms of timing, area, and cell usage. It’s often the first report to check after a successful synthesis.

report_timing: This gives the critical path details, showing timing delays and slack for the most critical paths in the design. This is the primary report to debug timing violations or confirm that your design meets timing after applying constraints via the .sdc file.

report_units: Shows the units used in environment for reporting timing, power, capacitance, etc. The purpose is to ensure that we're interpreting timing and power numbers in the correct unit. Especially helpful when correlating results between tools like DC, PT (PrimeTime), or ICC-II.

>report_units

```
dc_shell> report_units
*****
Report : units
Design : comparator_8bit
Version: W-2024.09
Date   : Mon Jun  2 17:09:36 2025
*****
Units
-----
Time_unit      : 1.0e-09 Second(ns)
Capacitive_load_unit : 1.0e-15 Farad(fF)
Resistance_unit : 1.0e+06 Ohm(MOhm)
Voltage_unit   : 1 Volt
Power_unit     : N/A
Current_unit   : 1.0e-06 Amp(uA)
```

The timing report generates inside the path:
RTL2GDSII/DC/reports

in a file called: **timing.rpt**

The content of this file is same as that we get when entering the command: **report_timing**.

What is **WORK** directory in DC?

The line inside run_dc.tcl file (refer on page 2 or in original file):

```
define_design_lib WORK -path ./WORK means:
```

- **WORK** is just a **logical name** for the design library.
- -path ./WORK tells DC to map this logical library (WORK) to a physical directory named WORK.

3. Physical Design Phase using IC Compiler

Gate-Level Netlist (Post-Synthesis)



Import to ICC-II (icc2_shell)



Floor Planning



Power Planning



Placement



Clock Tree Synthesis



Routing



PrimeTime STA (pt_shell)

>For physical design, cd to: RTL2GDSII/ICCII in terminal and type: `icc2_shell` to enter into IC compiler. Then: `start_gui` and finally source the **TCL scripts** one-by-one from the shell as:

>`source scripts/<file_name>.tcl`

1. Floor Planning:

floorplan.tcl file code:

```
set PDK_PATH ../../ref
create_lib -ref_lib $PDK_PATH/lib/ndm/saed32rvt_c.ndm COMP_8BIT_LIB
read_verilog {../../DC/results/comparator_8bit.mapped.v} -library COMP_8BIT_LIB -design comparator_8bit -top comparator_8bit
# open the lib and block after saving
# open_lib COMP_8BIT_LIB
# open_block COMP_8BIT

# FloorPlan settings
# Scenario 5:
initialize_floorplan -shape L -control_type die -side_length {20 30 20 20} -core_offset {8}
set_individual_pin_constraints -ports [get_ports clk] -exclude_sides {1 2 3 4 5}
place_pins -self
create_placement -floorplan -effort low

#####
save_block -as COMP_8BIT
save_lib
#####
```

*Here, we have used the **Scenario 5** for all the workflows from Floor Planning to Routing.*

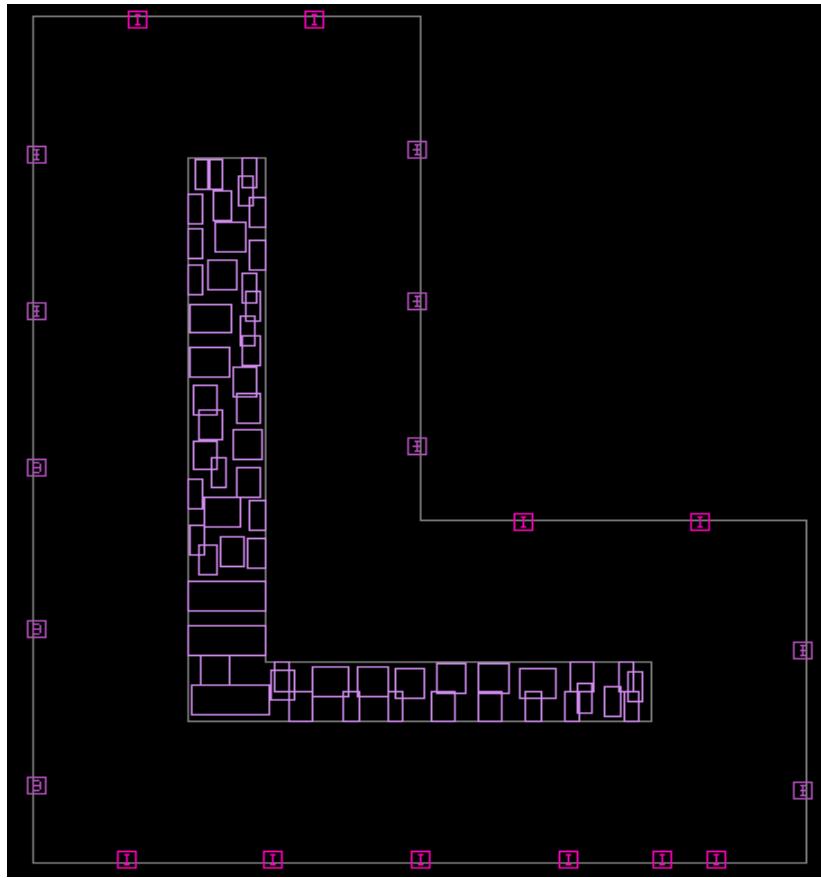
Floorplanning Parameters and Their Meanings

- To check specific parameter in manual

man (parameter)

Parameter	Meaning
-shape	Defines the geometric layout of the core (e.g., Rectangular, L, T, U).
-core_utilization	Sets the percentage of the core area to be filled with logic cells.
-core_offset	Distance between core boundary and die edge , in microns.
-coincident_boundary	If true , aligns core and die edges to be coincident.
-control_type	Determines whether control is based on the die or the core dimensions.
-orientation	Orientation of the core (e.g., N, S, E, W = North, South, East, West).
-side_length	Custom lengths of each side for non-rectangular shapes.
-flip_first_row	Flips the first row of standard cells , useful for alternating power rails.
-location {x y}	Specific (x, y) placement location for a pin or port.
-sides	Specifies on which sides of the die/core pins are allowed.
-pin_spacing_distance	Minimum spacing between pins , useful for routing clarity.
-offset	Distance from a side to place pins, in microns.
-exclude_sides	Sides on which pins should not be placed .
create_placement_blockage	Defines area where no standard cells can be placed (blockage).
-type hard	Indicates the blockage is non-negotiable (cannot be overridden).
-effort	Determines the placement optimization effort (e.g., low, medium, high).

```
>source scripts/floorplan.tcl
```



```
>report_units
```

```
icc2_shell> report_units
*****
Report : user_units
Design : comparator_8bit
Version: W-2024.09
Date   : Mon Jun  2 17:26:24 2025
*****
```

Input Units (set by technology library)	
time	: 1.00ns
resistance	: 1.00MΩ
capacitance	: 1.00fF
voltage	: 1.00V
current	: 1.00uA
power	: 1.00pW
length	: 1.00um
energy	: 1.00pj/t
Output Units (set by technology library)	
time	: 1.00ns
resistance	: 1.00MΩ
capacitance	: 1.00fF
voltage	: 1.00V
current	: 1.00uA
power	: 1.00pW
length	: 1.00um
energy	: 1.00pj/t

```
>report_timing
```

```
Startpoint: b[1] (input port clocked by clk)
Endpoint: a_eq_b_reg (rising edge-triggered flip-flop clocked by clk)
Mode: default
Corner: default
Scenario: default
Path Group: **in2reg_default**
Path Type: max
```

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
input external delay	0.50	0.50 f
b1[1] (in)	0.00	0.50 f
U70/Y (INVX0_RVT)	0.07	0.57 r
U86/Y (NOR2X0_RVT)	0.06	0.64 r
U74/Y (OA1221XL_RVT)	0.06	0.70 r
U82/Y (NAND2X0_RVT)	0.02	0.71 f
U80/Y (AND2X1_RVT)	0.03	0.75 f
U90/Y (OA122X1_RVT)	0.04	0.79 r
U93/Y (OA221X1_RVT)	0.04	0.83 r
U95/Y (OA22X1_RVT)	0.04	0.87 r
U97/Y (OA122X1_RVT)	0.05	0.92 f
U103/Y (NOR2X0_RVT)	0.04	0.96 r
a_eq_b_reg/D (DFFX1_RVT)	0.00	0.96 r
data arrival time		0.96

Point	Incr	Path
clock clk (rise edge)	3.00	3.00
clock network delay (ideal)	0.00	3.00
a_eq_b_reg/CLK (DFFX1_RVT)	0.00	3.00 r
clock uncertainty	-0.30	2.70
library setup time	-0.03	2.67
data required time		2.67

Point	Incr	Path
data required time		2.67
data arrival time		-0.96

slack (MET)		
slack (MET)		1.71

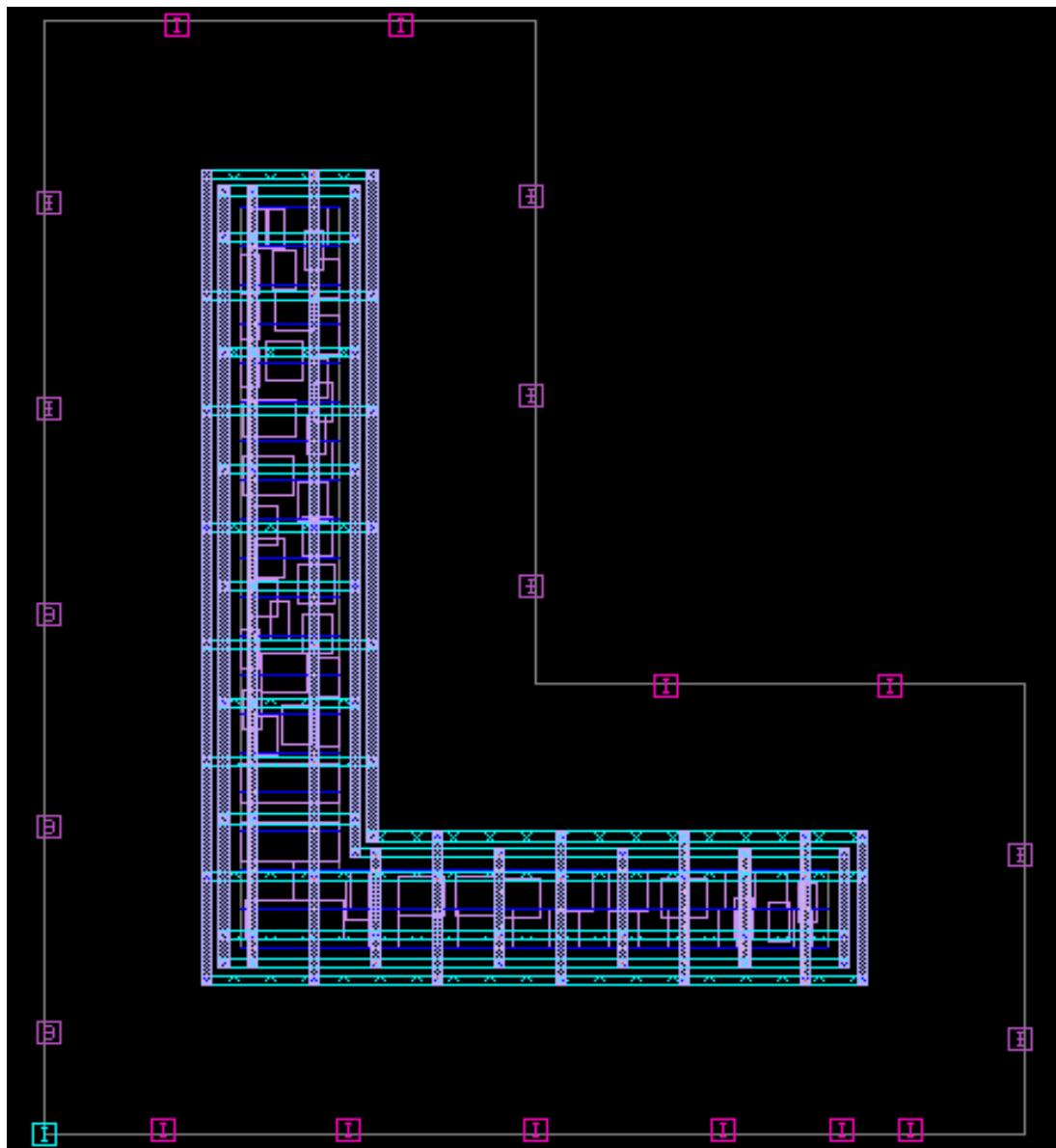
>report_qor

Cell Count	
Hierarchical Cell Count:	0
Hierarchical Port Count:	0
Leaf Cell Count:	58
Buf/Inv Cell Count:	25
Buf Cell Count:	0
Inv Cell Count:	25
Combinational Cell Count:	55
Single-bit Isolation Cell Count:	0
Multi-bit Isolation Cell Count:	0
Isolation Cell Banking Ratio:	0.00%
Single-bit Level Shifter Cell Count:	0
Multi-bit Level Shifter Cell Count:	0
Level Shifter Cell Banking Ratio:	0.00%
Single-bit ELS Cell Count:	0
Multi-bit ELS Cell Count:	0
ELS Cell Banking Ratio:	0.00%
Sequential Cell Count:	3
Integrated Clock-Gating Cell Count:	0
Sequential Macro Cell Count:	0
Single-bit Sequential Cell Count:	3
Multi-bit Sequential Cell Count:	0
Sequential Cell Banking Ratio:	0.00%
BitsPerflop:	1.00
Macro Count:	0
Area	
Combinational Area:	100.13
Noncombinational Area:	19.82
Buf/Inv Area:	31.77
Total Buffer Area:	0.00
Total Inverter Area:	31.77
Macro/Black Box Area:	0.00
Net Area:	0
Net XLength:	372.95
Net YLength:	419.24
Cell Area (netlist):	119.96
Cell Area (netlist and physical only):	119.96
Net Length:	792.19
Design Rules	
Total Number of Nets:	75
Nets with Violations:	16
Max Trans Violations:	16
Max Cap Violations:	0

2. Power Planning:

Power Planning is used to distribute power (VDD) and ground (VSS) across the chip. Power rings, stripes, and grids are created around and within the core to ensure stable and uniform power delivery to all standard cells and macros.

```
>source scripts/power_planning.tcl
```



>report_units

```
icc2_shell> report_units
*****
Report : user_units
Design : comparator_8bit
Version: W-2024.09
Date   : Mon Jun 2 17:32:31 2025
*****

Input Units (set by technology library)
-----
time          : 1.00ns
resistance    : 1.00MOhm
capacitance   : 1.00fF
voltage       : 1.00V
current       : 1.00uA
power         : 1.00pW
length        : 1.00um
energy        : 1.00pj/t

Output Units (set by technology library)
-----
time          : 1.00ns
resistance    : 1.00MOhm
capacitance   : 1.00fF
voltage       : 1.00V
current       : 1.00uA
power         : 1.00pW
length        : 1.00um
energy        : 1.00pj/t
```

>report_timing

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
input external delay	0.50	0.50 f
b[1] (in)	0.00	0.50 f
U70/Y (INVX0_RVT)	0.07	0.57 r
U86/Y (NOR2X0_RVT)	0.06	0.64 f
U74/Y (OAI221X1_RVT)	0.06	0.70 r
U82/Y (NAND2X0_RVT)	0.02	0.71 f
U80/Y (AND2X1_RVT)	0.03	0.75 f
U90/Y (OAI22X1_RVT)	0.04	0.79 r
U93/Y (OA221X1_RVT)	0.04	0.83 r
U95/Y (OA22X1_RVT)	0.04	0.87 r
U97/Y (OAI22X1_RVT)	0.05	0.92 f
U103/Y (NOR2X0_RVT)	0.04	0.96 r
a_eq_b_reg/D (DFFX1_RVT)	0.00	0.96 r
data arrival time		0.96
clock clk (rise edge)	3.00	3.00
clock network delay (ideal)	0.00	3.00
a_eq_b_reg/CLK (DFFX1_RVT)	0.00	3.00 r
clock uncertainty	-0.30	2.70
library setup time	-0.03	2.67
data required time		2.67
data required time		2.67
data arrival time		-0.96
slack (MET)		1.71

>report_qor

Cell Count	

Hierarchical Cell Count:	0
Hierarchical Port Count:	0
Leaf Cell Count:	58
Buf/Inv Cell Count:	25
Buf Cell Count:	0
Inv Cell Count:	25
Combinational Cell Count:	55
Single-bit Isolation Cell Count:	0
Multi-bit Isolation Cell Count:	0
Isolation Cell Banking Ratio:	0.00%
Single-bit Level Shifter Cell Count:	0
Multi-bit Level Shifter Cell Count:	0
Level Shifter Cell Banking Ratio:	0.00%
Single-bit ELS Cell Count:	0
Multi-bit ELS Cell Count:	0
ELS Cell Banking Ratio:	0.00%
Sequential Cell Count:	3
Integrated Clock-Gating Cell Count:	0
Sequential Macro Cell Count:	0
Single-bit Sequential Cell Count:	3
Multi-bit Sequential Cell Count:	0
Sequential Cell Banking Ratio:	0.00%
BitsPerflop:	1.00
Macro Count:	0

Area	

Combinational Area:	100.13
Noncombinational Area:	19.82
Buf/Inv Area:	31.77
Total Buffer Area:	0.00
Total Inverter Area:	31.77
Macro/Black Box Area:	0.00
Net Area:	0
Net XLength:	372.95
Net YLength:	419.24

Cell Area (netlist):	119.96
Cell Area (netlist and physical only):	119.96
Net Length:	792.19

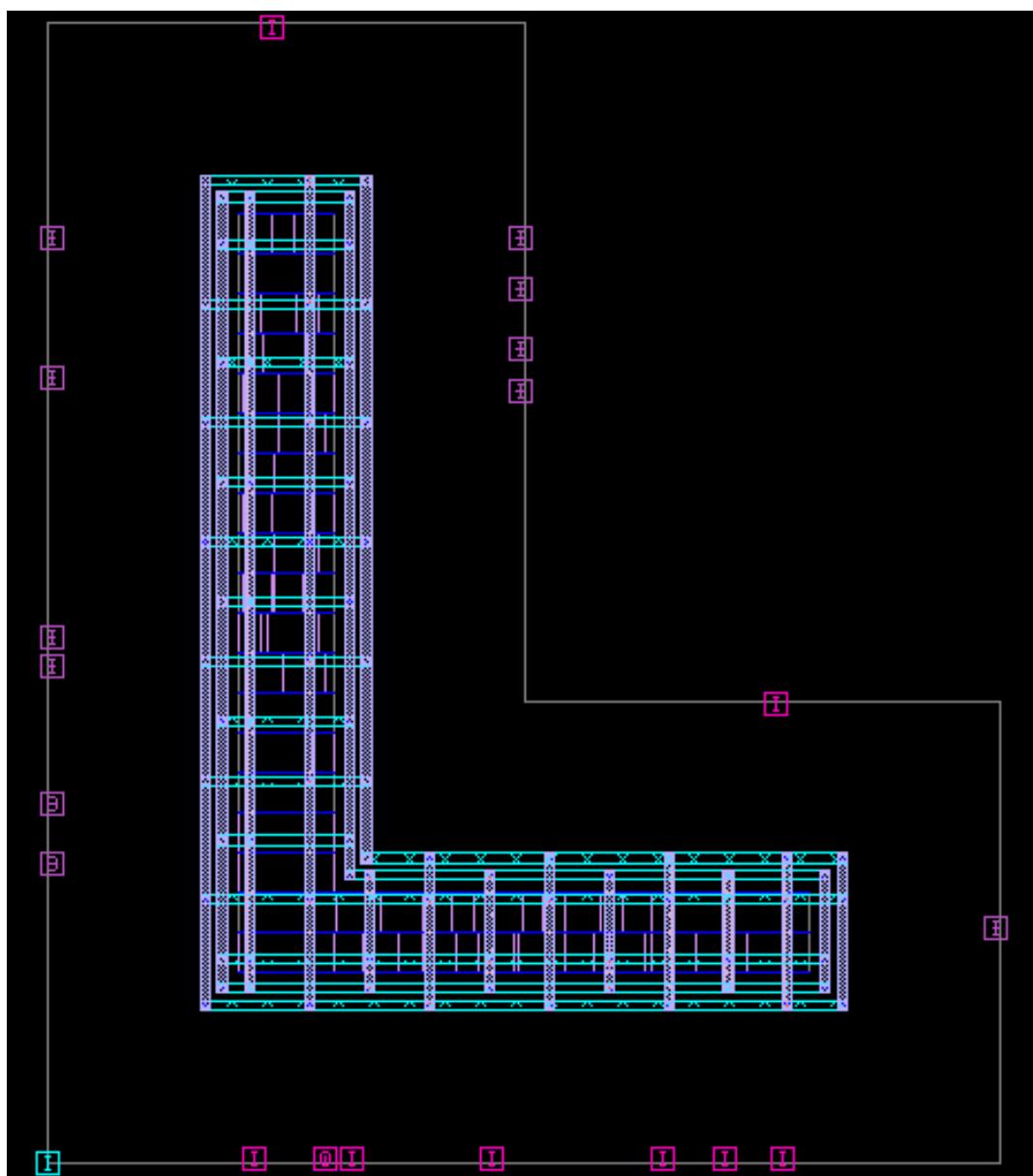
Design Rules	

Total Number of Nets:	77
Nets with Violations:	16
Max Trans Violations:	16
Max Cap Violations:	0

3. Placement:

Placement arranges the standard cells within the defined core area without overlap. It aims to minimize total wirelength and congestion while ensuring timing and design rules are met before clock tree insertion.

> *source scripts/placement.tcl*



> report_units

```
icc2_shell> report_units
*****
Report : user_units
Design : comparator_8bit
Version: W-2024.09
Date   : Mon Jun  2 17:36:54 2025
*****


Input Units (set by technology library)
-----
time          : 1.00ns
resistance    : 1.00MOhm
capacitance   : 1.00fF
voltage       : 1.00V
current       : 1.00uA
power         : 1.00pW
length        : 1.00um
energy        : 1.00pj/t


Output Units (set by technology library)
-----
time          : 1.00ns
resistance    : 1.00MOhm
capacitance   : 1.00fF
voltage       : 1.00V
current       : 1.00uA
power         : 1.00pW
length        : 1.00um
energy        : 1.00pj/t
```

>report_timing

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
input external delay	0.50	0.50 f
b[1] (in)	0.00	0.50 f
HFSINV_72_4/Y (INVX2_RVT)	0.06	0.56 r
U86/Y (NOR2X0_RVT)	0.07	0.62 f
ctmTdsLR_1_8/Y (OA221X1_RVT)	0.07	0.69 f
ctmTdsLR_1_10/Y (OA221X1_RVT)	0.07	0.76 f
U90/Y (OA122X1_RVT)	0.05	0.81 r
U93/Y (OA221X1_RVT)	0.05	0.86 r
U95/Y (OA22X1_RVT)	0.05	0.91 r
U97/Y (OA122X1_RVT)	0.06	0.97 f
U103/Y (NOR2X0_RVT)	0.05	1.01 r
a_eq_b_reg/D (DFFX1_RVT)	0.00	1.01 r
data arrival time		1.01

clock clk (rise edge)	3.00	3.00
clock network delay (ideal)	0.00	3.00
a_eq_b_reg/CLK (DFFX1_RVT)	0.00	3.00 r
clock uncertainty	-0.30	2.70
library setup time	-0.03	2.67
data required time		2.67

data required time		2.67
data arrival time		-1.01

slack (MET)		1.66

```
>report_qor
```

Cell Count	
Hierarchical Cell Count:	0
Hierarchical Port Count:	0
Leaf Cell Count:	36
Buf/Inv Cell Count:	8
Buf Cell Count:	0
Inv Cell Count:	8
Combinational Cell Count:	33
Single-bit Isolation Cell Count:	0
Multi-bit Isolation Cell Count:	0
Isolation Cell Banking Ratio:	0.00%
Single-bit Level Shifter Cell Count:	0
Multi-bit Level Shifter Cell Count:	0
Level Shifter Cell Banking Ratio:	0.00%
Single-bit ELS Cell Count:	0
Multi-bit ELS Cell Count:	0
ELS Cell Banking Ratio:	0.00%
Sequential Cell Count:	3
Integrated Clock-Gating Cell Count:	0
Sequential Macro Cell Count:	0
Single-bit Sequential Cell Count:	3
Multi-bit Sequential Cell Count:	0
Sequential Cell Banking Ratio:	0.00%
BitsPerflop:	1.00
Macro Count:	0

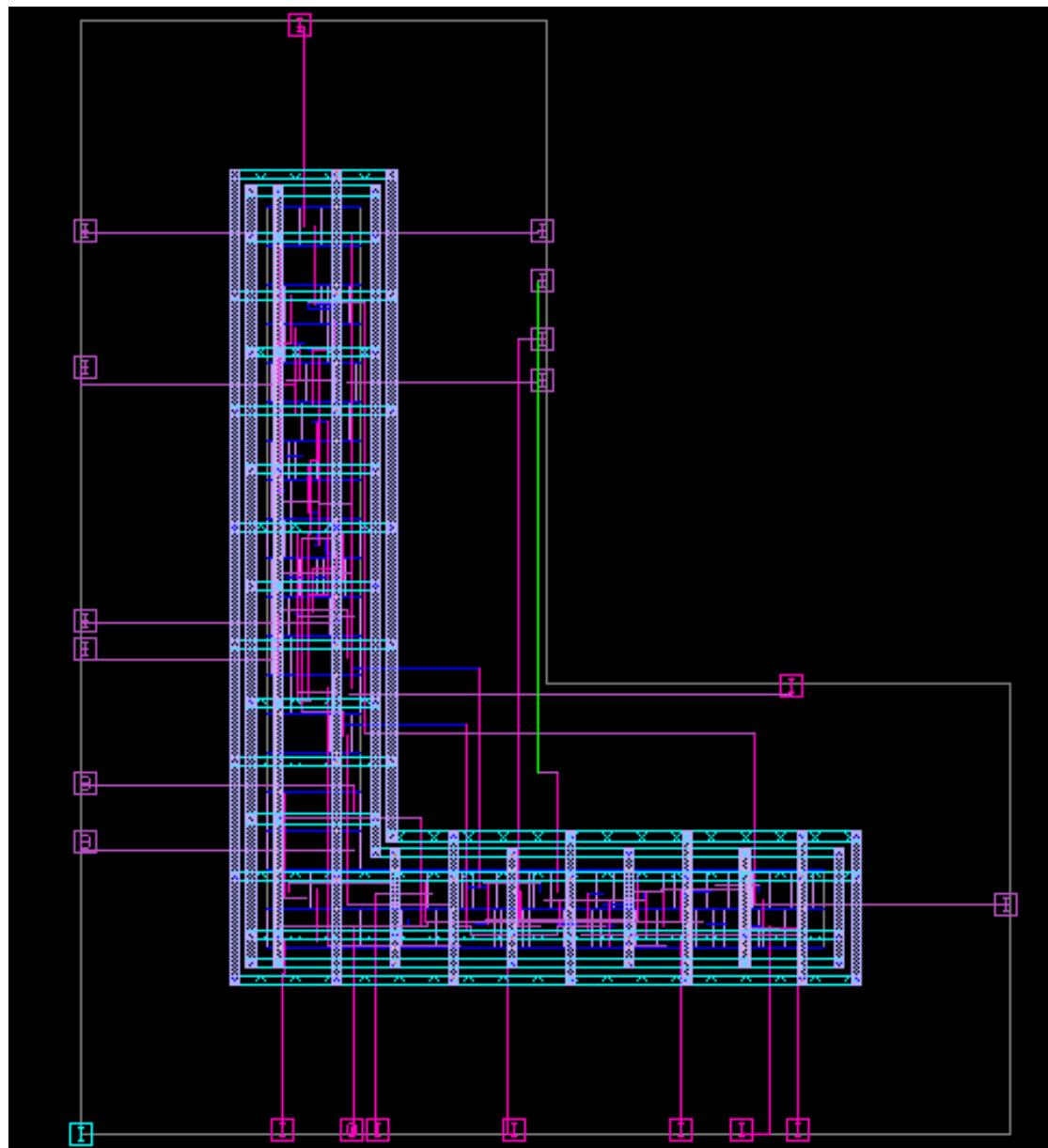
Area	
Combinational Area:	73.70
Noncombinational Area:	19.82
Buf/Inv Area:	12.71
Total Buffer Area:	0.00
Total Inverter Area:	12.71
Macro/Black Box Area:	0.00
Net Area:	0
Net XLength:	254.36
Net YLength:	330.41
Cell Area (netlist):	93.52
Cell Area (netlist and physical only):	93.53
Net Length:	584.77

Design Rules	
Total Number of Nets:	55
Nets with Violations:	16
Max Trans Violations:	16
Max Cap Violations:	0

4. Clock Tree Synthesis:

CTS creates a balanced clock distribution network from the clock source to all sequential elements. The goal is to minimize skew and insertion delay to ensure synchronized and reliable operation of flip-flops across the chip.

```
>source scripts/clock.tcl
```



>report_units

```
icc2_shell> report_units
*****
Report : user_units
Design : comparator_8bit
Version: W-2024.09
Date   : Mon Jun 2 17:39:52 2025
*****


Input Units (set by technology library)
-----
time          : 1.00ns
resistance    : 1.00MOhm
capacitance   : 1.00fF
voltage       : 1.00V
current       : 1.00uA
power         : 1.00pW
length        : 1.00um
energy        : 1.00pj/t


Output Units (set by technology library)
-----
time          : 1.00ns
resistance    : 1.00MOhm
capacitance   : 1.00fF
voltage       : 1.00V
current       : 1.00uA
power         : 1.00pW
length        : 1.00um
energy        : 1.00pj/t
```

>report_timing

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (propagated)	0.03	0.03
input external delay	0.50	0.53 f
b[3] (in)	0.00	0.53 f
ctmTdsLR_2_449/Y (NAND2X0_RVT)	0.12	0.64 r
ctmTdsLR_1_448/Y (INVX0_RVT)	0.04	0.68 f
U99/Y (0A222X1_RVT)	0.09	0.77 f
ctmTdsLR_4_457/Y (0A221X1_RVT)	0.05	0.82 f
ctmTdsLR_3_456/Y (INVX0_RVT)	0.03	0.85 r
ctmTdsLR_2_455/Y (NAND3X0_RVT)	0.03	0.87 f
ctmTdsLR_1_454/Y (INVX0_RVT)	0.03	0.90 r
U100/Y (0A22X1_RVT)	0.04	0.94 r
U101/Y (0A22X1_RVT)	0.04	0.99 r
ctmTdsLR_3_462/Y (INVX0_RVT)	0.01	0.99 f
ctmTdsLR_1_460/Y (NAND2X0_RVT)	0.05	1.05 r
U103/Y (NOR2X0_RVT)	0.05	1.10 f
a_eq_b_reg/D (DFFX1_RVT)	0.00	1.10 f
data arrival time		1.10
clock clk (rise edge)	3.00	3.00
clock network delay (propagated)	0.06	3.06
a_eq_b_reg/CLK (DFFX1_RVT)	0.00	3.06 r
clock uncertainty	-0.30	2.76
library setup time	-0.02	2.74
data required time		2.74
data required time		2.74
data arrival time		-1.10
slack (MET)		1.64

>report_qor

Cell Count	
Hierarchical Cell Count:	0
Hierarchical Port Count:	0
Leaf Cell Count:	51
Buf/Inv Cell Count:	23
Buf Cell Count:	3
Inv Cell Count:	20
Combinational Cell Count:	48
Single-bit Isolation Cell Count:	0
Multi-bit Isolation Cell Count:	0
Isolation Cell Banking Ratio:	0.00%
Single-bit Level Shifter Cell Count:	0
Multi-bit Level Shifter Cell Count:	0
Level Shifter Cell Banking Ratio:	0.00%
Single-bit ELS Cell Count:	0
Multi-bit ELS Cell Count:	0
ELS Cell Banking Ratio:	0.00%
Sequential Cell Count:	3
Integrated Clock-Gating Cell Count:	0
Sequential Macro Cell Count:	0
Single-bit Sequential Cell Count:	3
Multi-bit Sequential Cell Count:	0
Sequential Cell Banking Ratio:	0.00%
BitsPerflop:	1.00
Macro Count:	0

Area	
Combinational Area:	94.03
Noncombinational Area:	19.82
Buf/Inv Area:	38.12
Total Buffer Area:	10.17
Total Inverter Area:	27.96
Macro/Black Box Area:	0.00
Net Area:	0
Net XLength:	299.62
Net YLength:	354.79
Cell Area (netlist):	113.86
Cell Area (netlist and physical only):	113.86
Net Length:	654.41

Design Rules	
Total Number of Nets:	70
Nets with Violations:	17
Max Trans Violations:	17
Max Cap Violations:	0

5. Routing:

Routing connects all placed components based on the netlist, forming physical metal wires for signal, power, and clock nets. It consists of global and detailed routing while ensuring DRC compliance and minimizing parasitic effects.

Parasitic Effects:

In VLSI (Very Large-Scale Integration) design, **parasitic effects** refer to the unwanted resistance (R), capacitance (C), and sometimes inductance (L) that are unintentionally introduced by interconnect wires (metal traces) and device layouts during physical implementation of a chip.

Main causes of parasitic effects include: Long wires having resistances and capacitances, closely placed wires having capacitive coupling (crosstalk), Vias and contacts introducing resistance, Complex routing introducing distributed R and C, etc.

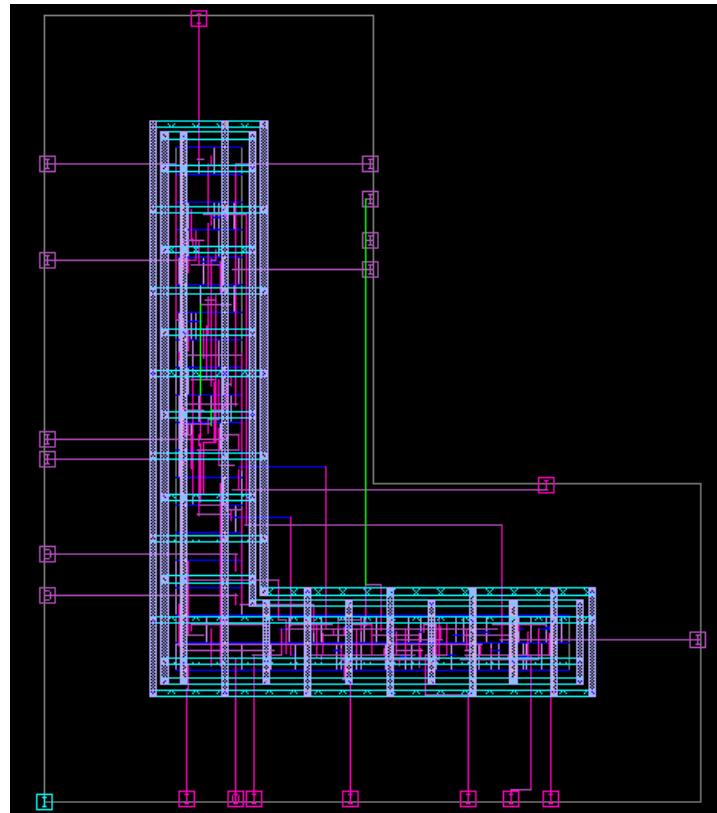
They are important because they can: Increase signal delays (slower performance), Distort signal waveforms (integrity issues), Causing timing violations (setup and hold failures), Increase power consumption,

For example, after routing our 8-bit comparator, actual wire lengths and placements are known. Tools like IC Compiler II extract parasitic data (RC values) and PrimeTime uses them to perform accurate Static Timing Analysis (STA) to ensure your chip still meets timing.

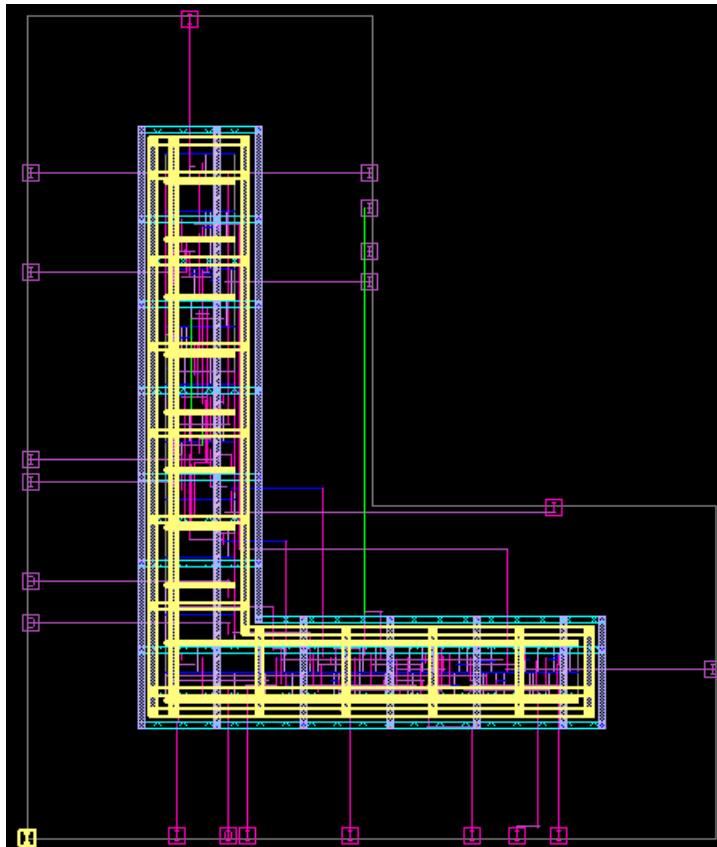
This is why it is said that:

“Pre-layout timing is ideal. Post-layout timing is real.”

```
>source scripts/route.tcl
```



(Highlighted nets that are connected to VDD)



>report_units

```
icc2_shell> report_units
*****
Report : user_units
Design : comparator_8bit
Version: W-2024.09
Date   : Mon Jun  2 17:46:27 2025
*****  
  
Input Units (set by technology library)  
-----  
time          : 1.00ns  
resistance    : 1.00MΩ  
capacitance   : 1.00fF  
voltage       : 1.00V  
current       : 1.00uA  
power         : 1.00pW  
length        : 1.00um  
energy        : 1.00pj/t  
  
Output Units (set by technology library)  
-----  
time          : 1.00ns  
resistance    : 1.00MΩ  
capacitance   : 1.00fF  
voltage       : 1.00V  
current       : 1.00uA  
power         : 1.00pW  
length        : 1.00um  
energy        : 1.00pj/t
```

>report_timing

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (propagated)	0.03	0.03
input external delay	0.50	0.53 f
b[3] (in)	0.00	0.53 f
ctmTdsLR_2_449/Y (NAND2X0_RVT)	0.12	0.64 r
ctmTdsLR_1_448/Y (INVX0_RVT)	0.04	0.68 f
U99/Y (OA222X1_RVT)	0.09	0.77 f
ctmTdsLR_4_457/Y (OA221X1_RVT)	0.05	0.82 f
ctmTdsLR_3_456/Y (INVX0_RVT)	0.04	0.86 r
ctmTdsLR_2_455/Y (NAND3X0_RVT)	0.03	0.89 f
ctmTdsLR_1_454/Y (INVX0_RVT)	0.03	0.92 r
U100/Y (OA22X1_RVT)	0.04	0.96 r
U101/Y (OA22X1_RVT)	0.04	1.00 r
ctmTdsLR_3_462/Y (INVX0_RVT)	0.01	1.01 f
ctmTdsLR_1_460/Y (NAND2X0_RVT)	0.05	1.06 r
U103/Y (NOR2X0_RVT)	0.05	1.12 f
a_eq_b_reg/D (DFFX1_RVT)	0.00	1.12 f
data arrival time		1.12
clock clk (rise edge)	3.00	3.00
clock network delay (propagated)	0.06	3.06
a_eq_b_reg/CLK (DFFX1_RVT)	0.00	3.06 r
clock uncertainty	-0.30	2.76
library setup time	-0.02	2.74
data required time		2.74
data required time		2.74
data arrival time		-1.12
slack (MET)		1.63

>report_qor

Cell Count	
Hierarchical Cell Count:	0
Hierarchical Port Count:	0
Leaf Cell Count:	50
Buf/Inv Cell Count:	22
Buf Cell Count:	2
Inv Cell Count:	20
Combinational Cell Count:	47
Single-bit Isolation Cell Count:	0
Multi-bit Isolation Cell Count:	0
Isolation Cell Banking Ratio:	0.00%
Single-bit Level Shifter Cell Count:	0
Multi-bit Level Shifter Cell Count:	0
Level Shifter Cell Banking Ratio:	0.00%
Single-bit ELS Cell Count:	0
Multi-bit ELS Cell Count:	0
ELS Cell Banking Ratio:	0.00%
Sequential Cell Count:	3
Integrated Clock-Gating Cell Count:	0
Sequential Macro Cell Count:	0
Single-bit Sequential Cell Count:	3
Multi-bit Sequential Cell Count:	0
Sequential Cell Banking Ratio:	0.00%
BitsPerflop:	1.00
Macro Count:	0

Area	
Combinational Area:	92.00
Noncombinational Area:	19.82
Buf/Inv Area:	36.09
Total Buffer Area:	8.13
Total Inverter Area:	27.96
Macro/Black Box Area:	0.00
Net Area:	0
Net XLength:	296.48
Net YLength:	362.45
Cell Area (netlist):	111.82
Cell Area (netlist and physical only):	111.82
Net Length:	658.93

Design Rules	
Total Number of Nets:	69
Nets with Violations:	18
Max Trans Violations:	18
Max Cap Violations:	0

PrimeTime: Static Timing Analysis (STA)

PrimeTime STA performs accurate timing analysis using post-route parasitic information. It ensures that the design meets all setup and hold timing constraints under worst-case conditions before tape-out.

run_pt_p1.tcl file code:

```
set report_default_significant_digits 6
set link_path "./../ref/lib/stdcell_rvt/saed32rvttt0p78vn40c.db"

read_verilog "./../ICClI/results/comp_8bit.routed.v"
link_design
current_design comparator_8bit

read_sdc "./../CONSTRAINTS/comparator_8bit.sdc"

read_parasitics "./../ICClI/results/comp_8bit_func::nom.spf.p1_125.spf"

update_timing -full

report_timing
report_design

check_timing -verbose > ./reports/check_timing/check_timing.p1_report
report_global_timing > ./reports/timing/report_global_timing.p1_report
report_clock_skew -attribute > ./reports/clock/report_clock.p1_report
report_analysis_coverage > ./reports/analysis_coverage/report_analysis_coverage.p1_report
report_timing -slack_lesser_than 0.0 -delay min_max -nosplit -input -net > ./reports/timing/report_timing.p1_report
```

All of the reports of Prime Time get generated inside: RTL2GDSII/PT/reports

> To run the Prime-Time shell, inside the RTL2GDSII/PT, type: **pt_shell**

> Next, just source the **run_pt_p1.tcl** file to get the output!

> **report_units**

```
pt_shell> report_units
*****
Report : units
Design : comparator_8bit
Version: W-2024.09
Date   : Mon Jun 2 17:56:18 2025
*****

Units
-----
Capacitive_load_unit      : 1e-15 Farad
Current_unit                : 1e-06 Amp
Resistance_unit             : 1e+06 Ohm
Time_unit                   : 1e-09 Second
Voltage_unit                 : 1 Volt
```

```
> report_timing
```

Point	Incr	Path
clock clk (rise edge)	0.000000	0.000000
clock network delay (ideal)	0.000000	0.000000
input external delay	0.500000	0.500000 f
b[3] (in)	0.000000	& 0.500000 f
ctmTdsLR_2_449/Y (NAND2X0_RVT)	0.265596	& 0.765596 r
ctmTdsLR_1_448/Y (INVX0_RVT)	0.111050	& 0.876646 f
U99/Y (OA222X1_RVT)	0.242207	& 1.118853 f
ctmTdsLR_4_457/Y (OA221X1_RVT)	0.142096	& 1.260949 f
ctmTdsLR_3_456/Y (INVX0_RVT)	0.089440	& 1.350389 r
ctmTdsLR_2_455/Y (NAND3X0_RVT)	0.082771	& 1.433160 f
ctmTdsLR_1_454/Y (INVX0_RVT)	0.090343	& 1.523503 r
U100/Y (OA22X1_RVT)	0.108363	& 1.631865 r
U101/Y (OA22X1_RVT)	0.115089	& 1.746955 r
ctmTdsLR_3_462/Y (INVX0_RVT)	0.035670	& 1.782625 f
ctmTdsLR_1_460/Y (NAND2X0_RVT)	0.112867	& 1.895491 r
U103/Y (NOR2X0_RVT)	0.132511	& 2.028002 f
a_eq_b_reg/D (DFFX1_RVT)	0.000008	& 2.028009 f
data arrival time		2.028009
clock clk (rise edge)	3.000000	3.000000
clock network delay (ideal)	0.000000	3.000000
a_eq_b_reg/CLK (DFFX1_RVT)		3.000000 r
clock reconvergence pessimism	0.000000	3.000000
clock uncertainty	-0.300000	2.700000
library setup time	-0.087736	2.612264
data required time		2.612264

data required time		2.612264
data arrival time		-2.028009

slack (MET)		0.584255

And finally, our Slack is MET with the given conditions to be +ve and less than 1!

```
> report_qor
```

```
pt_shell> report_qor
*****
Report : qor
Design : comparator_8bit
Version: W-2024.09
Date   : Mon Jun 2 17:56:33 2025
*****  
  
Timing Path Group 'clk' (max_delay/setup)
-----
Levels of Logic:                                12
Critical Path Length:                          2.028009
Critical Path Slack:                           0.584255
Total Negative Slack:                          0.000000
No. of Violating Paths:                         0  
  
Area
-----
Net Interconnect area:                         9.917094
Total cell area:                            111.823395
Design Area:                                 121.740486  
  
Cell & Pin Count
-----
Pin Count:                                    159
Hierarchical Cell Count:                      0
Hierarchical Port Count:                      0
Leaf Cell Count:                             50  
  
Design Rule Violations
-----
Total No. of Pins in Design:                 159
max_transition Count:                        46
max_transition Cost:                         10.778155
Total DRC Cost:                            10.778155
```

Learnings & Outcome

Through this 5-Day RTL to GDSII Workshop, I gained a complete hands-on understanding of how a digital design evolves from a behavioral RTL description to a fully layout-ready GDSII format, suitable for tapeout. The key learnings and outcomes from this project include:

- ✓ Learned to write Verilog RTL code for a sequential design with clocked logic and simulate it using industry-standard tools like Synopsys VCS and Verdi.
- ✓ Understood the concept of Register Transfer Level (RTL) and how to test designs through waveform debugging.
- ✓ Gained practical experience with logic synthesis using Design Compiler, including applying timing constraints, cell selection (using set_dont_use), and analysing reports (QoR, timing, area).
- ✓ Learned how to perform Physical Design using IC Compiler II: from floor planning, power planning, placement, clock tree synthesis, and routing.
- ✓ Understood the importance of parasitic extraction and how real post-layout timing differs from ideal pre-layout timing.
- ✓ Learned to use PrimeTime for post-route Static Timing Analysis (STA) to ensure timing closure under realistic, worst-case conditions.
- ✓ Gained experience in writing and organizing industry-grade TCL scripts to automate flows.
- ✓ Successfully achieved a positive and acceptable timing slack (< 1ns), met all STA requirements.

This workshop has solidified my practical understanding of the complete front-end to back-end VLSI flow and has prepared me to handle industrial-grade ASIC design tasks with confidence.

Complete Git-Hub Repository for the Project: [Github Repository](#)