ECE559 Report

cl344

December 2018

1 Static Timing Analysis

The Timing Analysis is operated with the Base Clock at 50 HMz. We used Post-fit and Fast-corner for a full timing analysis.

1.1 Identifications

1.1.1 Worst Case Slack

Slack indicates that the clock meets the requirement with some margin, so larger sack is better. According to the "Report All Core Time" page in our design, The Worst Case Slack against Setup Violations is 13.307 ns. From this result, we are confident that we don't have any failing path since there's no negative slack for the clock domain.

1.1.2 Maximum Frequency

According to the "Report FMax Summary", we find that the maximum frequency at which our design can be clocked is 149.41 MHz.

1.1.3 Critical Path

By using the "Report Worst Case Path" function, we find that the worst data delay is 6.528 ns and the path of Worst Case Slack is:

shiftreg_buf:input_shiftreg_inst1—mem[1464] : (0.232 ns)
input_shiftreg_inst1—mem[1464]—q : (0 ns)
reg_inst—Q[1464]—asdata : (5.89 ns)
reg6144:comb_6149—Q[1464] : (0.406 ns)

In the Path above, reg_inst—Q[1464]—asdata is the Critical Path since it takes the longest delay which is 5.89 ns.

1.2 Max Throughput

We are using the following equation to calculate Thoughput:

$$Throughput = DataPerClockPeriod * ClockFrequency \quad (1)$$

According to the euqation above, with Max Frequency as 83.89 MHz and data per clock period as 8 bits, we have:

$$MaxThroughput = 8bits * 83.89MHz = 0.67bits/ns = 671.14MB/sec \quad (2)$$

According to the calculation above, the Max Throughput is estimated to be 671.14 MB/sec.

1.3 Modification

The initial design includes redundant wires, which yields a Worst Case Slack as 8.079 ns and Max Frequency as 83.89 MHz. After removing the redundant wires, the Worst Case Slack is 13.307 ns and the Max Frequency increases to 149.41 MHz. The comparison below shows the improvements of the new design.

1.3.1 Worst Path Comparison

- Before Wire Reduction:
  shiftreg_buf:input_shiftreg_inst1—mem[4653] : (0.232 ns)
  input_shiftreg_inst1—mem[4653]—q : (0 ns)
  comb_6149—Q[4653]—asdata : (11.216 ns)
  reg6144:comb_6149—Q[4653] : (0.406 ns)

- After Wire Reduction:
  shiftreg_buf:input_shiftreg_inst1—mem[1464] : (0.232 ns)
  input_shiftreg_inst1—mem[1464]—q : (0 ns)
  reg_inst—Q[1464]—asdata : (5.89 ns)
  reg6144:comb_6149—Q[1464] : (0.406 ns)

1.3.2 All Clock Histogram Comparison

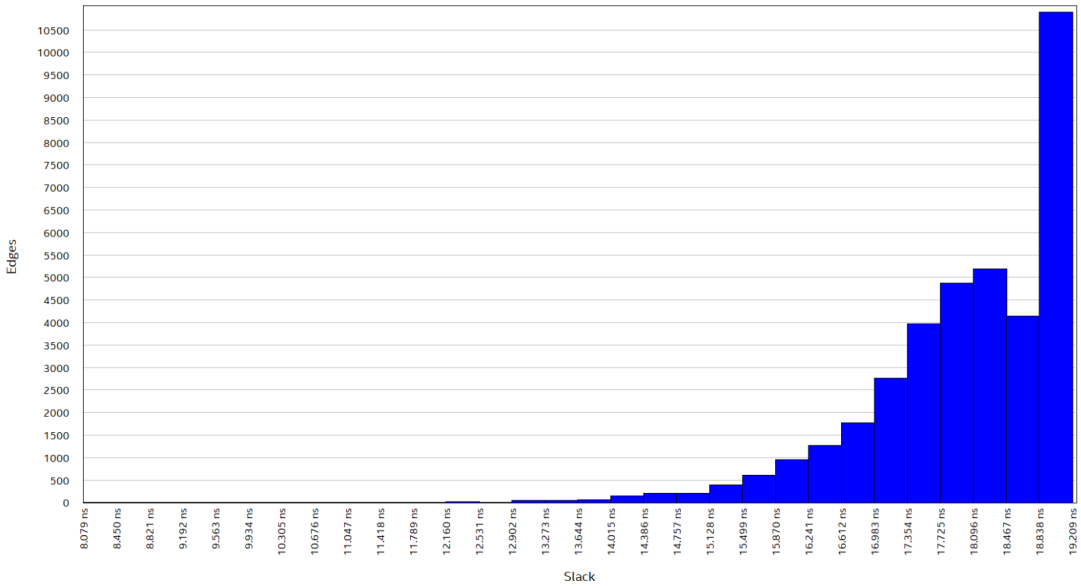

Figure 1: All Clock Histogram before wire reduction

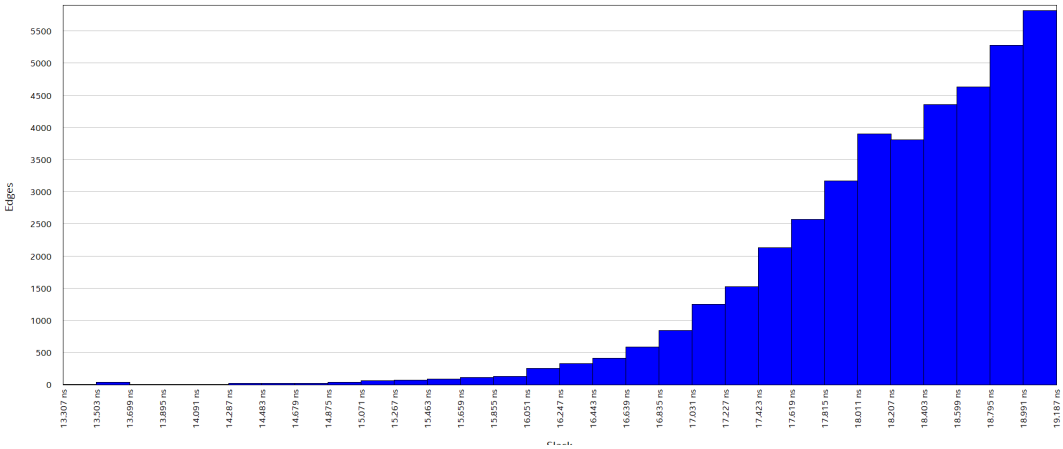

Figure 2: All Clock Histogram after wire reduction