ECE559 Fall2018, Constituent Coder Interleaver Group

Group Design Report

xxx

November 29, 2018

1 A high-level description of the function

I wonder if vinith can do this 1. A high-level description of the function for which the team was responsible, including: o how this function relates to the overall function of the encoder stack o how this set of functions relates to the relevant 3GPP standards

2 Description of the design

2. Description of the design, including: (mostly yao) o interfaces to other functions in the encoder stack (mostly yao) o identification of the data path through the function and how the data path is controlled by FSMs, shown using a block diagram of the design as implemented. o for data path and associated combinational logic (not FSMs), include the RTL view from Quartus, with a brief prose description; this can be used to describe the block diagram mentioned in the previous bullet

(mostly yao) o FSM designs, with pictorial description (state transition diagrams) and text, clearly indicating what each state represents, how inputs determine the next state and Moore and Mealy outputs for each state, and also an indication of how the FSM is related to data flow through the function

3 Static timing analysis

(mostly cheng) 3. Static timing analysis o from the static timing analysis results, identify (a) worst-case slack against setup violations; (b) maximum frequency at which the design can be clocked; (c) the critical path corresponding to the worst-case slack. o based on the max frequency, comment on the max throughput that can be sustained by the function given the current design

4 Simulation results

(mostly yao) 4. Simulation results o what was simulated, what were the test conditions, what is the significance of the test in the context of the subsystem function o show on the plots of the results, by clear annotation on the plots, and in a prose discription, what the simulation results indicate with respect to operation and performance of the subsystem

5 Hardware test results

(mostly vinith) 5. Hardware test results o what was run on the hardware, was it run at speed or "statically"? o show appropriate indication of the test results (e.g. prints of logic analyzer displays), with clear annotation on the plots and accompanying prose decription o what were the test conditions, what is the significance of the test in the context of the subsystem function o relationship to simulation test results

6 A1

The circuit in Figure 6.8 was and simulated to find A1. Here're the simulation result:

Figure 1: Log magnitude and phase of A1

7 Closed-loop gain of non-inverting mode amplifier

The non-inverting mode amplifier circuit was built and simulated to find closed-loop gain Af. Here're the simulation result:

8 Design an inverting mode amplifier

Here are the conditions required:

$$VS/RS = -VO/RF$$
$$VO/VS = -RF/RS = -4$$