VLSI PROJECT REPORT

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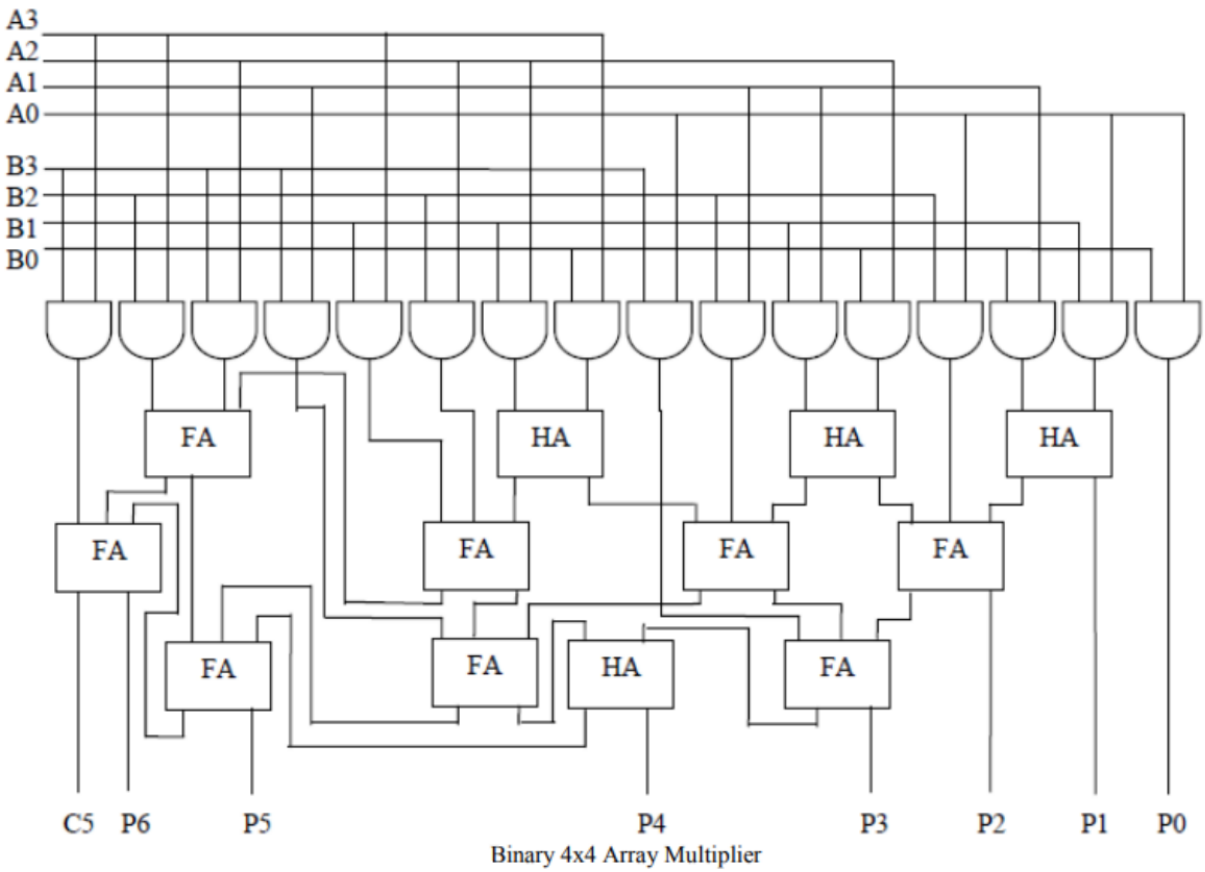
`NGSPICE`

1)

To make a ngspice circuit i used the following circuit:



Binary 4x4 Array Multiplier

i made a subckt for fulladder and a and gates using pmos and nmos gates and used them to implement the above circuit

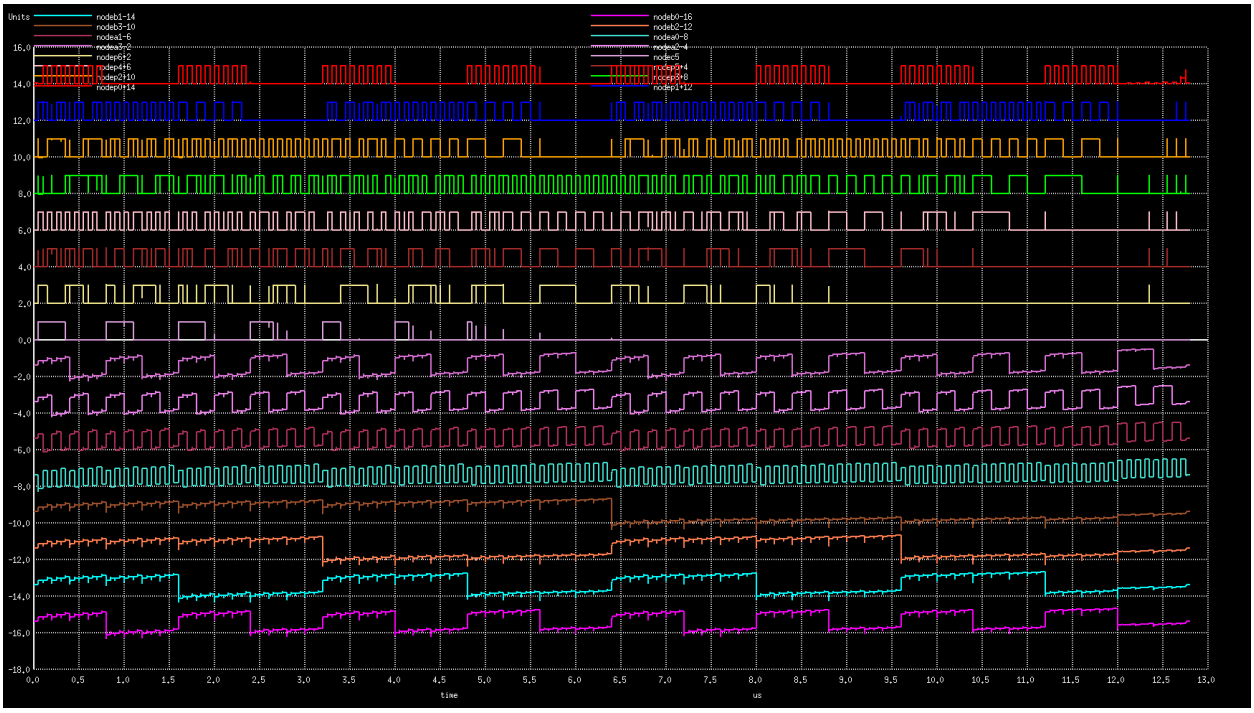
```
subckt adder nodeA nodeB nodeC nodesum nodecarry vddd! gndd!
Mn1 node11  nodeA gndd! gndd!   nmos W={1*XX*Wmin} L={Lmin}
Mn2 node10  nodeA gndd! gndd!   nmos W={1*XX*Wmin} L={Lmin}
Mn3 node10  nodeB gndd! gndd!   nmos W={1*XX*Wmin} L={Lmin}
Mn4 node9 nodeC gndd! gndd!   nmos W={1*XX*Wmin} L={Lmin}
Mn5 node9 nodeA gndd! gndd!   nmos W={1*XX*Wmin} L={Lmin}
Mn6 node9 nodeB gndd! gndd!   nmos W={1*XX*Wmin} L={Lmin}
Mn7 node8 nodeA gndd! gndd!   nmos W={1*XX*Wmin} L={Lmin}
Mn8 node7 nodeB node8 gndd!   nmos W={1*XX*Wmin} L={Lmin}
Mn9 node6 nodeC node7 gndd!   nmos W={1*XX*Wmin} L={Lmin}
Mn10  node6 node12  node9 gndd!   nmos W={1*XX*Wmin} L={Lmin}
Mn11  node12  nodeC node10  gndd!   nmos W={1*XX*Wmin} L={Lmin}
Mn12  node12  nodeB node11  gndd!   nmos W={1*XX*Wmin} L={Lmin}
Mp1 node1 nodeA vddd! vddd!   pmos W={2*XX*Wmin} L={Lmin}
Mp2 node2 nodeA vddd! vddd!   pmos W={2*XX*Wmin} L={Lmin}
Mp3 node2 nodeB vddd! vddd!   pmos W={2*XX*Wmin} L={Lmin}
Mp4 node3 nodeC vddd! vddd!   pmos W={2*XX*Wmin} L={Lmin}
Mp5 node3 nodeA vddd! vddd!   pmos W={2*XX*Wmin} L={Lmin}
Mp6 node3 nodeB vddd! vddd!   pmos W={2*XX*Wmin} L={Lmin}
Mp7 node4 nodeA vddd! vddd!   pmos W={2*XX*Wmin} L={Lmin}
Mp8 node5 nodeB node4 vddd!   pmos W={2*XX*Wmin} L={Lmin}
Mp9 node6 nodeC node5 vddd!   pmos W={2*XX*Wmin} L={Lmin}
Mp10  node6 node12  node3 vddd!   pmos W={2*XX*Wmin} L={Lmin}
Mp11  node12  nodeC node2 vddd!   pmos W={2*XX*Wmin} L={Lmin}
Mp12  node12  nodeB node1 vddd!   pmos W={2*XX*Wmin} L={Lmin}
Mp13    nodesum node6  vddd!   vddd!    pmos W={2*XX*Wmin} L={Lmin}
Mp14    nodecarry node12  vddd!   vddd!    pmos W={2*XX*Wmin} L={Lmin}
Mn13    nodesum node6  gndd!   gndd!    nmos W={1*XX*Wmin} L={Lmin}
Mn14    nodecarry node12  gndd!   gndd!    nmos W={1*XX*Wmin} L={Lmin}

.ends adder

.subckt and nodeA nodeB node6 vddd! gndd!
Mp1 node5 nodeA vddd! vddd!   pmos W={2*XX*Wmin} L={Lmin}
Mp2 node5 nodeB vddd!   vddd!   pmos W={2*XX*Wmin} L={Lmin}
Mn1 node4 nodeA gndd!   gndd!   nmos W={1*XX*Wmin} L={Lmin}
Mn2 node5 nodeB node4   gndd!   nmos W={1*XX*Wmin} L={Lmin}
Mn3 node6   node5   gndd!   gndd!   nmos W={1*XX*Wmin} L={Lmin}
Mp3 node6   node5   vddd!   vddd!   pmos W={2*XX*Wmin} L={Lmin}
.ends and
```

i gave a input which takes into account every possible combination

```
VinA0 nodeA0 0 pulse 0 1 0 100p 100p 50n 100n
VinA1 nodeA1 0 pulse 0 1 0 100p 100p 100n 200n
VinA2 nodeA2 0 pulse 0 1 0 100p 100p 200n 400n
VinA3 nodeA3 0 pulse 0 1 0 100p 100p 400n 800n
VinB0 nodeB0 0 pulse 0 1 0 100p 100p 800n 1600n
VinB1 nodeB1 0 pulse 0 1 0 100p 100p 1600n 3200n
```

```
VinB2 nodeB2 0 pulse 0 1 0 100p 100p 3200n 6400n
VinB3 nodeB3 0 pulse 0 1 0 100p 100p 6400n 12800n
```

the plot of the following is:



2)

Now to calculate power of the circuit i wrote a python script which gives every input to my spice file

i calculated power by multiplying current and voltage of every input

```
power = inA3*iinA3 + inB3*iinB3 +inA2*iinA2 +inB2*iinB2 +inA1*iinA1 +inB1*iinB1 +inA0*iinA0 +inB0*iinB0
```

i stored every power in the file `power_smaples.txt` i got the maximum power as:

```
            max leakage power:              5.72481E-07
```

3)

To calculate delay i found 50 paths in the circuit and i put in a file `delay.txt`

Max delay came out to be:

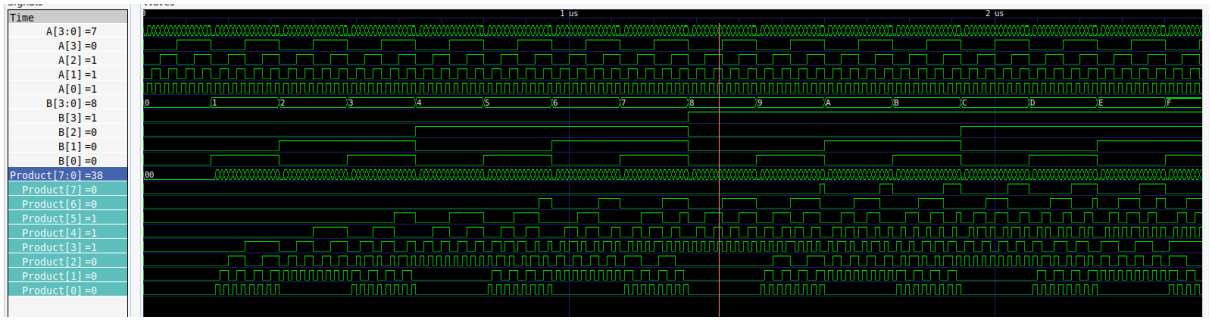
```
            max delay :     -4.246739e-09
```

VERILOG

i wrote structural code for the following :

1. Half Adder
2. Full adder
3. 4 bit adder
4. Multiplier

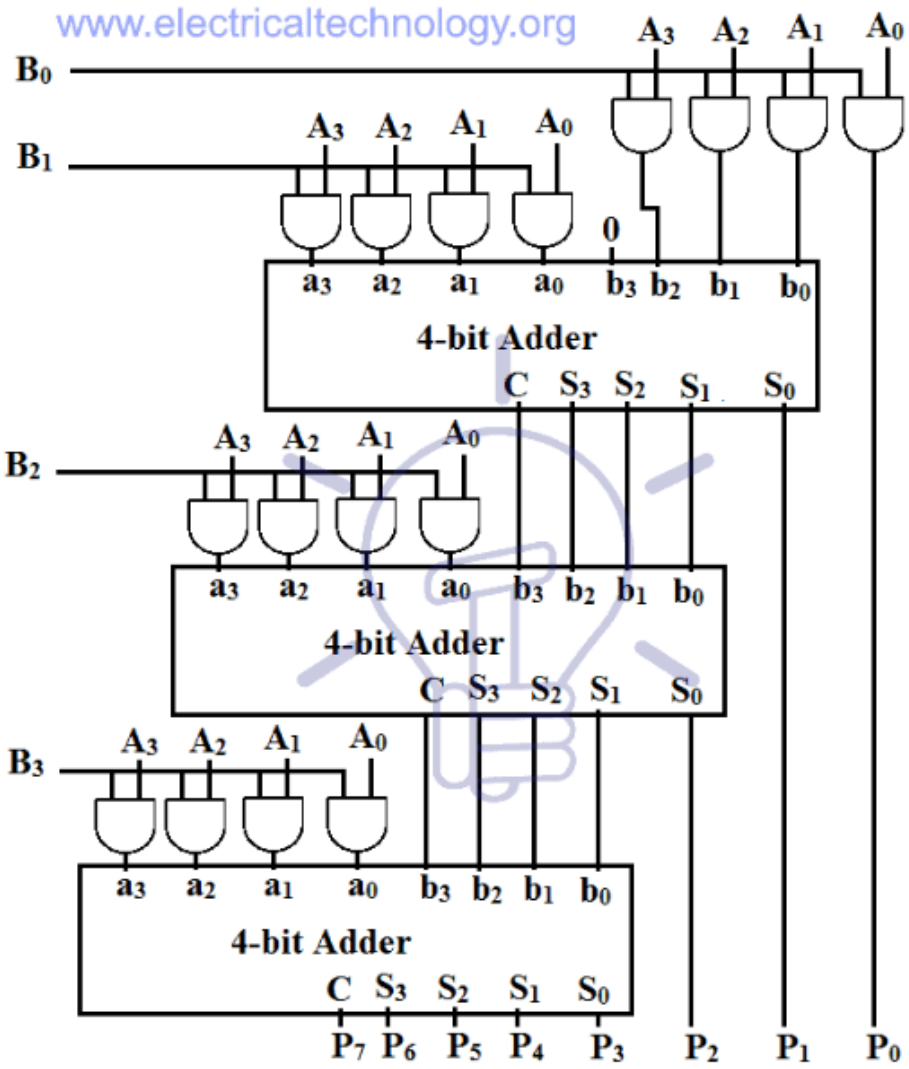
then i wrote a test bench code to give all inputs to my file and my output(gtkwave) was:



In this we can also see that 7 multiplied by 8 is 56

and output coming is in hexadecimal which is 38 = 3x16 + 8 = 56 in binary which is correct

this design is :

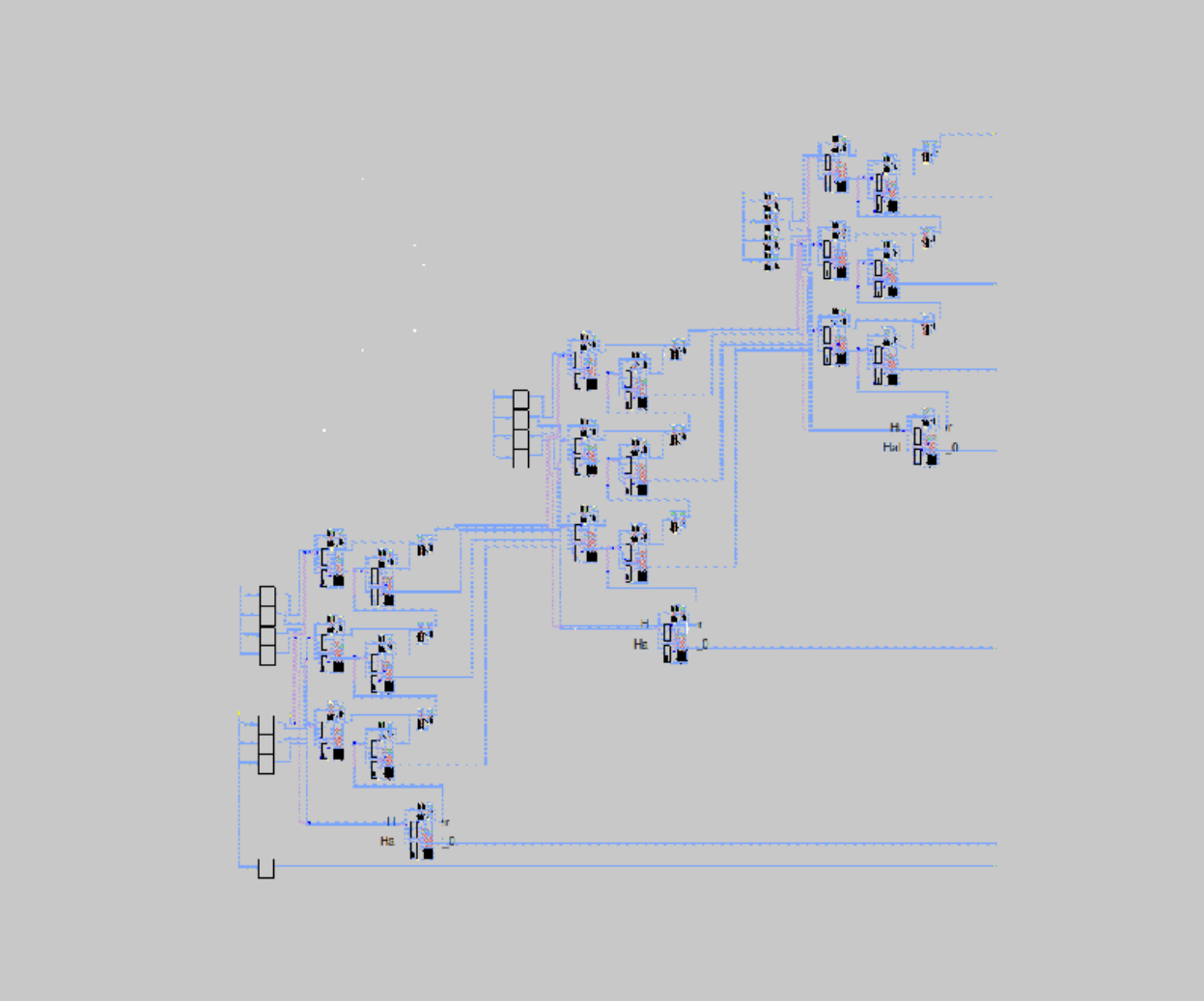


now we can verify the output of 2 circuit and verify their functioning

MAGIC

i made my magic layout using different blocks from start like inverte,and gate , or gate , adder , xor and then used all of them in the final layout

my layout is:



extract it into spice by the following commands:

```
extraxt all
ext2spice Multiplier_4x4.ext
```

then in the spice code change nfet to nmos and pfet to pmos,give inputs and plotted the output and verified that it is working