ESS Technology, Inc.

ES9012 / ES9018
SABRE32 Reference 32-bit Audio DAC
Datasheet

OVERVIEW

The ***SABRE32 Reference*** audio DAC series is the world's highest performance 32-bit audio DAC solution targeted for consumer applications such as Blu-ray players, audio pre-amplifiers, A/V receivers and professional applications such as recording systems, mixer consoles and digital audio workstations.

Part Number	Description	Package	DNR (dB)	THD (dB)	32-bit DAC	I2S/DSD Input	SPDIF Input	Jitter Reduction
ES9018	***SABRE32 Reference 8-Channel* Audio DAC**	64-LQFP	135 (mono) 129 (8ch)	-120	Yes	Yes	Yes	Yes
ES9012	***SABRE32 Reference Stereo Audio DAC***	64-LQFP	135 (mono) 133 (2ch)	-120	Yes	Yes	Yes	Yes

With ESS patented 32-bit Hyperstream™ DAC architecture and Time Domain Jitter Eliminator, the ***SABRE32 Reference Stereo DAC*** delivers an unprecedented DNR of up to 135dB and THD+N of -120dB, the industry's highest performance level that will satisfy the most demanding audio enthusiasts.

The ***SABRE32 Reference*** audio DAC's 32-bit Hyperstream™ architecture can handle full 32-bit PCM data via I2S input, as well as DSD or SPDIF data. The ***SABRE32 Reference*** supports up to 1.536MHz[1] input sampling rates and consumes less than 100mW.

KEY FEATURES

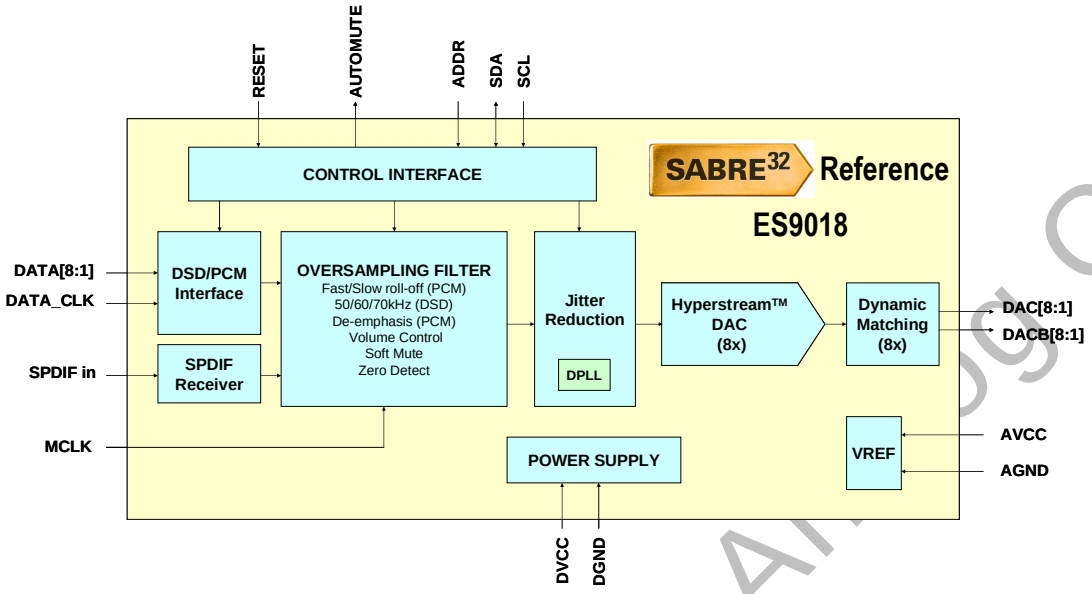
Feature	Benefit
Patented 32-bit Hyperstream™ DAC o Up to 135dB DNR o -120dB THD+N	Industry's highest performance 32-bit audio DAC with unprecedented dynamic range and ultra low distortion
Patented Time Domain Jitter Eliminator	Unmatched audio clarity free from input clock jitter
Universal digital input for up to 1.536MHz[1] sampling rate	Supports SPDIF, PCM (I2S, MSB/LSB justified 16-32-bit) or DSD input with DVD Audio and SACD compatibility.
Integrated DSP functions	Click-free soft mute and volume control Programmable filter characteristics for PCM/DSD Programmable Zero detect De-emphasis for 32, 44.1 and 48kHz sampling
Customizable output configuration	Mono, stereo, 8-channel (ES9018 only) output in current or voltage mode based on performance criterion
Customizable filter characteristics	User programmable filter allowing custom roll-off response
100mW power consumption	Simplifies power supply design

APPLICATIONS

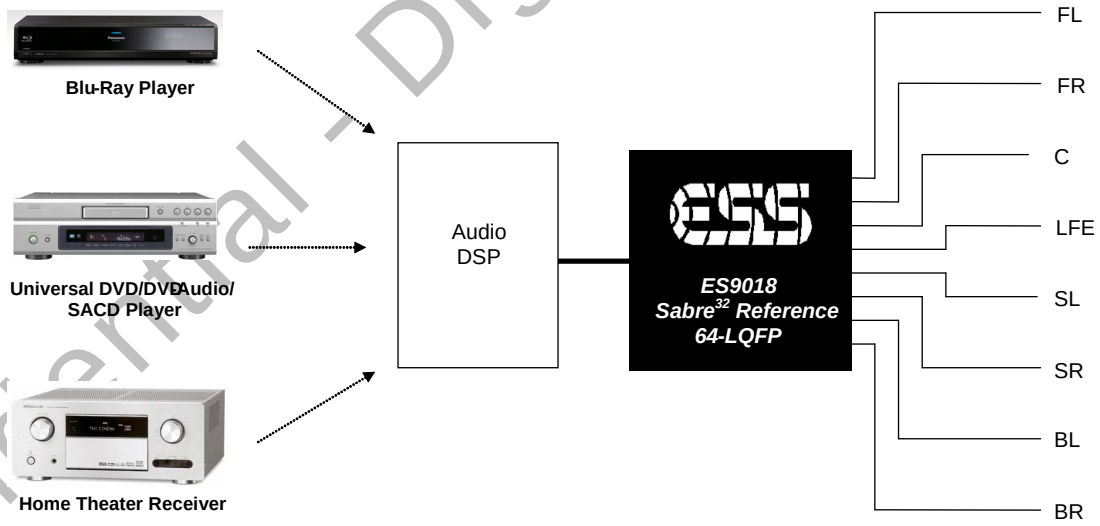
- Blu-ray / SACD / DVD-Audio player
- Audio preamplifier and receiver
- A/V processor
- Professional audio recording systems and mixing consoles
- Digital audio workstation

1. This is for oversample bypass mode only. The maximum sample rate using the internal oversampling filters is 500kHz.

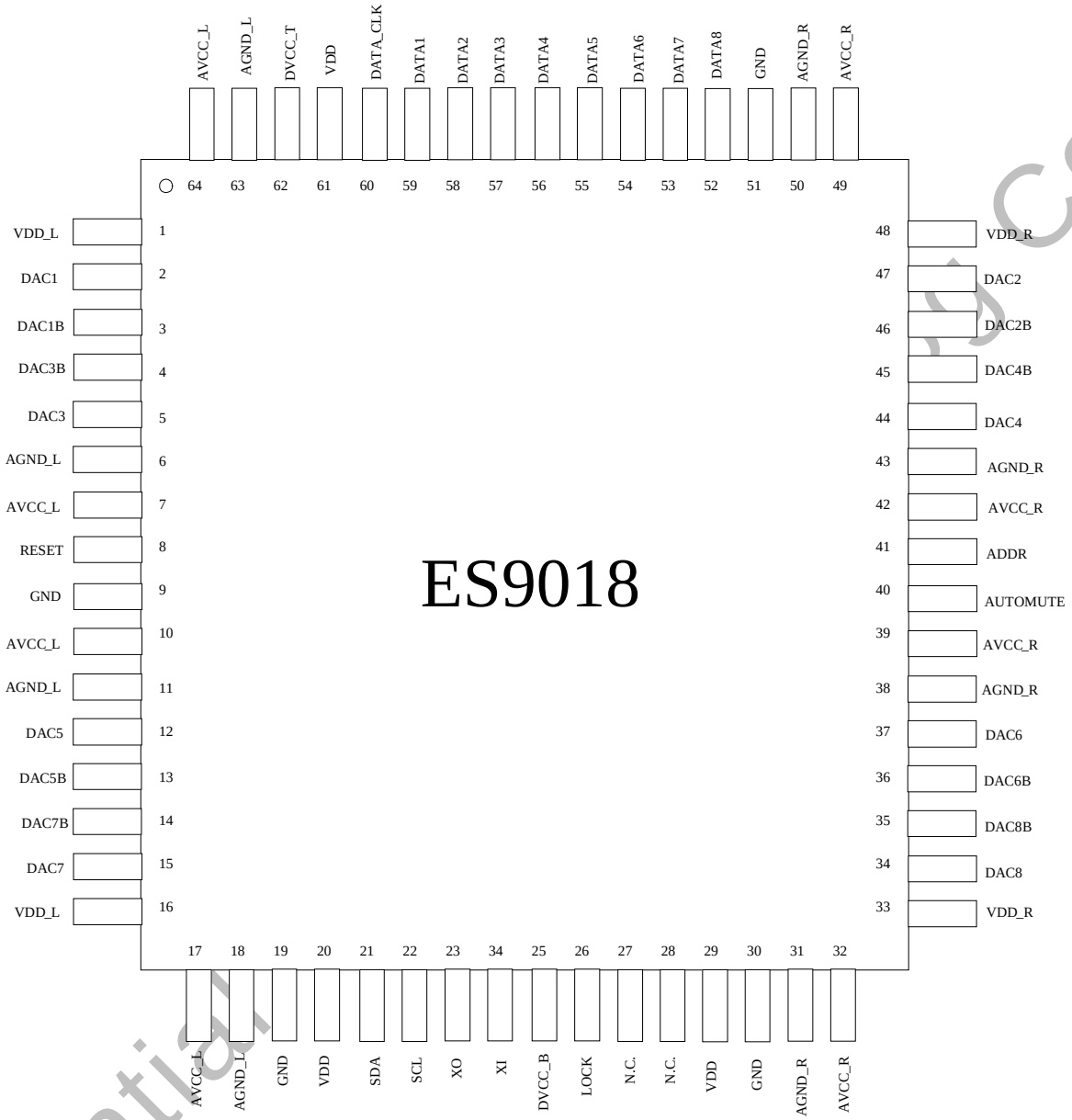
FUNCTIONAL BLOCK DIAGRAM (ES9018)



APPLICATION DIAGRAM (ES9018)



PIN LAYOUT (ES9018)



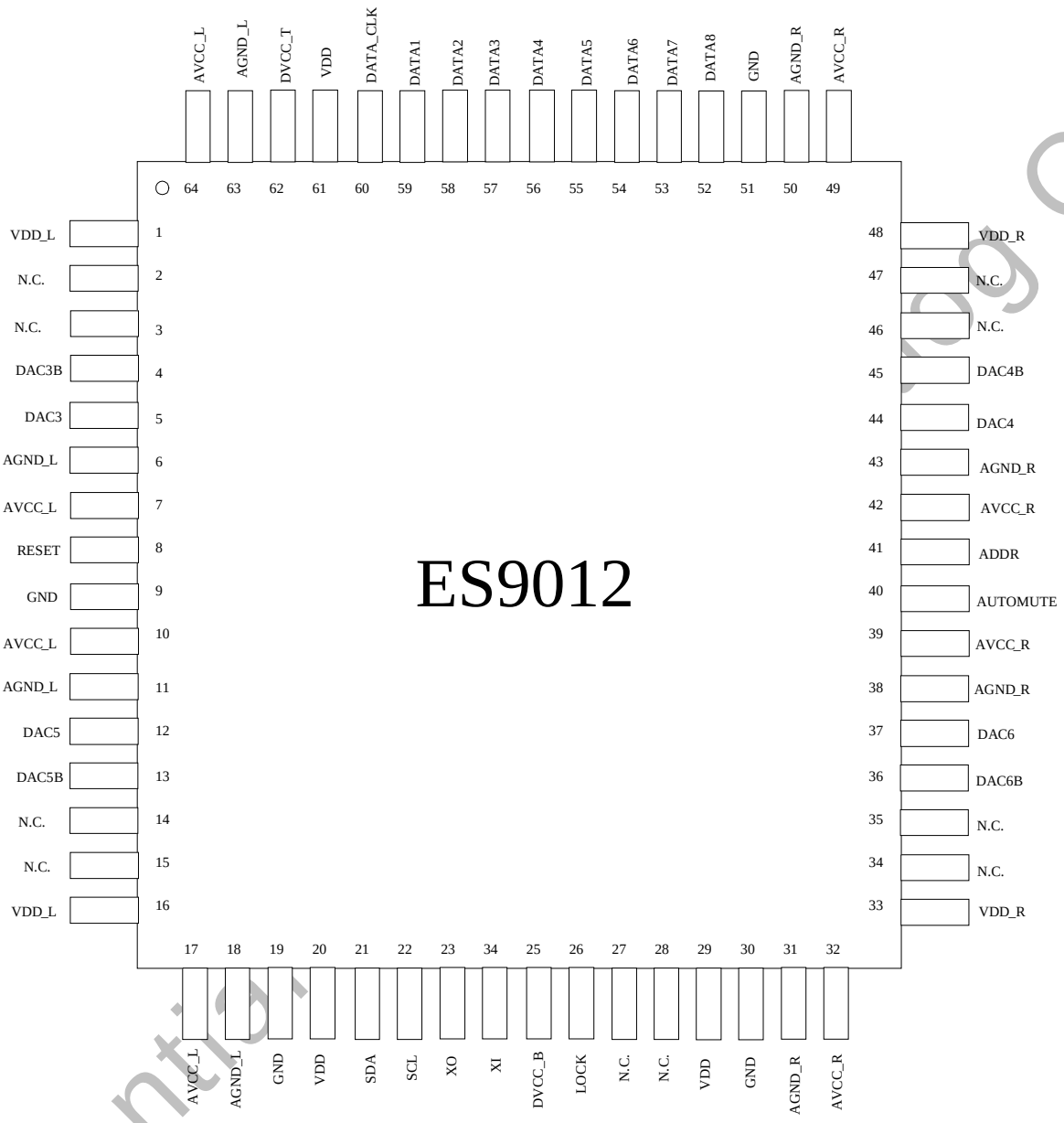
PIN DESCRIPTION (ES9018)

Pin	Name	I/O	Description
1	VDD_L	-	Analog Power (+1.2V) for Left channels
2	DAC1	O	Differential Positive Analog Output 1
3	DAC1B	O	Differential Negative Analog Output 1
4	DAC3B	O	Differential Negative Analog Output 3
5	DAC3	O	Differential Positive Analog Output 3
6	AGND_L	-	Analog Ground for Left channels
7	AVCC_L	-	Analog Power (+3.3V) for Left channels
8	RESET	I	Global Reset
9	GND	-	Digital Ground
10	AVCC_L	-	Analog Power (+3.3V) for Left channels
11	AGND_L	-	Analog Ground for Left channels
12	DAC5	O	Differential Positive Analog Output 5
13	DAC5B	O	Differential Negative Analog Output 5
14	DAC7B	O	Differential Negative Analog Output 7
15	DAC7	O	Differential Positive Analog Output 7
16	VDD_L	-	Analog Power (+1.2V) for Left channels
17	AVCC_L	-	Analog Power (+3.3V) for Left channels
18	AGND_L	-	Analog Ground for Left channels
19	GND	-	Digital Ground
20	VDD	-	Digital Power (+1.2V) for core of chip
21	SDA	I/O	I2C SDA
22	SCL	I	I2C SCL
23	XO	O	Xtal oscillator output
24	XI (MCLK)	I	Xtal oscillator input (Note: can also just be a clock input)
25	DVCC_B	-	Digital Power (+3.3V) for bottom pad ring of chip
26	LOCK	O	Lock output
27	N.C.		Not connected (leave open)
28	N.C.		Not connected (leave open)
29	VDD	-	Digital Power (+1.2V) for core of chip
30	GND	-	Digital Ground
31	AGND_R	-	Analog Ground for Right channels
32	AVCC_R	-	Analog Power (+3.3V) for Right channels
33	VDD_R	-	Analog Power (+1.2V) for Right channels
34	DAC8	O	Differential Positive Analog Output 8
35	DAC8B	O	Differential Negative Analog Output 8
36	DAC6B	O	Differential Negative Analog Output 6
37	DAC6	O	Differential Positive Analog Output 6
38	AGND_R	-	Analog Ground for Right channels
39	AVCC_R	-	Analog Power (+3.3V) for Right channels

Pin	Name	I/O	Description
40	AUTMOMUTE	O	Automute
41	ADDR	I	Chip Address Select
42	AVCC_R	-	Analog Power (+3.3V) for Right channels
43	AGND_R	-	Analog Ground for Right channels
44	DAC4	O	Differential Positive Analog Output 4
45	DAC4B	O	Differential Negative Analog Output 4
46	DAC2B	O	Differential Negative Analog Output 2
47	DAC2	O	Differential Positive Analog Output 2
48	VDD_R	-	Analog Power (+1.2V) for Right channels
49	AVCC_R	-	Analog Power (+3.3V) for Right channels
50	AGND_R	-	Analog Ground for Right channels
51	GND	-	Digital Ground
52	DATA8	I	DSD Data8 OR SPDIF Input8
53	DATA7	I	DSD Data7 OR SPDIF Input7
54	DATA6	I	DSD Data6 OR SPDIF Input6
55	DATA5	I	DSD Data5 OR PCM Data CH7/CH8 OR SPDIF Input5
56	DATA4	I	DSD Data4 OR PCM Data CH5/CH6 OR SPDIF Input4
57	DATA3	I	DSD Data3 OR PCM Data CH3/CH4 OR SPDIF Input3
58	DATA2	I	DSD Data2 OR PCM Data CH1/CH2 OR SPDIF Input2
59	DATA1	I	DSD Data1 OR PCM Frame Clock OR SPDIF Input1
60	DATA_CLK	I	PCM Bit Clock OR DSD Bit Clock
61	VDD	-	Digital Power (+1.2V) for core of chip
62	DVCC_T	-	Digital Power (+3.3V) for top pad ring of chip
63	AGND_L	-	Analog Ground for Left channels
64	AVCC_L	-	Analog Power (+3.3V) for Left channels

Table 1.1

PIN LAYOUT (ES9012)



PIN DESCRIPTION (ES9012)

Pin	Name	I/O	Description
1	VDD_L	-	Analog Power (+1.2V) for Left channels
2	N.C.	-	Not connected
3	N.C.	-	Not connected
4	DAC3B	O	Differential Negative Analog Output 3 (Left Channel)
5	DAC3	O	Differential Positive Analog Output 3 (Left Channel)
6	AGND_L	-	Analog Ground for Left channels
7	AVCC_L	-	Analog Power (+3.3V) for Left channels
8	RESET	I	Global Reset
9	GND	-	Digital Ground
10	AVCC_L	-	Analog Power (+3.3V) for Left channels
11	AGND_L	-	Analog Ground for Left channels
12	DAC5	O	Differential Positive Analog Output 5 (Left Channel)
13	DAC5B	O	Differential Negative Analog Output 5 (Left Channel)
14	N.C.	-	Not connected
15	N.C.	-	Not connected
16	VDD_L	-	Analog Power (+1.2V) for Left channels
17	AVCC_L	-	Analog Power (+3.3V) for Left channels
18	AGND_L	-	Analog Ground for Left channels
19	GND	-	Digital Ground
20	VDD	-	Digital Power (+1.2V) for core of chip
21	SDA	I/O	I2C SDA
22	SCL	I	I2C SCL
23	XO	O	Xtal oscillator output
24	XI (MCLK)	I	Xtal oscillator input (Note: can also just be a clock input)
25	DVCC_B	-	Digital Power (+3.3V) for bottom pad ring of chip
26	LOCK	O	Lock output
27	N.C.		Not connected (leave open)
28	N.C.		Not connected (leave open)
29	VDD	-	Digital Power (+1.2V) for core of chip
30	GND	-	Digital Ground
31	AGND_R	-	Analog Ground for Right channels
32	AVCC_R	-	Analog Power (+3.3V) for Right channels
33	VDD_R	-	Analog Power (+1.2V) for Right channels
34	N.C.	-	Not connected
35	N.C.	-	Not connected
36	DAC6B	O	Differential Negative Analog Output 6 (Right Channel)
37	DAC6	O	Differential Positive Analog Output 6 (Right Channel)
38	AGND_R	-	Analog Ground for Right channels
39	AVCC_R	-	Analog Power (+3.3V) for Right channels

Pin	Name	I/O	Description
40	AUTMOMUTE	O	Automute
41	ADDR	I	Chip Address Select
42	AVCC_R	-	Analog Power (+3.3V) for Right channels
43	AGND_R	-	Analog Ground for Right channels
44	DAC4	O	Differential Positive Analog Output 4 (Right Channel)
45	DAC4B	O	Differential Negative Analog Output 4 (Right Channel)
46	N.C.	-	Not connected
47	N.C.	-	Not connected
48	VDD_R	-	Analog Power (+1.2V) for Right channels
49	AVCC_R	-	Analog Power (+3.3V) for Right channels
50	AGND_R	-	Analog Ground for Right channels
51	GND	-	Digital Ground
52	DATA8	I	DSD Data8 OR SPDIF Input8
53	DATA7	I	DSD Data7 OR SPDIF Input7
54	DATA6	I	DSD Data6 OR SPDIF Input6
55	DATA5	I	DSD Data5 OR PCM Data CH7/CH8 OR SPDIF Input5
56	DATA4	I	DSD Data4 OR PCM Data CH5/CH6 OR SPDIF Input4
57	DATA3	I	DSD Data3 OR PCM Data CH3/CH4 OR SPDIF Input3
58	DATA2	I	DSD Data2 OR PCM Data CH1/CH2 OR SPDIF Input2
59	DATA1	I	DSD Data1 OR PCM Frame Clock OR SPDIF Input1
60	DATA_CLK	I	PCM Bit Clock OR DSD Bit Clock
61	VDD	-	Digital Power (+1.2V) for core of chip
62	DVCC_T	-	Digital Power (+3.3V) for top pad ring of chip
63	AGND_L	-	Analog Ground for Left channels
64	AVCC_L	-	Analog Power (+3.3V) for Left channels

Table 1.2

FUNCTIONAL DESCRIPTION

PCM, SPDIF and DSD Pin Connections

The following tables show how the pins are used for PCM and DSD audio formats.

PCM Audio Format
Note: XI clock (MCLK) must be > 192*FS when using PCM input (normal mode).
Note: XI clock (MCLK) must be > 24*FS when using PCM input (OSF bypass mode).

Pin Name	Description
DATA1	Frame clock
DATA[2:5]	8-channel PCM serial data
DATA_CLK	Bit clock for PCM audio format

Table 2

SPDIF Audio Formant
Note: XI clock (MCLK) must be > 386*FS when using SPDIF input.

Pin Name	Description
DATA[1:8]	Up to 8 SPDIF inputs can be connected to an 8-to-1 mux internal to ***SABRE^{32} Reference***, selectable via register SPDIF Source

Table 3

DSD Audio Format
Note: XI clock (MCLK) must be > 3*FS when using DSD input.

Pin Name	Description
DATA[1:8]	8-channel DSD data input
DATA_CLK	Bit clock for DSD data input

Table 4

FEATURE DESCRIPTION

Soft Mute

When Mute is asserted the output signal will ramp to the -∞ level. When Mute is reset the attenuation level will ramp back up to the previous level set by the volume control register. Asserting Mute will not change the value of the volume control register. The ramp rate is 0.0078125*FS dB/s, where FS = DATA_CLK/64 in PCM serial or DSD modes, or SPDIF sampling rate in SPDIF mode.

Automute Loopback

During an automute condition the external automute pin will always be asserted, however the ramping of the volume of each DAC DAC to -∞ can now be programmatically enabled or disabled.

Zero Detect

The use of the zero detect function to drive an external mute circuit is not required, but is recommended for designs that need the absolute maximum signal-to-noise ratios on an idle channel.

- In PCM serial mode, the Zero Detect output pin "AUTOMUTE" will become active once the audio data is continuously below the threshold set by <Register Automute_lev>, for a length of time defined by 2096896/(<Register#9>*DATA_CLK) Seconds.
- In SPDIF mode, the Zero Detect output pin "AUTOMUTE" will become active once the audio data is continuously below the threshold set by <Register Automute_lev>, for a length of time defined by 2096896/(<Register#9>*(64*FS) Seconds, where FS is the SPDIF sampling rate.
- In the DSD Mode, the Zero Detect output pin "AUTOMUTE" will become active when any 8 consecutive values in the DSD stream have as many 1's and 0's for a length of time defined by 2096896/(<Register Automute_time>*DATA_CLK) Seconds. The following table summarizes the conditions.

Mode	Detection Condition	Time
PCM	Data is continuously lower than <Register Automute_lev >	2096896/(<Register Automute_time >*DATA_CLK)
SPDIF	Data is continuously lower than <Register Automute_lev >	2096896/(<Register Automute_time >*(64*FS)) where FS is the SPDIF sampling rate
DSD	Equal number of 1s and 0s in every 8 bits of data	2096896/(<Register Automute_time >*DATA_CLK)

Table5

Volume Control

Each output channel has its own attenuation circuit. The attenuation for each channel is controlled independently. Each channel can be attenuated from 0dB to –127dB in 0.5dB steps.
Each 0.5dB step transition takes 64 intermediate levels. The result being that the level changes are done using small enough steps so that no switching noise occurs during the transition of the volume control. When a new volume level is set, the attenuation circuit will ramp softly to the new level.

Master Trim

The master trim sets the 0dB reference level for the volume control of each DAC. The master trim is programmable via registers 20-23 and is a 32bit signed number. Therefore it should never exceed 32'h7FFFFFFF (as this is full-scale signed).

All Mono Mode

The SABRE32can be put into an all mono mode where all eight DACs are driven from the same source. This can be useful for high-end audio applications. The source data for all eight DACs can be programmatically configured to be either PCM CH1 or CH2.

De-emphasis

The de-emphasis feature is included for audio data that has utilized the 50/15uS pre-emphasis for noise reduction. There are 3 de-emphasis filters, one for 32 kHz, 44.1 kHz and 48 kHz.

The de-emphasis filter can automatically be applied when an SPDIF stream sets the de-emphasis flag. It will auto detect the sample rate (32k, 44.1k, 48k) in either consumer or professional formats and then apply the correct de-emphasis filter. The automatic enabling of the de-emphasis filter can be disabled in Register 17 <en_auto>.

OSF Bypass

The oversampling FIR filter can be bypassed, sourcing data directly into the IIR filter. ESS recommends using 8*Fs as the input. For example, an external signal at 44.1kHz can be oversampled externally to 8*44.1kHz = 352.8kHz and then applied to the serial decoder in either I2S, LJ or RJ format. The maximum sample rate that can be applied is 1.536MHz (8*192kHz).

SPDIF Data Select

An SPDIF source multiplexer allows for up to eight SPDIF sources to be connected to the data pins on the ***SABRE^{32} Reference***. The ***SABRE^{32} Reference*** uses an internal programmable register to select the appropriate data pin to decode.

SPDIF input can be automatically decoded when there is valid SPDIF data if Register 17 <spdif_autodetect> is enabled.

Programmable Filter

The FIR filter can be programmed with custom coefficients to achieve an arbitrary frequency response that suits the needs of the product. The two stage interpolated filter exploits the symmetry of the coefficients to achieve a very sharp frequency response while using only 64 coefficients for the stage one filter and 14 coefficients for the stage two filter. Custom coefficients can be enabled via register 37 <prog_coeff_enabled> and can be programmed via the method explained in the FIR Programmable Filters section.

The length of the stage 2 filter is configurable to either 27 or 28 coefficients via register 17 <fir_length>.

System Clock (XI / MCLK)

A system clock is required for proper operation of the digital filters and modulation circuitry. Maximum clock frequency is 100MHz. The system clock must also satisfy:

Data Type	Valid MCLK Frequencies
DSD Data	100MHz > MCLK > 3*Fs , Fs = 2.8224MHz
Serial Normal Mode	100MHz > MCLK > 192*Fs
Serial OSF Bypass Mode	100MHz > MCLK > 24*Fs
SPDIF Data	100MHz > MCLK > 386*Fs

Data Clock

DATA_CLOCK must be 64*Fs for SERIAL, Fs for DSD modes, and is not required for SPDIF mode. This pin should be pulled low if not used.

Built-in Digital Filters

There are numerous applications for a stereo DAC so for added flexibility; two digital filter settings are possible, sharp roll-off and a slow roll-off for PCM mode. For DSD mode, there are 4 available filters with cutoffs at 47kHz, 50kHz, 60kHz, and 70kHz.

Sample Rate Calculation

The DPLL number can be read back from the ***SABRE^{32} Reference***, allowing for calculation of the sample rate. The sample rate can be calculated using: F_{in} = DPLL_NUM * 2^{32} / $F_{crystal}$. F_{in} must be divided by 64 for I^2S data.

DAC-bar Phase

Each DAC-bar phase can be configured to be in phase with DAC. This allows for the outputs of the DAC to be summed to drive an amplifier.

DPLL Lock Reset

The DPLL can be forced to relock, which is useful when the sample rate has been changed. This can be done by setting Register 17 <dpll_lock_rst_reg> high to force the reset, and then low to resume normal operation.

DPLL Frequency Phase Flip

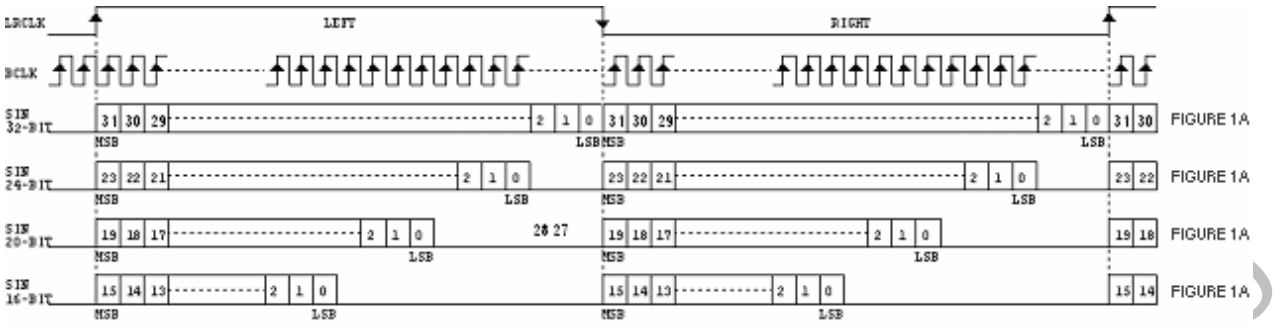
The DPLL can be set to lock to either the rising or falling edge of the clock. This can be set using Register 17 <fin_phase_flip>.

PCM Audio Interface Formats

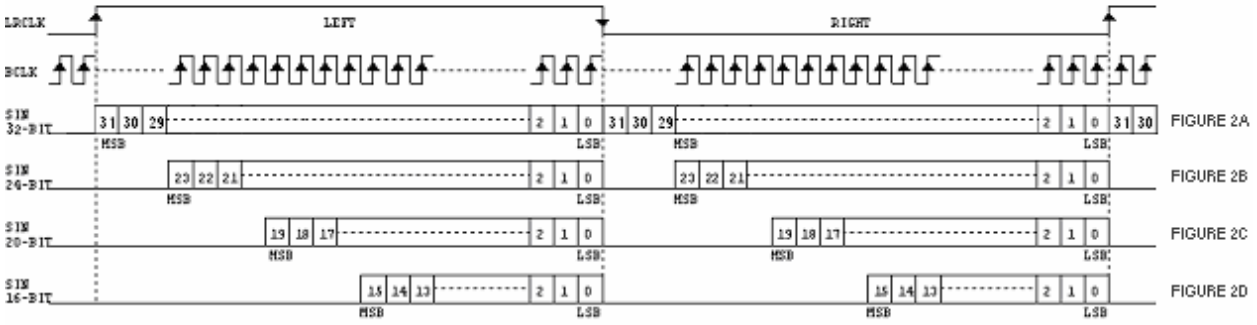
Several interface formats are provided so that direct connection to common audio processors is possible. The available formats and their accompanying diagrams are listed in the following table. The audio interface format can be set by programming the registers.

Format	Description	Figure
0	MSB First, Left Justified, up to 32-bit data	1A
1	I2S, up to 32-bit data	3A
2	MSB First, Right Justified, 32-bit data	2A
3	MSB First, Right Justified, 24-bit data	2B
4	MSB First, Right Justified, 20-bit data	2C
5	MSB First, Right Justified, 16-bit data	2D
6	DSD Normal Mode	4A
7	DSD Phase Mode	4B

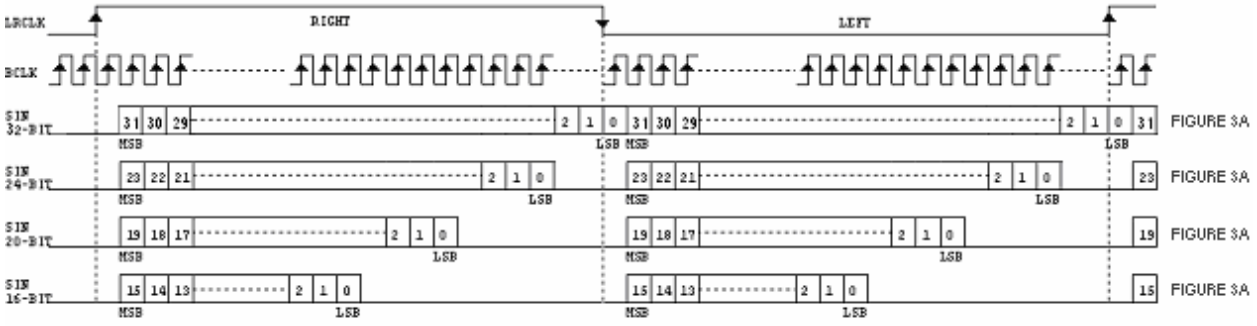
Table 6



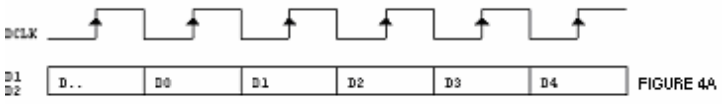
LEFT JUSTIFIED FORMAT



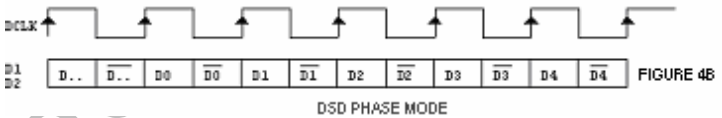
RIGHT JUSTIFIED FORMAT



I2S FORMAT



DSD NORMAL MODE



DSD PHASE MODE

SERIAL CONTROL INTERFACE

The registers inside the chip are programmed via an I2C interface. The diagram below shows the timing for this interface. The chip address can be set to 2 different settings via the "ADDR" pin. The table below summarizes this.

ADDR	CHIP ADDRESS
0	0x90
1	0x92

Table 7

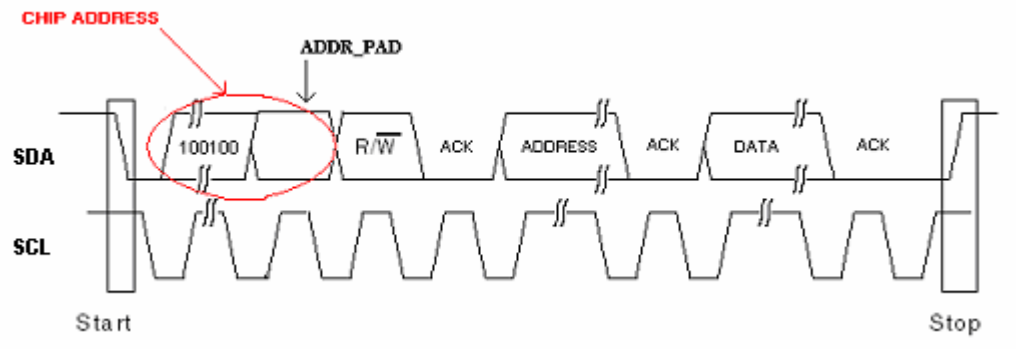


Diagram 1

Notes:

1. The "ADDR" pin is used to create the CHIP ADDRESS. (0x90, 0x92)
2. The first byte after the chip address is the "ADDRESS" this is the register address.
3. The second byte after the CHIP ADDRESS is the "DATA" this is the data to be programmed into the register at the previous "ADDRESS".

REGISTER SETTINGS

Register #0: Volume of DAC0 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #1: Volume of DAC1 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #2: Volume of DAC2 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #3: Volume of DAC3 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #4: Volume of DAC4 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #5: Volume of DAC5 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #6: Volume of DAC6 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #7: Volume of DAC7 **(default = 8'd0)**
Volume in dB's = -REG_VALUE/2

Register #8: Automute_lev **(default = 1'b0,7'd104)**
[7] : SPDIF_ENABLE.
- 1'b0 = Use either I2S or DSD input
- 1'b1 = Use SPDIF input

[6:0] : Automute trigger point in dB's = -REG_VALUE

Register #9: Automute_time **(default = 8'd4)**
Larger REG_VALUE = less time.
Smaller REG_VAULE = longer time.
Time in Seconds = 2096896/(REG_VALUE*DATA_CLK).

Register #10: Mode Control 1 **(default = 8'b11001110)**
[7:6] : 24/20/16 Bit for Serial Data Modes.
- 2'b00 = 24Bit
- 2'b01 = 20Bit
- 2'b10 = 16Bit
- 2'b11 = 32Bit

[5:4] : LJ/I2S/RJ Serial Data Modes.
- 2'b00 = I2S
- 2'b01 = LJ
- 2'b10 = RJ
- 2'b11 = I2S

[3] : RESERVED
- o Must be set to 1'b1 for normal operation.

[2] : JITTER_REDUCTION_ENABLE.

1'b0 = Bypass and stop JITTER_REDUCTION.
1'b1 = Use JITTER_REDUCTION.

[1] : BYPASS_DEEMPHASIS FILTER
1'b0 = Use De-emphasize Filter
1'b1 = Bypass De-emphasize Filter

[0] : MUTE DAC'S
1'b0 = Unmute All DAC's
1'b1 = Mute All DAC's

Register #11: Mode Control 2 (default = 8'b10000101)

[7] : RESERVED (must be set to 1'b1 for normal operation).
- Must be set to 1'b1 for normal operation.

[6:5] : RESERVED.
[4:2] : DPLL BANDWIDTH
3'b000 => No Bandwidth
3'b001 => Lowest Bandwidth
3'b010 => Low Bandwidth
3'b011 => Med-Low Bandwidth
3'b100 => Medium Bandwidth
3'b101 => Med-High Bandwidth
3'b110 => High Bandwidth
3'b111 => Highest Bandwidth
[1:0] : DE-EMPHASIS DELECT
2'b00 = 32kHz
2'b01 = 44.1kHz
2'b10 = 48kHz
2'b11 = RESERVED

Register #12: Mode Control 3 (default = 8'b00100000)

[7:0] : RESERVED
- Must be set to 8'b00100000 for normal operation.

Register #13: DAC Polarity (default = 8'b00000000)

[7] : POLARITY OF DAC8
1'b0 = In-Phase
1'b1 = Anti-Phase
[6] : POLARITY OF DAC7
1'b0 = In-Phase
1'b1 = Anti-Phase
[5] : POLARITY OF DAC6
1'b0 = In-Phase
1'b1 = Anti-Phase
[4] : POLARITY OF DAC5
1'b0 = In-Phase
1'b1 = Anti-Phase
[3] : POLARITY OF DAC4
1'b0 = In-Phase
1'b1 = Anti-Phase
[2] : POLARITY OF DAC3
1'b0 = In-Phase
1'b1 = Anti-Phase
[1] : POLARITY OF DAC2
1'b0 = In-Phase

1'b1 = Anti-Phase
[0] : POLARITY OF DAC1
1'b0 = In-Phase
1'b1 = Anti-Phase

Register #14: DAC3/4/7/8 Source IIR Bandwidth, FIR Rolloff (default = 8'b00001011)

[7] : SOURCE OF DAC8
1'b0 = DAC8
1'b1 = DAC6
[6] : SOURCE OF DAC7
1'b0 = DAC7
1'b1 = DAC5
[5] : SOURCE OF DAC4
1'b0 = DAC4
1'b1 = DAC2
[4] : SOURCE OF DAC3
1'b0 = DAC3
1'b1 = DAC1
[3] : RESERVED
- Must be set to 1'b1 for normal operation.

[2:1] : IIR BANDWIDTH
1'd0 = Normal (for least in-band ripple for PCM data set to Normal)
1'd1 = 50k
1'd2 = 60k
1'd3 = 70k
[0] : FIR ROLLOFF SPEED
1'b0 = Slow Rolloff
1'b1 = Fast Rolloff

Register #15: Mode Control 4 (default = 8'b00000000)

[7:0] : RESERVED
- Must be set to 8'b00000000 for normal operation.

Register #16: Automute Loopback (default = 8'b00000000)

[7:4] RESERVED
[3] automute_loopback
1'b1 => Ramp volume to -infinity upon automute condition.
1'b0 => Do not ramp volume down upon automute condition.
[2:0] RESERVED

Register #17: Mode Control 5 (default = 8'b00011100)

[7] mono_ch_select
1'b1 => Use the right channel when all_mono mode is enabled.
1'b0 => Use the left channel when all_mono mode is enabled.
[6] OSF_bypass
1'b1 => Send data directly from the I2S receiver to the IIR filter at 8x. This will cause the signal to bypass the FIR filters as well as the deemphasis filter, but will still apply the volume controls.
1'b0 => Use the OSF filter (normal operation).
[5] dpll_lock_rst_reg
1'b1 => Manually override the dpll_lock.
This will force the Jitter Eliminator to relock to the signal.
1'b0 => Normal operation
[4] auto_deemph
1'b1 => Deemphasis in SPDIF mode is automatically applied with the correct frequency

if 44.1k/48k/32k are detected in the SPDIF channel status bits.
0'b1 => Deemphasis filter is not automatically applied.

[3] spdif_autodetect
1'b1 => Automatically detect SPDIF input.
1'b0 => Must manually select SPDIF input.
Note: This should only be set if I2S data will not be applied to the pins.

[2] Fir_length
1'b1 => 2nd stage FIR filter is 28 coefficients in length.
1'b0 => 2nd stage FIR filter is 27 coefficients in length.

[1] fin_phase_flip
1'b1 => Invert the phase to the DPLL.
1'b0 => Do not invert the phase to the DPLL.

[0] all_mono
1'b1 => All 8 DAC's are sourced from one source for true mono.
The channel to use as the source is selected by te mono_ch_select register.
1'b0 => Normal 8 channel mode.

Register #18: SPDIF Source (default = 8'd1)

This registers chooses the SPDIF source. The ***SABRE^{32} Reference*** has an 8-to-1 multiplexer which allows up to 8 SPDIF inputs to be connected to the data pins.

8'd1 => data1
8'd2 => data2
8'd4 => data3
8'd8 => data4
8'd16 => data5
8'd32 => data6
8'd64 => data7
8'd128 => data8

Register #19: DACB Polarity (default = 8'b00000000)

[7] dac8B polarity
1'b1 => in-phase
1'b0 => anti-phase (normal operation)

[6] dac7B polarity
1'b1 => in-phase
1'b0 => anti-phase (normal operation)

[5] dac6B polarity
1'b1 => in-phase
1'b0 => anti-phase (normal operation)

[4] dac5B polarity
1'b1 => in-phase
1'b0 => anti-phase (normal operation)

[3] dac4B polarity
1'b1 => in-phase
1'b0 => anti-phase (normal operation)

[2] dac3B polarity
1'b1 => in-phase
1'b0 => anti-phase (normal operation)

[1] dac2B polarity
1'b1 => in-phase
1'b0 => anti-phase (normal operation)

[0] dac1B polarity
1'b1 => in-phase
1'b0 => anti-phase (normal operation)

Registers #23-20: Master Trim (default = 32'h7fffffff)

This is a 32 bit value that sets the 0dB level for all volume controls. This is a signed number, so it should never exceed 32'h7fffffff (which is 2^{31} - 1). (Reg 23 are the MSB's, Reg 20 are the LSB's)

Register 24: Phase Shift (default = 8'b00110000)

[7:4] RESERVED
[3:0] phase_shift
4'd0 => default
4'd1 => default + 1/clk delay
4'd2 => default + 2/clk delay
4'd3 => default + 3/clk delay
4'd4 => default + 4/clk delay
4'd5 => default + 5/clk delay
4'd6 => default + 6/clk delay
4'd7 => default + 7/clk delay
4'd8 => default + 8/clk delay
4'd9 => default + 9/clk delay
4'd10 => default + 10/clk delay
4'd11 => default + 11/clk delay
4'd12 => default + 12/clk delay
4'd13 => default + 13/clk delay
4'd14 => default + 14/clk delay
4'd15 => default + 15/clk delay

Register 25: DPLL Mode Control (default = 8'b00000010)

[7:2] RESERVED
[1] dpll_bw_defaults
1'b1 => Use the best DPLL bandwidth settings.
1'b0 => Allow all settings.
[0] dpll_bw_128x
1'b1 => Multiply the DPLL BANDWIDTH setting by 128.
1'b0 => Use the DPLL BANDWIDTH setting.

Register 27: Status

This is a read-only register. All of these values are set by internal logic on the chip.
[7:4] RESERVED
[3] dsd_pcm
1'b1 => DSD mode.
1'b0 => I2S or SPDIF mode.
[2] spdif_valid
1'b1 => The SPDIF data is valid.
1'b0 => The SPDIF data is invalid.
[1] spdif_en
1'b1 => SPDIF mode is currently enabled. This can be done manually by setting spdif_en_r (Register 8) or by having spdif_autodetect enabled with valid SPDIF data on the input.
1'b0 => SPDIF mode is currently disabled.
[0] lock
1'b1 => The Jitter Eliminator is locked to an incoming signal.
1'b0 => The Jitter Eliminator is not locked to an incoming signal.

Register 31-28: DPLL_NUM

This is a read-only 32bit value that can be used to calculate the sample rate. The sample rate can be calculated using: F_{in} = DPLL_NUM * 2^{32} / $F_{crystal}$. F_{in} must be divided by 64 for I^2S data. Reg 31 are the MSB's, Reg 28 are the LSB's

Register #37 (default = 8'b00000000)

[7:6] RESERVED
[5] stage1_prog_coeff_enabled
1'b1 => The stage 1 interpolating FIR filter will use the downloaded (custom) coefficients.
1'b0 => The stage 1 interpolating FIR filter will use the built-in coefficients.
[4] stage1_programming_enabled
1'b1 => The stage 1 coefficients are set for writing. This bit must be enabled prior to programming the stage 1 FIR coefficients.
1'b0 => The stage 1 coefficients are not set for writing.
[3:2] RESERVED
[1] stage2_prog_coeff_enabled
1'b1 => The stage 2 FIR filter will use the downloaded (custom) coefficients.
1'b0 => The stage 2 FIR filter will use the built-in coefficients.
[0] stage2_programming_enabled |
1'b1 => The stage 2 coefficients are set for writing. This bit must be enabled prior to programming the stage 2 FIR coefficients.
1'b0 => The stage 2 coefficients are not set for writing.

Register #41-38: Stage 1 FIR Coefficients

These 32 bits are used for writing the stage 1 FIR coefficients. See the programming section for more information. Reg 41 are the MSB's, Reg 38 are the LSB's

Register #45-42: Stage 2 FIR Coefficients

These 32 bits are used for writing the stage 2 FIR coefficients. See the programming section for more information. Reg 45 are the MSB's, Reg 42 are the LSB's

Register #71-48: SPDIF Channel Status Data

These registers allow read back of the SPDIF channel status. The status definition is different for the consumer configuration (Table 7) and professional configuration (Table 8)
Reg 71 are the MSB's, Reg 48 are the LSB's Format is [191:0]

SPDIF CHANNEL STATUS - Consumer configuration (Base Address = 48)								
Address Offset	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	Reserved	Reserved	0:2Channel 1:4Channel	Reserved	0:No-Preemph 1:Preemph	0:CopyRight 1:Non-CopyRight	0:Audio 1:Data	**0:Consumer** 1:Professional
1	Category Code 0x00: General 0x01:Laser-Optical 0x02:D/D Converter 0x03:Magnetic 0x04:Digital Broadcast 0x05:Musical Instrument 0x06:Present A/D Converter 0x08:Solid State Memory 0x16:Future A/D Converter 0x19:DVD 0x40:Experimental							
2	Channel Number 0x0:Don't Care 0x1:A (Left) 0x2:B (Right) 0x3:C 0x4:D 0x5:E 0x6:F 0x7:G 0x8:H 0x9:I 0xA:J 0xB:K 0xC:L 0xD:M 0xE:N 0xF:O				Source Number 0x0:Don't Care 0x1:1 0x2:2 0x3:3 0x4:4 0x5:5 0x6:6 0x7:G 0x8:8 0x9:9 0xA:10 0xB:11 0xC:12 0xD:13 0xE:14 0xF:15			
3	Reserved	Reserved	Clock Accuracy 0x0:Level 2 +-1000ppm 0x1:Level 1 +-50ppm 0x2:Level 3 variable pitch shifted		Sample Frequency 0x0:44.1k 0x2:48k 0x3:32k 0x4:22.05k 0x6:24k 0x8:88.2k 0xA:96k 0xC:176.4k 0xE:192k			
4	Reserved	Reserved	Reserved	Reserved	Word Length: If Word Field Size=0 |If Word Field Size = 1 000=Not indicated |000=Not indicated 100 = 23bits |100 = 19bits 010 = 22bits |010 = 18bits 110 = 21bits |110 = 17bits 001 = 20bits |001 = 16bits 101 = 24bits |101 = 20bits			Word Field Size 0:Max 20bits 1:Max 24bits
5-23	Reserved							

Table 7

SPDIF CHANNEL STATUS - Professional configuration (Base Address = 48)								
Address Offset	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	sampling frequency: 00: not indicated (or see byte 4) 10: 48 kHz 01: 44.1 kHz 11: 32 kHz		lock: 0: locked 1: unlocked	emphasis: 000: Emphasis not indicated 001: No emphasis 011: CD-type emphasis 111: J-17 emphasis			0:Audio 1:Non-audio	0:Consumer **1:Professional**
1	User bit management: 0000: no indication 1000: 192-bit block as channel status 0100: As defined in AES18 1100: user-defined 0010: As in IEC60958-3 (consumer)					Channel mode: 0000: not indicated (default to 2 ch) 1000: 2 channel 0100: 1 channel (monophonic) 1100: primary / secondary 0010: stereo 1010: reserved for user applications 0110: reserved for user applications 1110: SCDSR (see byte 3 for ID) 0001: SCDSR (stereo left) 1001: SCDSR (stereo right) 1111: Multichannel (see byte 3 for ID)		
2	alignment level: 00: not indicated 10: –20 dB FS 01: –18.06 dB FS		Source Word Length: If max=20bits |If max=24bits 000=Not indicated |000=Not indicated 100 = 23bits |100 = 19bits 010 = 22bits |010 = 18bits 110 = 21bits |110 = 17bits 001 = 20bits |001 = 16bits 101 = 24bits |101 = 20bits			Use of aux sample word: 000: not defined, audio max 20 bits 100: used for main audio, max 24 bits 010: used for coord, audio max 20 bits 110: reserved		
3	Channel identification: if bit 7 = 0 then channel number is 1 plus the numeric value of bits 0-6 (bit reversed). if bit 7 = 1 then bits 4–6 define a multichannel mode and bits 0–3 (bit reversed) give the channel number within that mode.							
4	fs scaling: 0: no scaling 1: apply factor of 1 / 1.001 to value		Sample frequency (fs): 0000: not indicated 0001: 24 kHz 0010: 96 kHz 1001: 22.05 kHz 1010: 88.2 kHz 1011: 176.4 kHz 0011: 192 kHz 1111: User defined			Reserved	DARS (Digital audio reference signal): 00: not a DARS 01: DARS grade 2 (+ / –10 ppm) 10: DARS grade 1 (+ / –1 ppm) 11: Reserved	
5	Reserved							
6-9	alphanumerical channel origin: four-character label using 7-bit ASCII with no parity. Bits 55, 63, 71, 79 = 0.							
10-13	alphanumerical channel destination: four-character label using 7-bit ASCII with no parity. Bits 87, 95, 103, 111 = 0.							
14-17	local sample address code: 32-bit binary number representing the sample count of the first sample of the channel status block.							
18-21	time of day code: 32-bit binary number representing time of source encoding in samples since midnight							
22	reliability flags 0: data in byte range is reliable 1: data in byte range is unreliable							
23	CRCC 00000000: not implemented X: error check code for bits 0–183							

Table 8

FIR PROGRAMMABLE FILTERS

The ***SABRE[32] Reference*** has a two stage interpolating filter with both built-in and programmable coefficients. Each stage can be programmed and enabled independently. Each channel can also have a different filter per stage.

Each stage of the FIR filter either uses the built-in coefficients, or the programmable coefficients. Register 37 bits 5 and 1 are used for setting the filter coefficient sources.

Programming the filter requires passing every coefficient for all 8 channels to the ***SABRE[32] Reference*** via I2C. Stage 1 and Stage 2 must be programmed independently. Programming starts by enabling the appropriate enable_programming bit in register 37.

To program stage 1, bit 4 of register 37 must be set high. Then the 32bit coefficients are written to registers 41 (Bits [31:24]), 40 (Bits[23:16]), 39 (Bits[15:8]), 38 (Bits[7:0]) in that order. The first write to these 4 consecutive register is the 32-bit value for Channel1, coefficient1. The next write to these 4 consecutive registers is the 32-bit value for Channel2, coefficient1. After 8 writes to these 4 consecutive registers, coefficient 2 for all 8 filters is ready to be input. There are 64 coefficients to write for Stage 1. So that is 4 bytes per coefficient, 8 channels and 64 coefficients for a total of 2048 bytes to program the stage 1. Once complete, zero must be written to register 38. Bit 4 of register 37 must then be set low to finalize the programming.

To program stage 2, bit 0 of register 37 must be set high. Then the 32bit coefficients are written to registers 45 (Bits [31:24]), 44 (Bits [23:16]), 43 (Bits [15:8]), 42 (Bits [7:0]), in that order. The first write to these 4 consecutive register is the 32-bit value for Channel1, coefficient1. The next write to these 4 consecutive registers is the 32-bit value for Channel2, coefficient1. After 8 writes to these 4 consecutive registers, coefficient 2 for all 8 filters is ready to be input. There are 16 coefficients to write for Stage 2. So that is 4 bytes per coefficient, 8 channels and 16 coefficients for a total of 512 bytes to program the stage 1. Once complete, zero must be written to register 42. Bit 0 of register 37 must then be set low to finalize the programming.

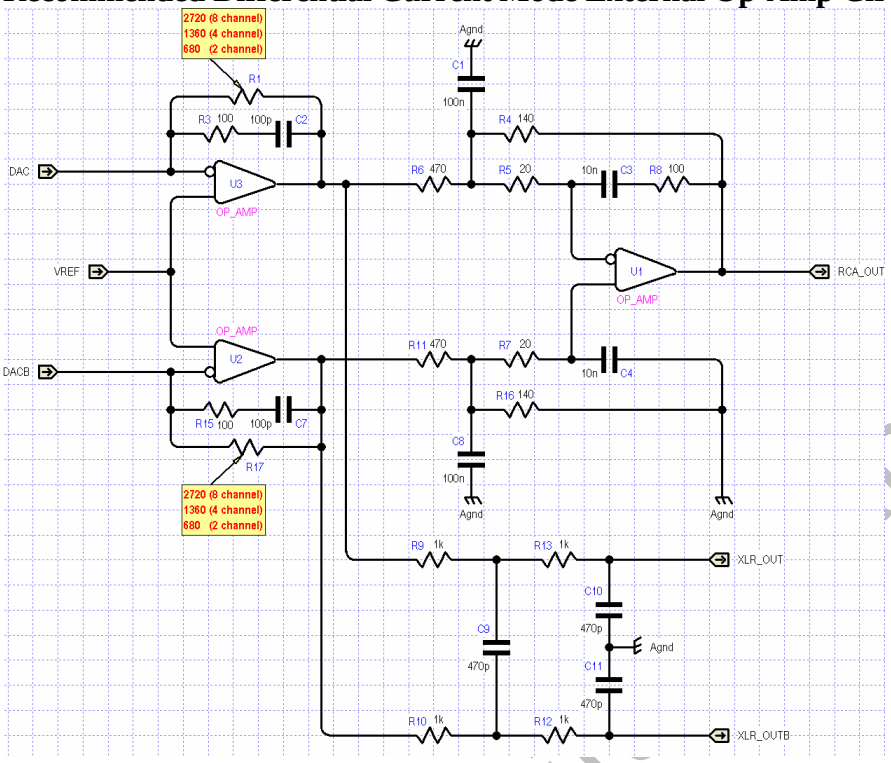
C++ Sample Code for writing custom coefficients to either stage.

```
void CLoadCoeffDlg::ProgramStage(int nStage)
{
	BYTE WE;
	BYTE WritePort[4];
	BYTE WriteData[4];
	int nTotal;
	if(nStage==0){			//programming stage 1
		WE=0x10;
		WritePort[0]=41;
		WritePort[1]=40;
		WritePort[2]=39;
		WritePort[3]=38;
		nTotal=64;
	}
	else{				//programming stage 2
		WE=0x01;
		WritePort[0]=45;
		WritePort[1]=44;
		WritePort[2]=43;
		WritePort[3]=42;
		nTotal=16;
```

```
	}
	if(!m_pParent->WriteRegisters(1, 37, &WE))
		return;
	for(int nCIndex=0; nCIndex<nTotal; nCIndex++){
		for(int nCh=0; nCh<8; nCh++){
			DWORD nCoeff;
			if(nStage==0)
				nCoeff=CoeffCh[nCh].CoeffStage1[nCIndex];
			else
				nCoeff=CoeffCh[nCh].CoeffStage2[nCIndex];
			WriteData[0]=(BYTE)(nCoeff>>24)&0xff;
			WriteData[1]=(BYTE)((nCoeff>>16)&0xff);
			WriteData[2]=(BYTE)((nCoeff>>8)&0xff);
			WriteData[3]=(BYTE)((nCoeff)&0xff);
			if(!m_pParent->WriteRegisters(4, WritePort, WriteData))
				return;
		}
	}
	WE=0x00;
	if(nStage == 0) WriteRegisters(1, 38, &WE);
	else if(nStage == 1) WriteRegisters(1, 42, &WE);
	if(!m_pParent->WriteRegisters(1, 37, &WE));
}
```

APPLICATION DIAGRAMS

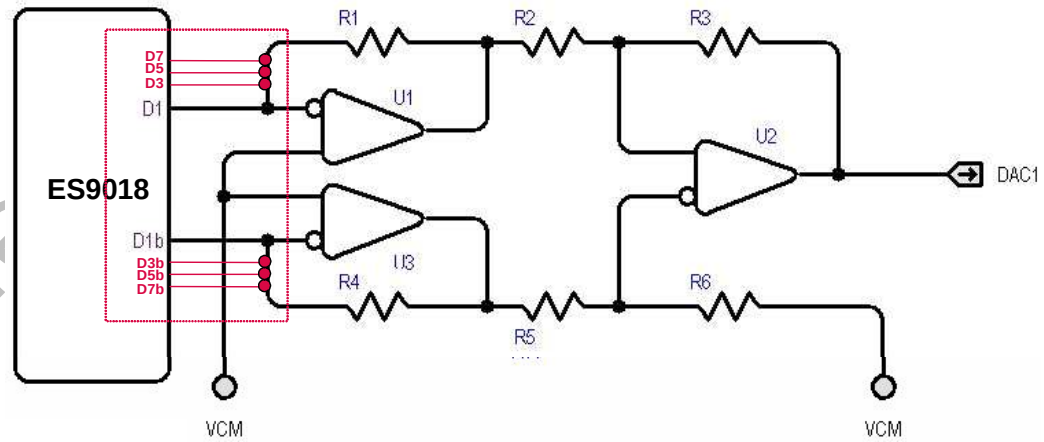
Recommended Differential Current Mode External Op-Amp Circuit



ES9018 Stereo Quad-differential Current Mode

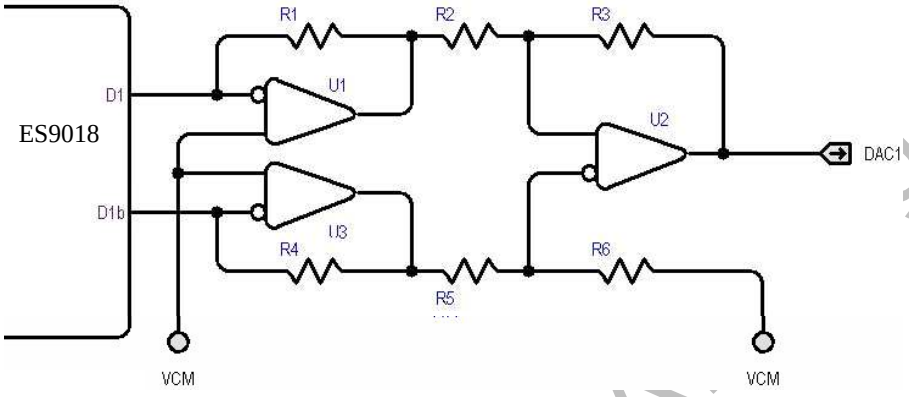
Sabre^{32} Reference in stereo "quad -differential" current mode

(DNR: 133dB, THD: -120dB)



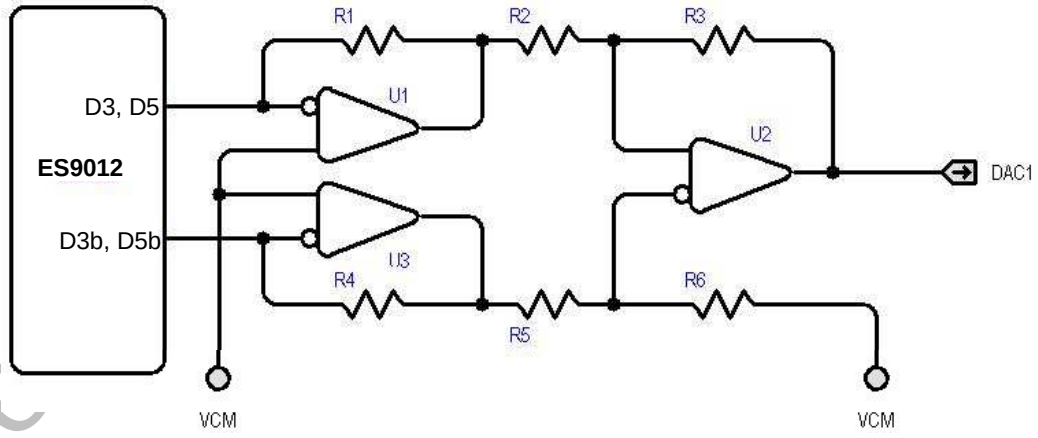
ES9018 8-channel Differential Current Mode

Sabre[32] Reference in 8-channel differential current mode
(DNR: 129dB, THD: -120dB)



ES9012 Stereo Mode

(DNR: 133dB, THD: -120dB)



ABSOLUTE MAXIMUM RATINGS

PAREMETER	RATING
Storage temperature	-65°C to 105°C
Voltage range for 5V tolerant pins	-0.5V to +5.5V
Voltage range for all other pins	-0.5V to (DVCC_T+0.5V) or -0.5V to (DVCC_B+0.5V)

WARNING: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

RECOMMENDED OPERATING CONDITIONS

PAREMETER	SYMBOL	CONDITIONS
Operating temperature	T_A	0°C to 70°C
Digital core supply voltage	VDD	1.2V ± 5%, 37mA nominal (*1)
Digital power supply voltage	DVCC_T, DVCC_B	3.3V ± 5%, 7mA nominal (*1)
Analog power supply voltage	AVCC_L, AVCC_R	3.3V ± 5%, 25mA nominal (*1)

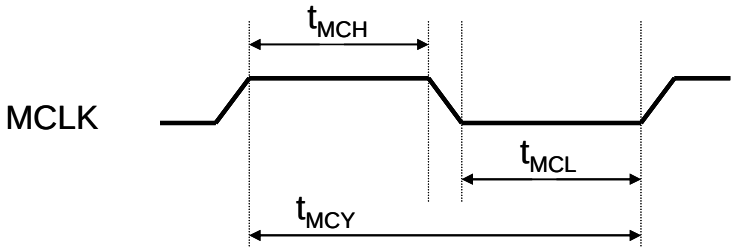
Note

(*1) fs =48kHz, MCLK=40MHz, I2S input, output unloaded

DC ELECTRICAL CHARACTERISTICS

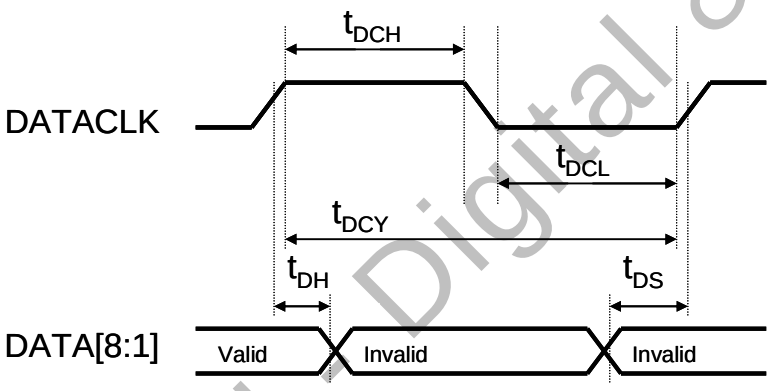
SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
V_{IH}	High-level input voltage	2.0	DVCC_T or DVCC_B	V	All inputs TTL levels except CLK and 5V tolerant input pins
		2.0	5.5	V	All 5V tolerant inputs
V_{IL}	Low-level input voltage	-0.3	0.8	V	All input TTL levels except CLK
V_{CLKH}	CLK high-level input	2.0	DVCC_B+0.25	V	TTL level input
V_{CLKL}	CLK low-level input	-0.3	0.8	V	
V_{OH}	High-level output voltage	3.0		V	I_{OH} = 1mA
V_{OL}	Low-level-output voltage		0.45	V	I_{OL} = 4mA
I_{LI}	Input leakage current		±15	µA	
I_{LO}	Output leakage current		±15		
C_{IN}	Input capacitance		10	pF	fc = 1MHz
C_O	Input/output capacitance		12		
C_{CLK}	CLK capacitance		20	pF	fc = 1MHz

MCLK Timing



Parameter	Symbol	Min	Max	Unit
MCLK pulse width high	T_{MCH}	4.5		ns
MCLK pulse width low	T_{MCL}	4.5		ns
MCLK cycle time	T_{MCY}	10		ns
MCLK duty cycle		45:55	55:45	

Audio Interface Timing



Parameter	Symbol	Min	Max	Unit
DATA_CLK pulse width high	t_{DCH}	4.5		ns
DATA_CLK pulse width low	t_{DCL}	4.5		ns
DATA_CLK cycle time	t_{DCY}	10		ns
DATA_CLK duty cycle		45:55	55:45	
DATA set-up time to DATA_CLK rising edge	t_{DS}	2		ns
DATA hold time to DATA_CLK rising edge	t_{DH}	2		ns

ANALOG PERFORMANCE

Test Conditions (unless otherwise stated)

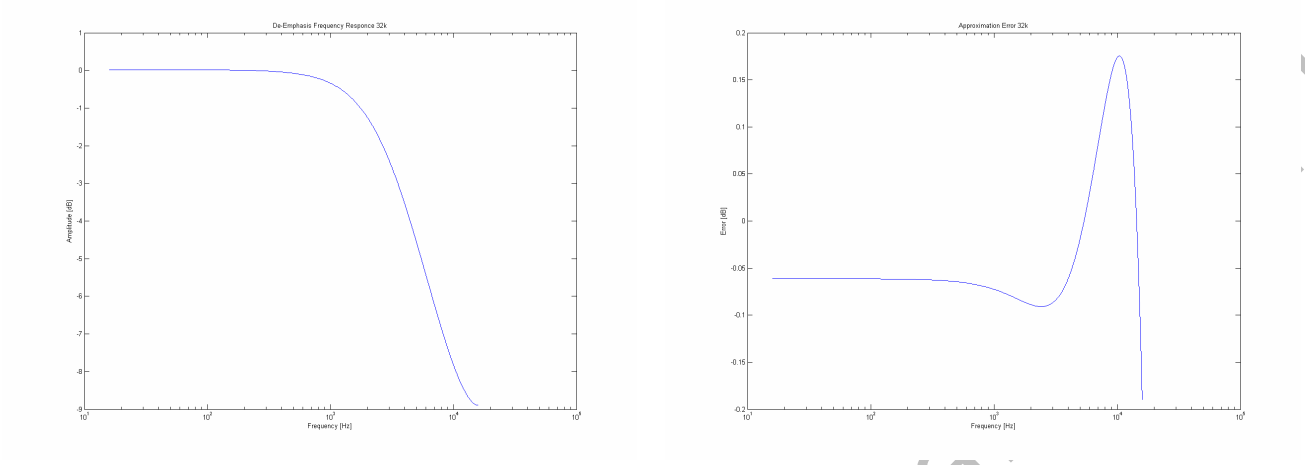
1. T_A=25°C, AVCC=3.3V, DVCC=1.2V, fs =44.1kHz, MCLK=27Mhz and 32-bit data
2. SNR/DNR: A-weighted over 20-20kHz in averaging mode
3. THD+N: un-weighted over 20-20kHz bandwidth

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				32		Bits
MCLK (PCM normal mode)				>192		fs
MCLK (PCM OSF bypass mode)				>24		fs
MCLK (DSD mode)				>3		fs
MCLK (SPDIF mode)				>386		fs
DYNAMIC PERFORMANCE						
DNR (mono differential current mode)		-60dBFS		135		dB-A
DNR (stereo differential current mode)		-60dBFS		133		dB-A
DNR (8-ch differential current mode)		-60dBFS		129		dB-A
DNR (8-ch differential voltage mode)		-60dBFS		120		dB-A
THD+N (differential current mode)		0dBFS		-120		dB
THD+N (differential voltage mode)		0dBFS		-108		dB
PCM sampling frequency (normal mode)					500	kHz
PCM sampling frequency (OSF bypass)					1.536	MHz
Level Linearity Error		-126dBFS		±0.3		dB
		-138dBFS		±1.0		dB
ANALOG OUTPUT						
Differential voltage output range		Full-scale out		3.05 (0.924*AVCC)		V pp
Differential voltage output offset		Bipolar zero out		1.65 (AVCC/2)		V
Differential current output range (Note *1)		Full-scale out		3.903		mA pp
Differential current output offset (Note *1)		Bipolar zero out to virtual ground at voltage Vg (V)		2.112 – 1000*Vg/781.25		mA
Digital Filter Performance						
De-emphasis error					±0.2	dB
Mute Attenuation				127		dB
PCM Filter Characteristics (Sharp Roll Off)						
Pass band		±0.003dB			0.454	fs
		-3dB			0.49	fs
Stop band		< -115dB	0.546			fs
Group Delay				35/fs		s
PCM Filter Characteristics (Slow Roll Off)						
Pass band		±0.05dB			0.308	fs
		-3dB			0.454	fs
Stop band		< -100dB	0.814			fs
Group Delay				6.25/fs		s
DSD Filter Characteristics						
Pass band		-3dB		50/60/70		kHz
Stop band attenuation				18		dB/oct

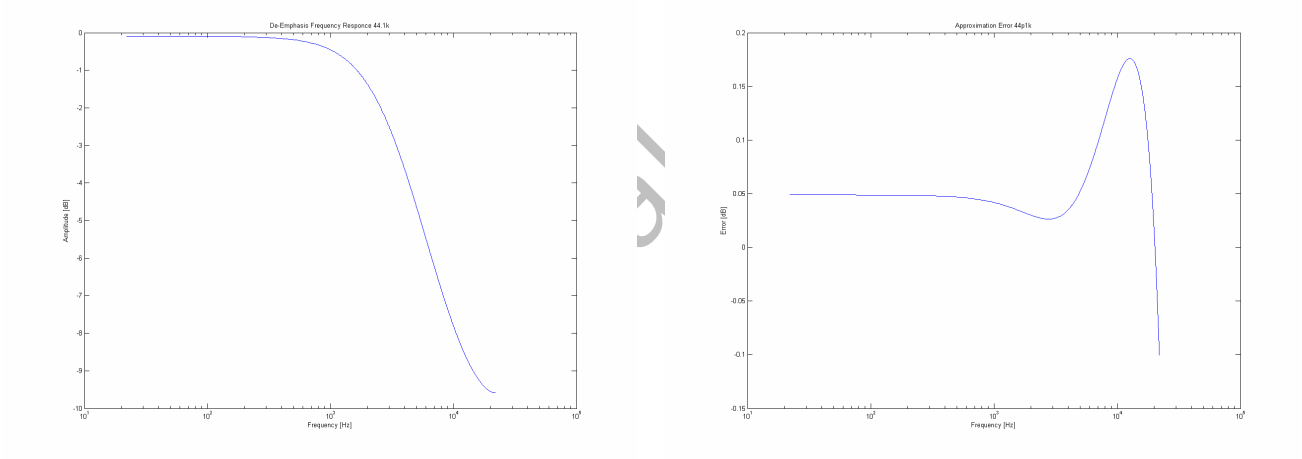
Note

*1. Differential current output is equivalent to a differential voltage source in series with a 781.25Ω resistor. The differential voltage source has a peak-to-peak output range of 3.05V (0.924*AVCC) and an output offset of 1.65V (AVCC/2).

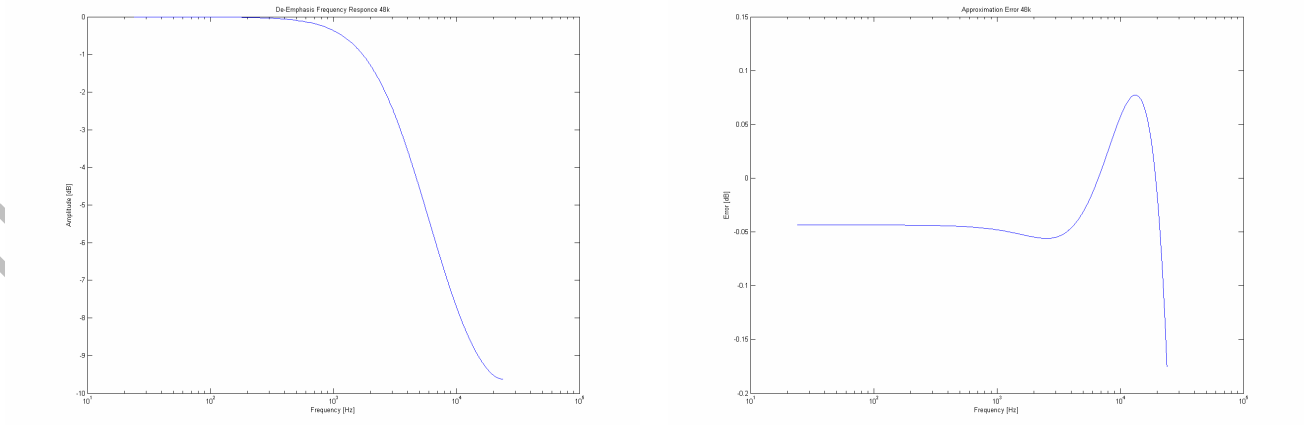
PCM DE-EMPHASIS FILTER RESPONSE (32kHz)



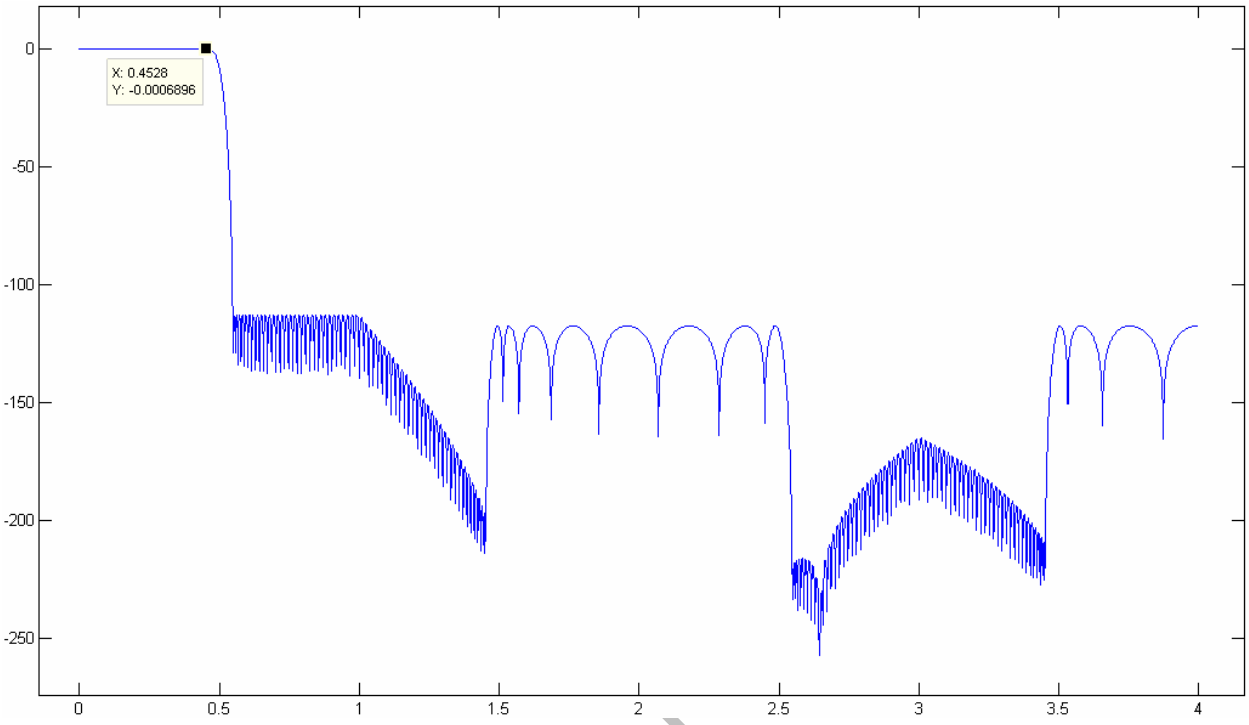
PCM DE-EMPHASIS FILTER RESPONSE (44.1kHz)



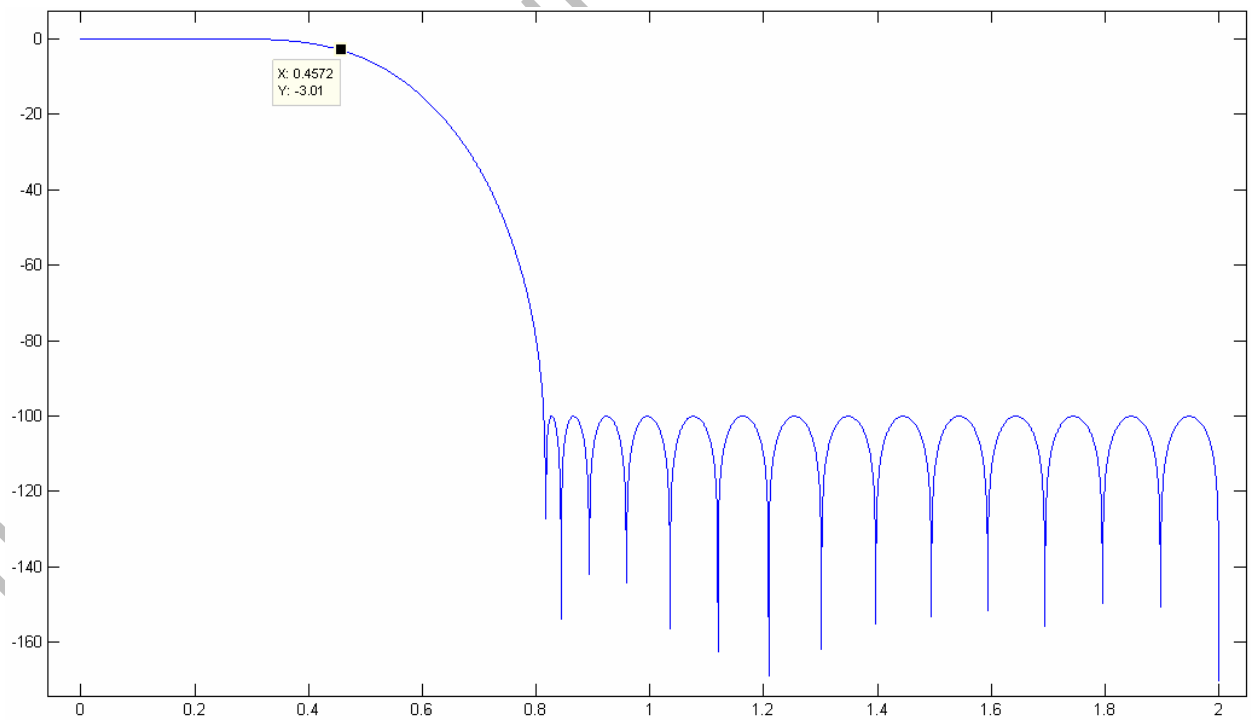
PCM DE-EMPHASIS FILTER RESPONSE (48kHz)



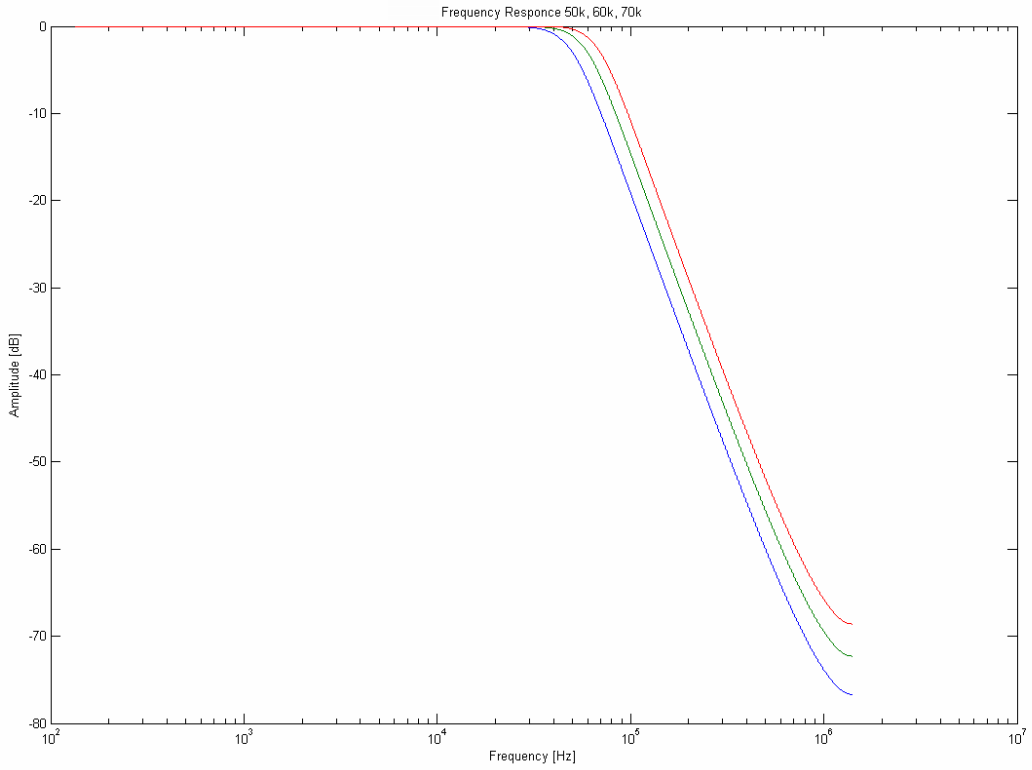
PCM SHARP ROLL-OFF FILTER RESPONSE



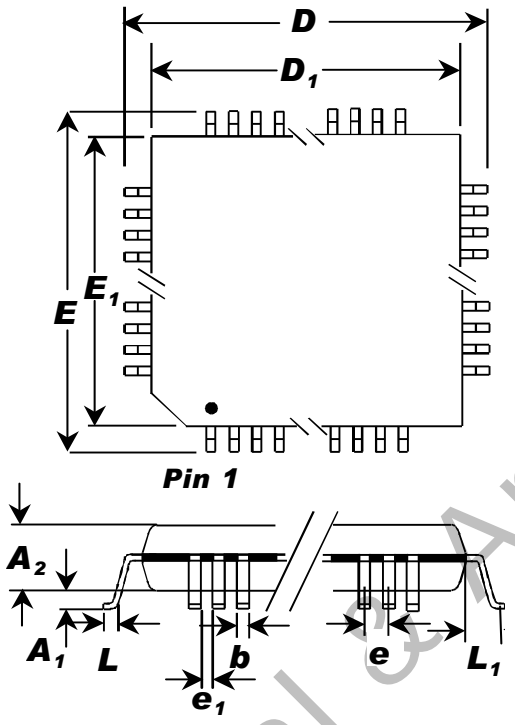
PCM SLOW ROLL-OFF FILTER RESPONSE



DSD FILTER RESPONSE



64 Pin LQFP Mechanical Dimensions



		MILLIMETERS		
Symbol	Description	Min.	Nom.	Max.
D	Lead-to Lead, X-axis	11.75	12.00	12.25
D1	Package's Outside, X-axis	9.90	10.00	10.10
E	Lead-to Lead, Y-axis	11.75	12.00	12.25
E1	Package's Outside, Y-axis	9.90	10.00	10.10
A1	Board Standoff	0.05	0.10	0.15
A2	Package Thickness	1.35	1.40	1.45
b	Lead Width	0.17	0.22	0.27
e	Lead Pitch		0.50 BSC	
e_1	Lead Gap	0.23	0.28	0.33
L	Foot Length	0.45	0.60	0.75
L1	Lead Length		1.00	
	Coplanarity			0.102
	Foot Angle	0º		7º
	No. of Leads in X-axis		16	
	No. of Leads in Y-axis		16	
	No. of Leads Total		64	
	Package Type		LQFP	

ORDERING INFORMATION

Part Number	Description	Package
ES9018S	Sabre^{32} Reference 8-channel Audio DAC	64-pin LQFP
ES9012S	Sabre^{32} Reference Stereo Audio DAC	64-pin LQFP

The letter S at the end of the part number identifies the package type LQFP.

Revision History

Revision	Date	Notes
Initial	January 21, 2009	Initial version
1.0	January 23, 2009	Update Register #15 default value Update Audio Interface Timing Update Level Linearity Error Performance Add details to FIR Programmable Filters and Registers sections
1.1	March 13, 2009	Add ES9012

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