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SAVITECH.COM

SA9127

DSD64 / DSD128 / DSD256
PCM 32Bit / 384KHz
USB Audio Streaming Controller

Datasheet v1.0

SAVITECH Corporation

SA9127
USB Audio Streaming Controller

Overview

The SA9127 is a USB High-Speed compliant audio steaming controller with support up to 32bit / 384KHz PCM and DSD64 / 128 / 256 . The SA9127 is ideal for both one stereo-in and one stereo-out professional digital audio interface applications. It s PCM resolution and sampling rate can be configurable with 16 / 24 / 32 bit and 32 / 44.1 / 48 / 88.2 / 96 / 176.4 / 192 / 352.8 / 384KHz respectively.

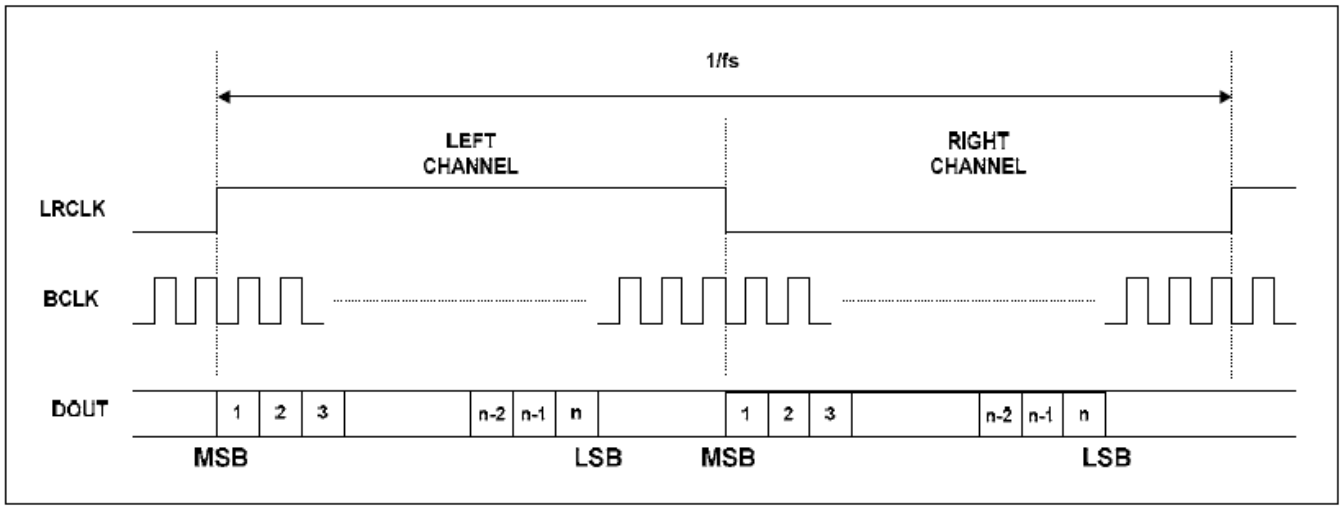
Features

- USB 2.0 High-Speed Compliant
- USB Audio Class v1.0 and v2.0 supported
- Isochronous output endpoints for playback
- One interrupt endpoint for HID
- One DSD interface for connect with external DSD DAC
- Support DSD64 / DSD128 / DSD256 of native and DSD64 / DSD128 of DoP in Async mode
- Support DSD L / R data line swap feature
- Support resolutions up to 32-bit and sampling rates up to 384KHz
- One I2S input pairs and one I2S output pairs for PCM
  - Independent sample rates for each pairs
  - 32 / 44.1 / 48 / 88.2 / 96 / 176.4 / 192 KHz recording sampling rates
  - 16 / 24 bit resolution for recording
  - 32 / 44.1 / 48 / 88.2 / 96 / 176.4 / 192 / 352.8 / 384KHz playback sampling rates
  - 16 / 24 / 32 bit resolution for playback
- Control and I/O
  - I2C bus
  - GPIOs
- 48-pin WQFN 6x6 package

Serial Audio Interfaces Formats

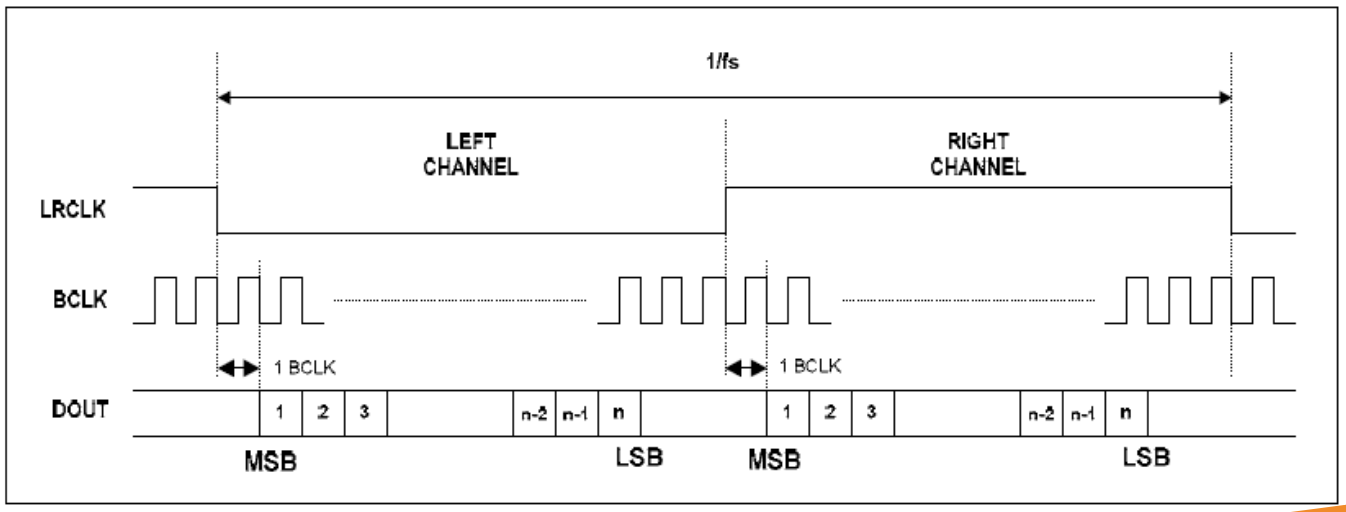
■ L-justified format:

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending the on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.



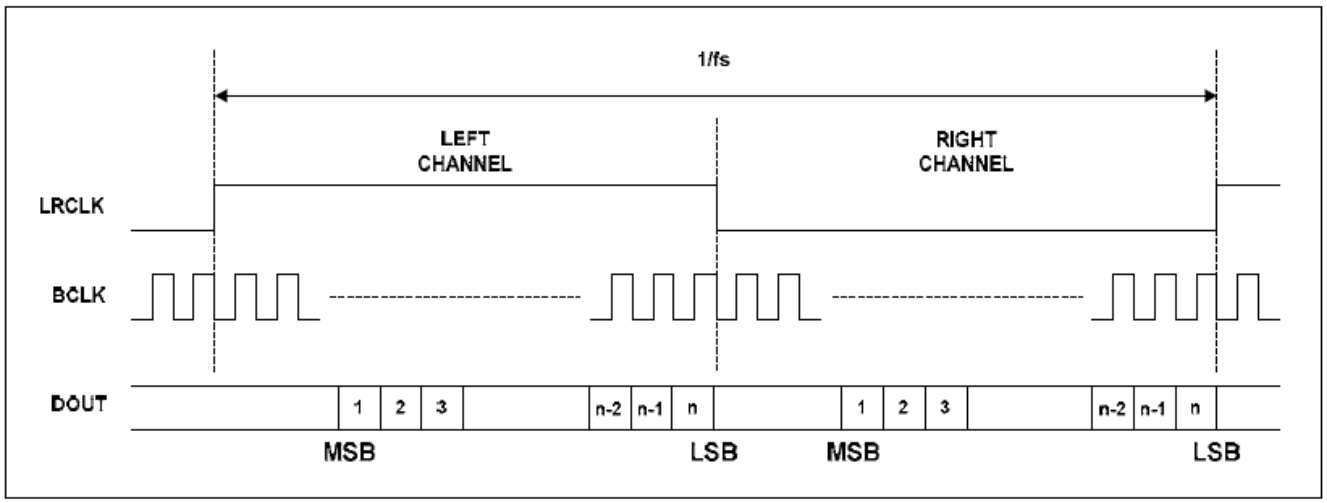
■ I2S format

In I2S mode, the MSB is available on the second rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending the on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.



■ R-justified format

In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending the on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition. In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending the on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.



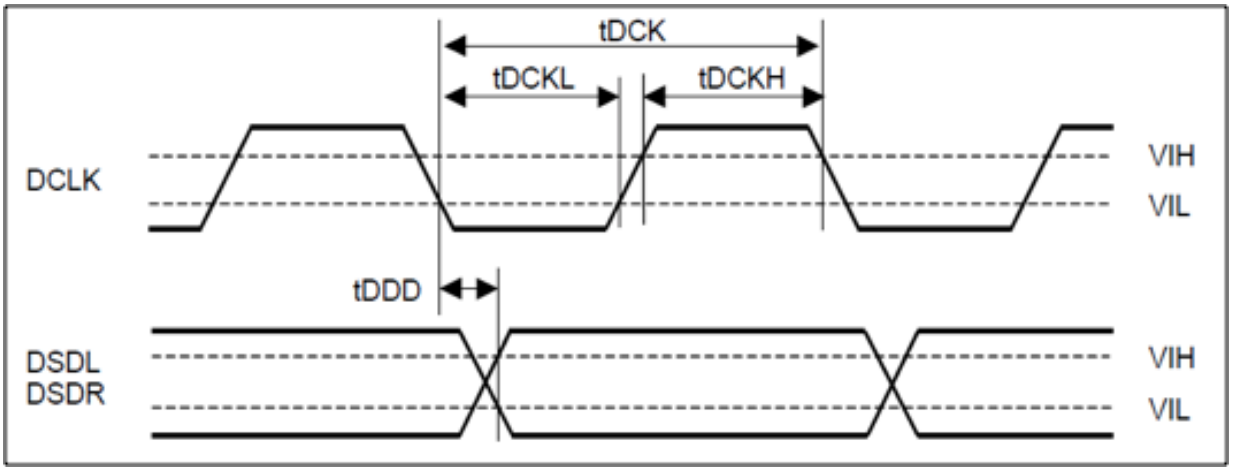
DSD Audio Data Interfaces

Playback:

SA9127 supports five modes for playback DSD data over USB Audio stream

Supported DSD formats:

■ DSD 64 for 88.2K 32-bit	DCLK(@2.8224MHz)	Direct-DSD
■ DSD 128 for 176.4K 32-bit	DCLK(@5.6448MHz)	Direct-DSD
■ DSD 256 for 352.8K 32-bit	DCLK(@11.2896MHz)	Direct-DSD
■ DSD 64 for 176.4K 24-bit	DCLK(@5.6448MHz)	DoP/dCS
■ DSD 128 for 352.8K 24-bit	DCLK(@11.2896MHz)	DoP/dCS

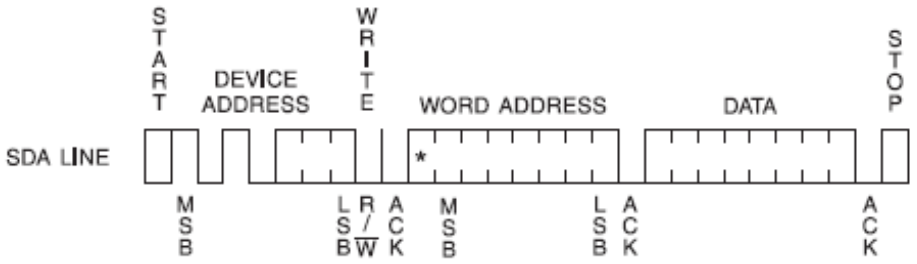


The DSDL and DSDR are all output by negative edge of DCLK. And DSD DAC will sample them by post edge of DCLK.

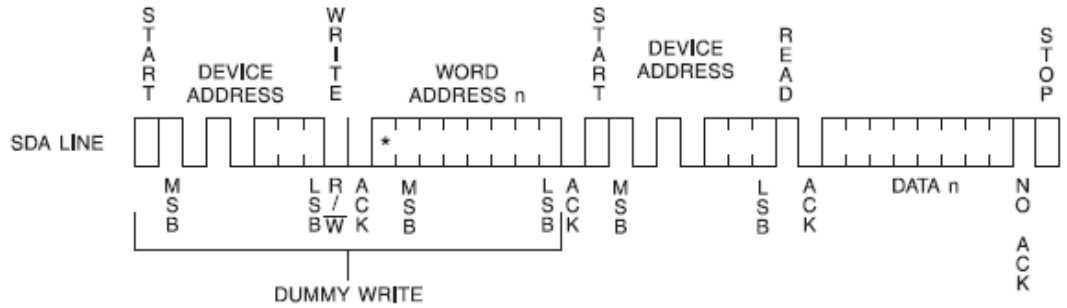
I²C Master Interfaces

One serial I²C master is supported in SA9127 to control external peripheral devices (EEPROM). SA9127 needs at least 32KByte EEPROM to load Firmware code.

Byte Write



Random Read



DSD External Control Signals

SA9127 provides these pins for DSD and special usage

FLAGs	Definition
SOF_FLAG	User can check this pin to understand USB is in suspend or not 0: USB is in suspend 1: USB is in normal mode
DSD_FLAG	User can check this pin to understand DSD mode is detected or not 0: PCM mode 1: DSD mode
DSD_128_FLAG	User can check this pin to understand which DSD mode is played now (DSD64 or DSD128 mode) 0: DSD 64 mode 1: DSD 128 mode

WQFN-48 Pin Assignment

Pin	Name	Pin	Name
1	TEST	33	DBCLK / DSD_CLK
2	VDD33_LDO	34	VDD18
3	GND_LDO	35	VDD33
4	VDD18_LDO	36	DDATA / DSD_DL
5	VDD33	37	DMCLK
6	VDD33	38	DLRCK / DSD_DR
7	VDD18	39	ABCLK
8	SOF_FLAG	40	ADATA
9	DSD_DLAG	41	AMCLK
10	DSD_128_FLAG	42	VDD33
11	REXT	43	ALRCK
12	VDD33	44	VDD33
13	VDD33	45	TEST
14	DP	46	VDD18
15	DM	47	TEST
16	GND	48	TEST
17	XI	49	Thermal PAD
18	XO		
19	VDD18		
20	VDD33		
21	VDD33		
22	VDD33		
23	VDD18		
24	VDD33		
25	GPIO1		
26	GPIO4		
27	GPIO5		
28	GPIO6		
29	RESETN		
30	VDD33		
31	SCL		
32	SDA		

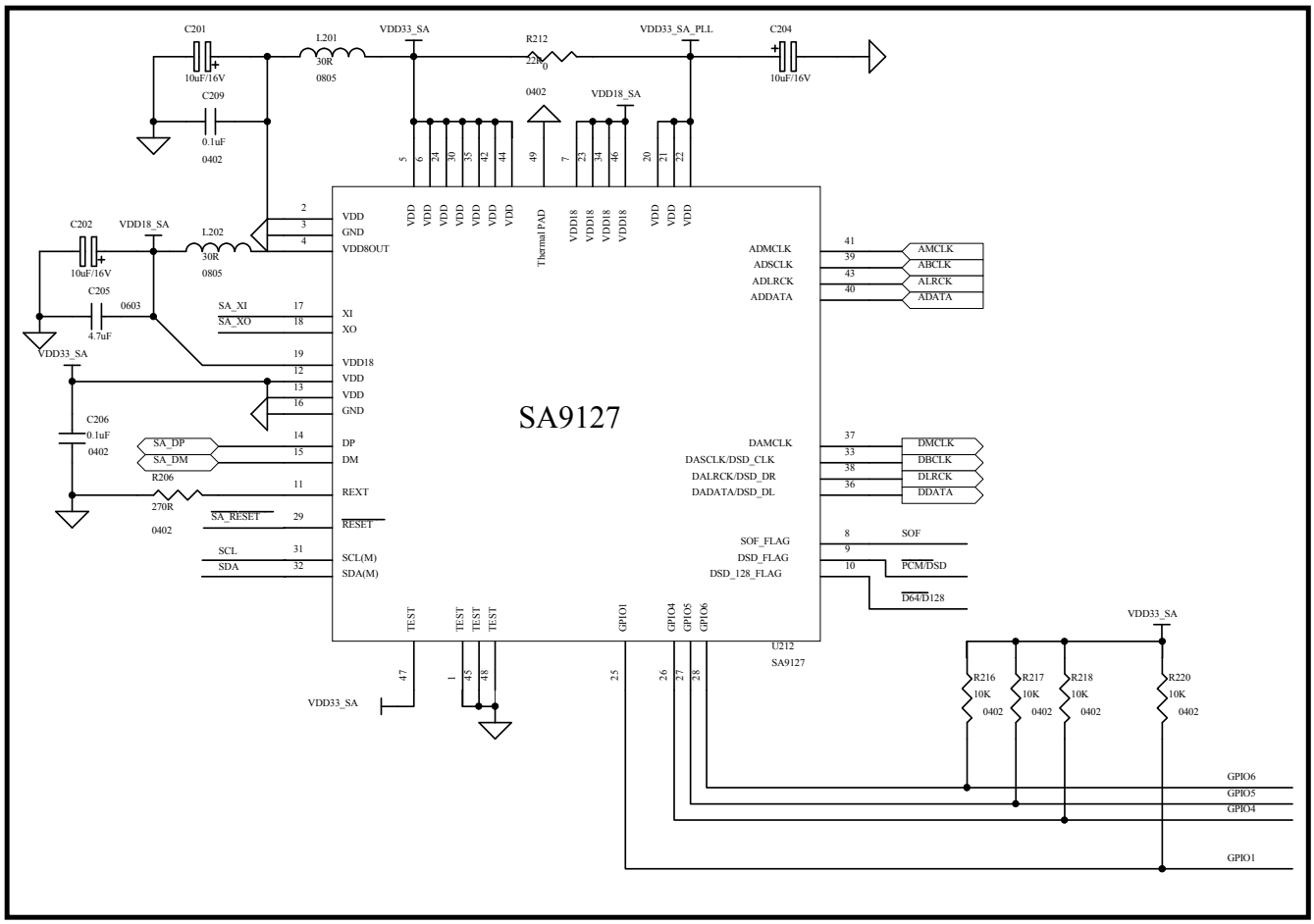
WQFN-48 Pin Description

Pin	Name	I/O/P	Description
1	TEST	I	Normal Operation needs pull-down
2	VDD33_LDO	P	LDO 3.3V Input
3	GND_LDO	P	LDO Ground
4	VDD18_LDO	P	LDO 1.8V Output
5	VDD33	P	I/O power
6	VDD33	P	I/O power
7	VDD18	P	Core power
8	SOF_FLAG	O / 3.3V	USB SOF(Start Of Frame) indicator
9	DSD_DLAG	O / 3.3V	DSD/PCM indicator, 0 : PCM, 1 : DSD
10	DSD_128_FLAG	O / 3.3V	DSD64/DSD128 indicator
11	REXT	I	Connect 270ohm resistor to ground
12	VDD33	P	USB2.0 PHY power
13	VDD33	P	USB2.0 PHY power
14	DP	I/O	USB2.0 signals
15	DM	I/O	USB2.0 signals
16	GND	P	USB2.0 PHY ground
17	XI	I	12MHz X'stal
18	XO	O	12MHz X'stal
19	VDD18	P	USB2.0 PHY power
20	VDD33	P	PLL power
21	VDD33	P	PLL power
22	VDD33	P	PLL power
23	VDD18	P	Core power
24	VDD33	P	I/O power
25	GPIO1	OD	General purpose I/O, For DAC reset used
26	GPIO4	OD	General purpose I/O
27	GPIO5	OD	General purpose I/O
28	GPIO6	OD	General purpose I/O
29	RESETN	I / 3.3V	Power-on reset signal (active low)
30	VDD33	P	I/O power
31	SCL	I/O / 3.3V	Master I2C clock
32	SDA	I/O / 3.3V	Master I2C data

Pin	Name	I/O/P	Description
33	DBCLK / DSD_CLK	I/O / 3.3V	I2S output BCLK / DSD Clock
34	VDD18	P	Core power
35	VDD33	P	I/O power
36	DDATA / DSD_DL	I/O / 3.3V	I2S output DATA / DSD LEFT DATA
37	DMCLK	I/O / 3.3V	I2S output MCLK
38	DLRCK / DSD_DR	I/O / 3.3V	I2S output LRCK / DSD RIGHT DATA
39	ABCLK	I/O / 3.3V	I2S input BCLK
40	ADATA	I/O / 3.3V	I2S input DATA
41	AMCLK	I/O / 3.3V	I2S input MCLK
42	VDD33	P	I/O power
43	ALRCK	I/O / 3.3V	I2S input LRCK
44	VDD33	P	I/O power
45	TEST	I	Normal Operation needs pull-down
46	VDD18	P	Core power
47	TEST	I	Normal Operation needs pull-high
48	TEST	I	Normal Operation needs pull-down
49	Thermal PAD	P	Connect to GND

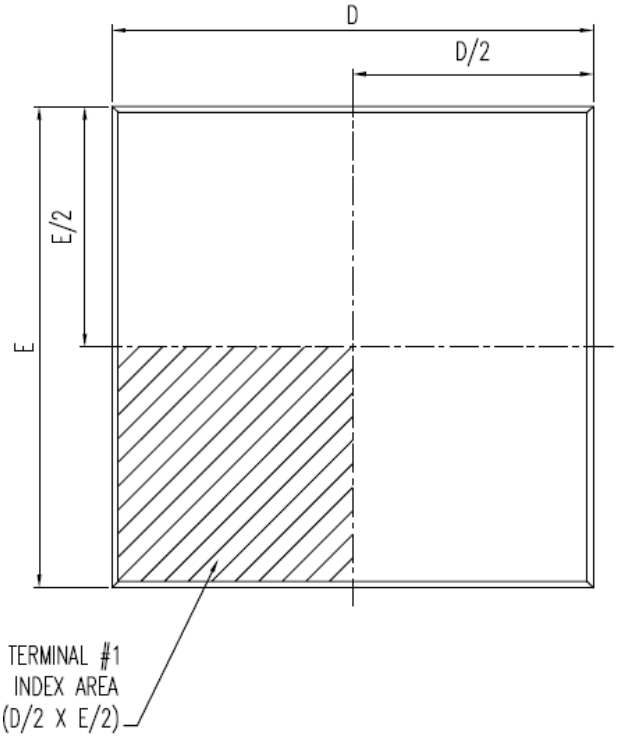
REFERENCE DESIGN

SA9127

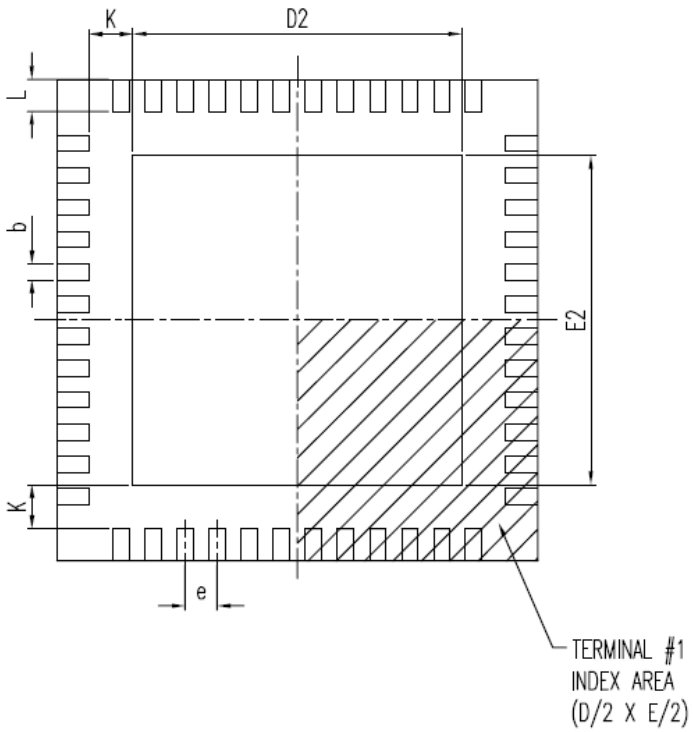


WQFN 48 MECHANICAL DATA

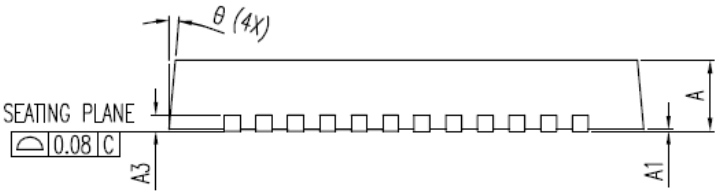
TOP VIEW



BOTTOM VIEW



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20 REF.	
D		6.00 BASIC	
D2	3.95	4.10	4.25
E		6.00 BASIC	
E2	3.95	4.10	4.25
e		0.40 BASIC	
b	0.15	0.20	0.25
L	0.30	0.40	0.50
K	0.20		
θ	0°		14°
JEDEC		MO-220 (Variation WJJE)	



SIDE VIEW