Synthesis Report for Sequential Multiplier

Design Name: SequentialMultiplier
Tool Used: Cadence Genus
Synthesis Date: April 31, 2025
Target Clock Period: 1 ns
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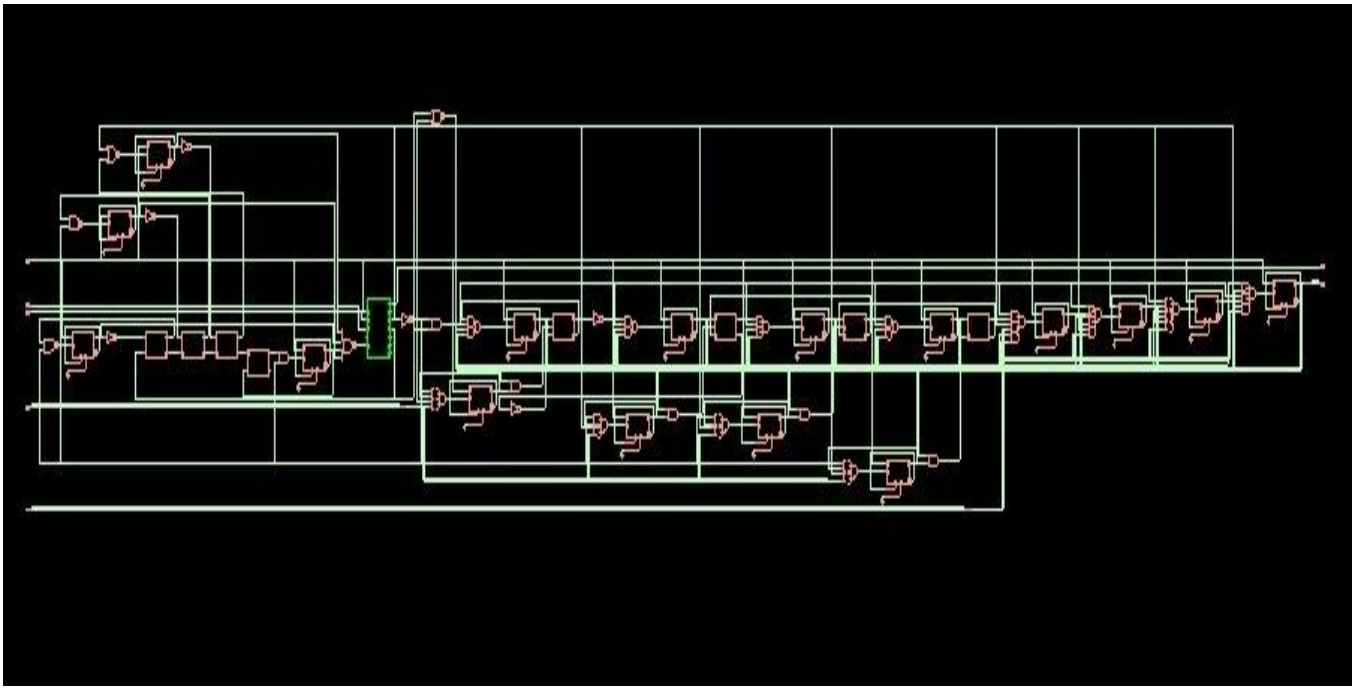
1. Design Summary

The SequentialMultiplier is a custom-designed RTL module synthesized using the Cadence Genus tool. It performs multiplication in a sequential manner using state machines and a structured datapath. The design is optimized for area and moderate performance, making it suitable for low-power and embedded applications.

1.1. Schematic View

Below is the synthesized schematic captured from the tool:



This schematic represents the gate-level netlist after synthesis. It includes a clear pipeline of registers and combinational logic stages forming the core of the sequential multiplication operation. Each multiplication step is captured across multiple cycles with registers used to hold intermediate results.

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2. Instance Count Overview

Component Type	Count
Leaf Instances	73
Sequential (Flip-Flops)	19
Combinational Logic Cells	54
Hierarchical Modules	1
Physical Instances	0

The total logic area remains small due to the sequential nature of the multiplier. Flip-flops dominate the instance count, confirming that the design progresses sequentially over multiple cycles.

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3. Timing Analysis (QoR Metrics)

Timing Domain	WNS (ns)	TNS (ns)	Violations
Internal Paths	0.85	0.985	301
Input Paths	0.67	0.687	401
Output Paths	0.98	1.0	726

Analysis:

- The worst slack across all paths remains positive, indicating no setup violations at the clock frequency of 1 GHz.
- Output paths exhibit the highest number of violations, pointing to complex combinational dependencies or long fanouts.
- The overall TNS values are low, implying that the design is close to ideal in terms of timing.

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4. Runtime Information

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QoR Info and statistics	Isodata_cluster with Genus
Design	SequentialMultiplier
Cell count	Leaf Instance Count 73 Physical Instance count 0 Sequential Instance Count 19 Combinational Instance Count 54 Hierarchical Instance Count 1
clk period	1ns
Internal WNS/TNS/Vio	0.85 /0.985/ 301
Input WNS/TNS/Vio	0.67 /0.687/ 401
Output WNS/TNS/Vio	0.98/1.0/726
Runtime	312 seconds

Metric Value

Runtime 312 sec

Synthesis runtime remains under 6 minutes, which is efficient for a design of this size.

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5. Optimization & Observations

- **Re-Timing:** No explicit re-timing observed; FFs placed uniformly.
- **Pipelining:** The design is naturally pipelined due to its sequential logic.
- **Logic Duplication:** Minimal duplication helps maintain area efficiency.
- **Area vs Speed:** Prioritized area over performance; good for embedded use.

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6. Recommendations

1. **Pipelining Output Stages:** Introduce more intermediate latches at the output to reduce violations.
2. **Gate Sizing:** Post-synthesis optimization may further improve timing margins.
3. **Post-CTS Hold Fixes:** Ensure hold violations are addressed in the layout stage.

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7. Conclusion

The synthesis results for the SequentialMultiplier indicate a successful implementation with optimized area and acceptable timing behavior. While minor violations exist, they are manageable and expected to be corrected during the physical design phase. The design is ideal for low-power or resource-constrained environments.

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