Introduction

Previously while modelling several types of Inverters such as 120 degree square wave inverters, 180 degree square wave inverters, SPWM inverters, the necessity of dead-time was realised. Without it the inverters run a risk of malfunction due to shoot-through. Strategies of dead time introduction are available which were undertaken to eliminate any such chances. But due to the dead time itself, we observed several distortions in voltage waveform (in form of sharp notches) which could be detrimental for our inverter operated system. So in the following text, a method to eliminate the effects of dead-time has been explained.

Principle of Dead-Time Distortion [1]:

Dead-time is provided in between the gating signals of the top and bottom semiconductor switches in an inverter leg to prevent the shorting of DC bus. Due to this dead time, there is a significant unwanted change in the output voltage of the inverter. The effect is different for different pulse width modulation (PWM) methodologies. The effect of dead-time on the output fundamental voltage is studied theoretically as well as experimentally for bus-clamping PWM methodologies.

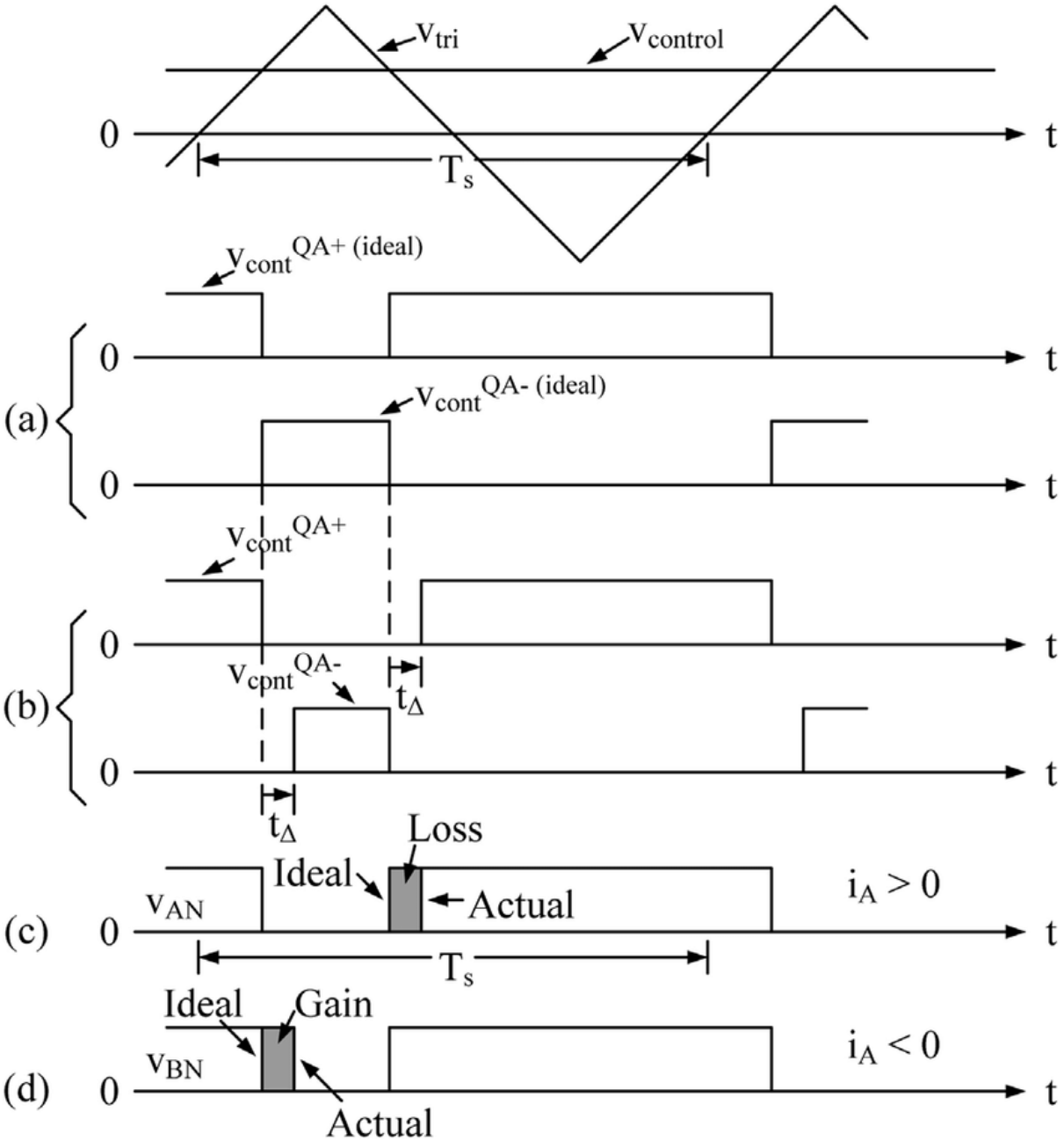

Fig.1 Effects of dead time.[2]

V_{AN} and V_{BN} represents the different voltage pulse-trains for positive and negative direction of current i_A respectively. If the current is positive (i.e. leaving the inverter leg), then as the figure suggests, the pulses are truncated by a length proportional to dead-time period. Whereas if i_A is negative, the pulses are protracted for the same length. This causes change in average voltage output depending upon the direction of current. This phenomenon is described in a diagram below.

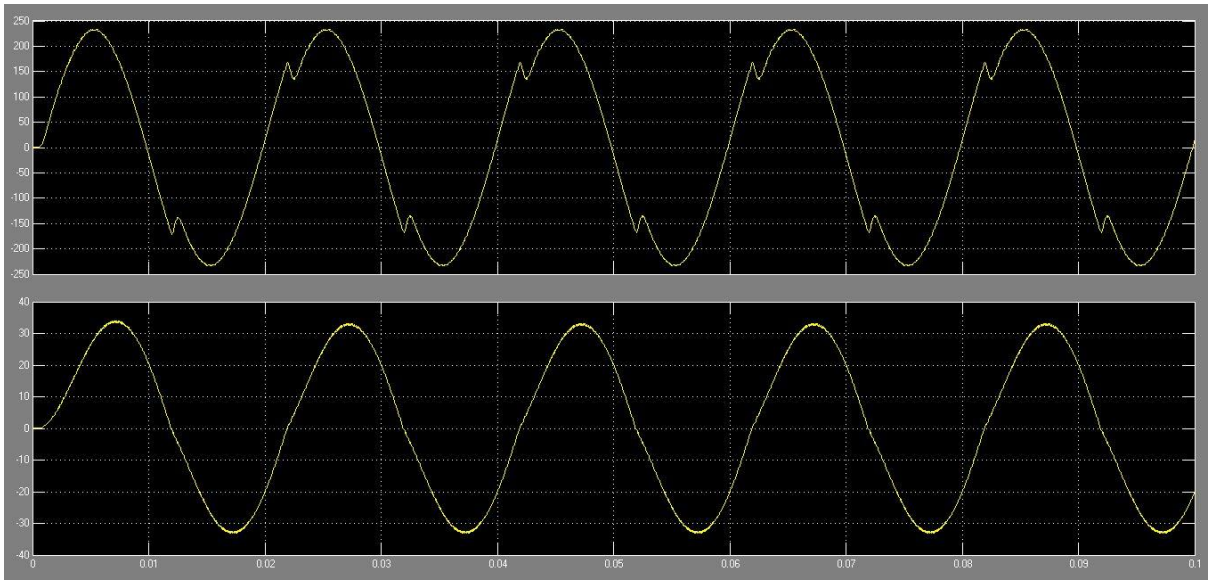

Fig.2 Upper waveform represents voltage waveform (filtered) with dead-time and lower represents current, notice how notches in voltage waveform appear at zero crossing of current.

SINGLE PHASE UNIPOLAR SPWM INVERTER [3]

The Modulation Process is Included in Inverter for Switching. A basic of Pulse Width Modulation (PWM) Technique is as. There are many forms of modulation used for communicating information. When a high Frequency signal has amplitude varied in response to a lower frequency signal we have AM (amplitude modulation).When the signal frequency is varied in response to the modulating signal we have FM (frequency modulation. These signals are used for radio modulation because the high frequency carrier signal is needs for efficient radiation of the signal. When communication by pulses was introduced, the amplitude, frequency and pulse width become possible modulation options. In many power electronic converters where the output voltage can be one of two values, the only option is modulation of average conduction time.

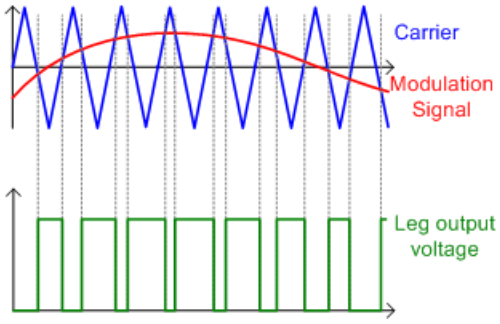

Fig.3 PWM pulse generation.[4]

Instead of, maintaining the width of all pulses of same as in case of multiple pulse width modulation, the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse. The distortion factor and lower order harmonics are reduced significantly. The gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency Fc. The frequency of reference signal Fr, determines the inverter output frequency and its peak amplitude Ar, controls the modulation index M, and Vrms output voltage VO. The number of pulses per half cycle depends on carrier frequency. Inverters that use PWM switching

techniques have a DC input voltage that is usually constant in magnitude. The inverters job is to take this input voltage and output ac where the magnitude and frequency can be controlled. There are many different ways that pulse-width modulation can be implemented to shape the output to be AC power. A common technique called sinusoidal-PWM will be explained. In order to output a sinusoidal waveform at a specific frequency a sinusoidal control signal at the specific frequency is compared with a triangular waveform. The inverter then uses the frequency of the triangle wave as the switching frequency. This is usually kept constant. The triangle waveform, vtri, is at switching frequency fs; this frequency controls the speed at which the inverter switches are turned off and on. The control signal, vcontrol, is used to modulate the switch duty ratio and has a frequency f1. This is the fundamental frequency of the inverter voltage output. Since the output of the inverter is affected by the switching frequency it will contain harmonics at the switching frequency. The duty cycle of the one of the inverter switches is called the amplitude modulation ratio, ma

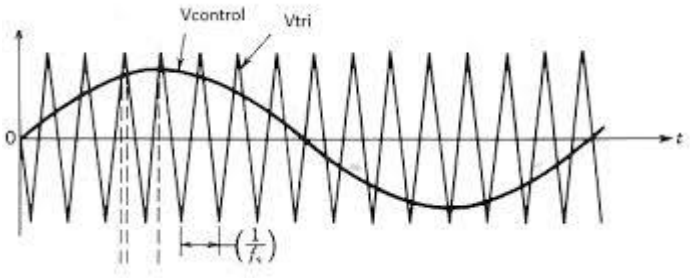

Fig.4 Desired Frequency is compared with a Triangular Waveform.[6]

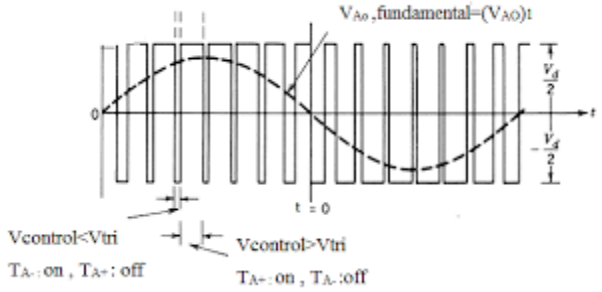

Fig.5 Pulse-width Modulation (PWM).[7]

Vcontrol and Vtri .The two switches are never off at the same time which results in the output voltage fluctuating between +/- Vd/2.Where voltage outputs are measured with respect to load neutral.

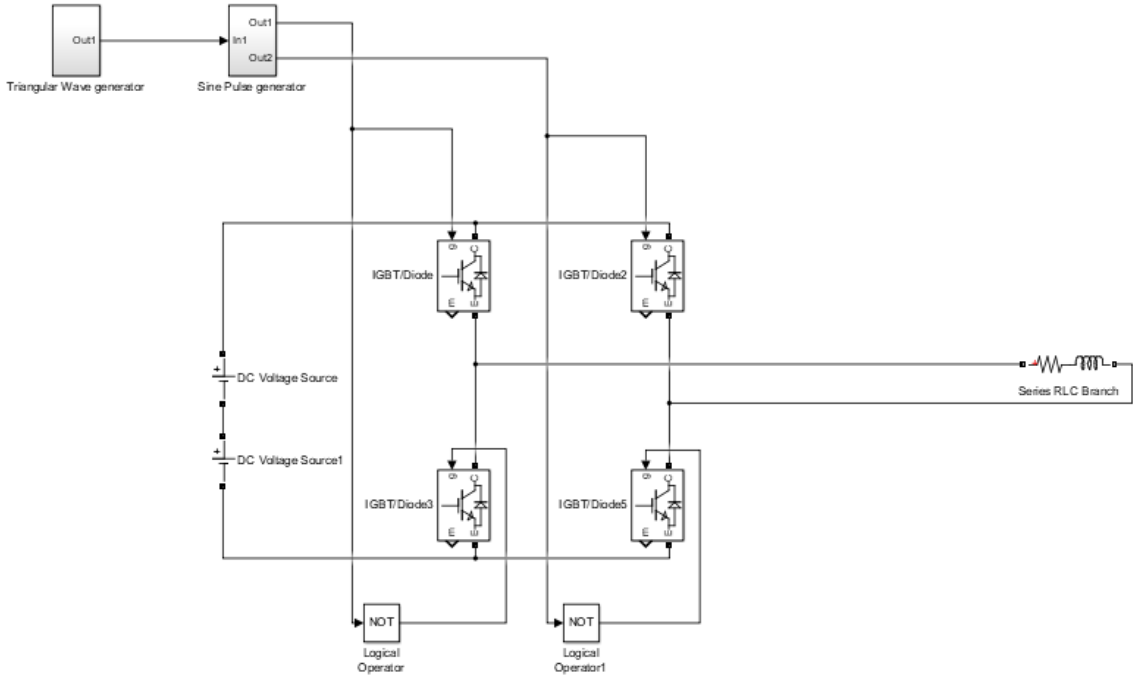

Fig.6 Simulink model of Sine PWM inverter.

In the presented model, The PWM signals were produced (by the masked boxes) and were fed to the IGBTs so as to cause the switching. Snubber resistances used is of the order 10^5 ohms and snubber capacitances is 47 nF. This results in an output which was fed to RL output.

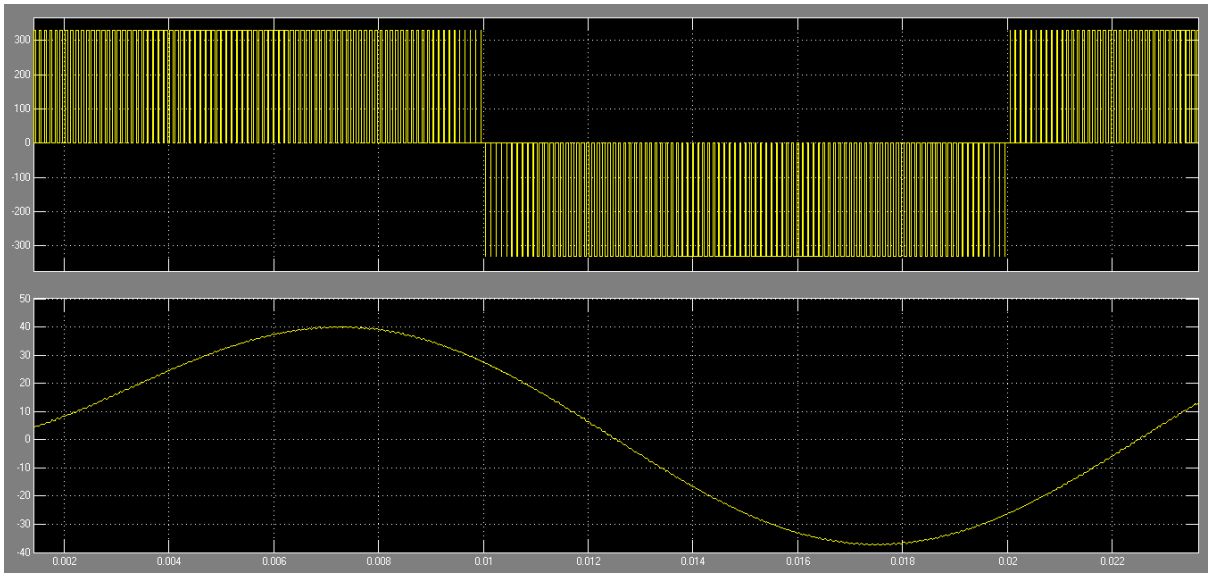

Fig.7 SPWM output waveform(unfiltered)

Dead-Time Distortion in SPWM Inverter

Dead-time/Blanking-time was added to the switching of SPWM inverter using a particular scheme. The model is given below.

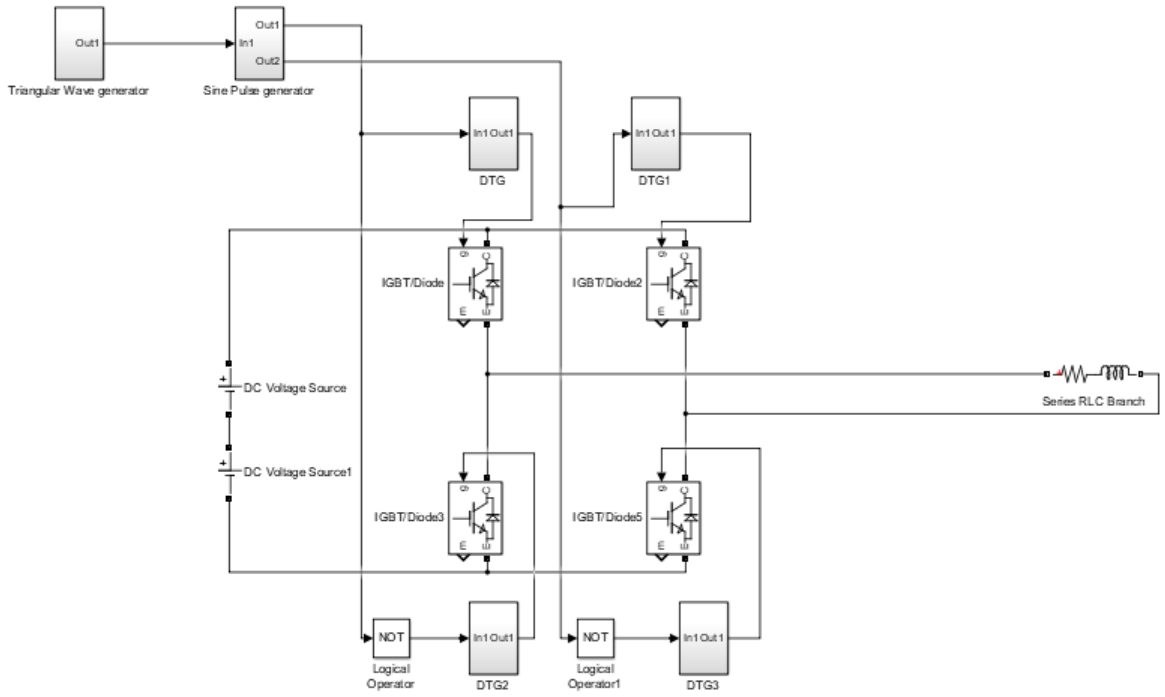

Fig.8 SPWM inverter with dead-time

The above figure represents the same SPWM inverter but with dead-time generators (DTGs) inserted. The RL load is being fed by the inverter and the following waveform is obtained.

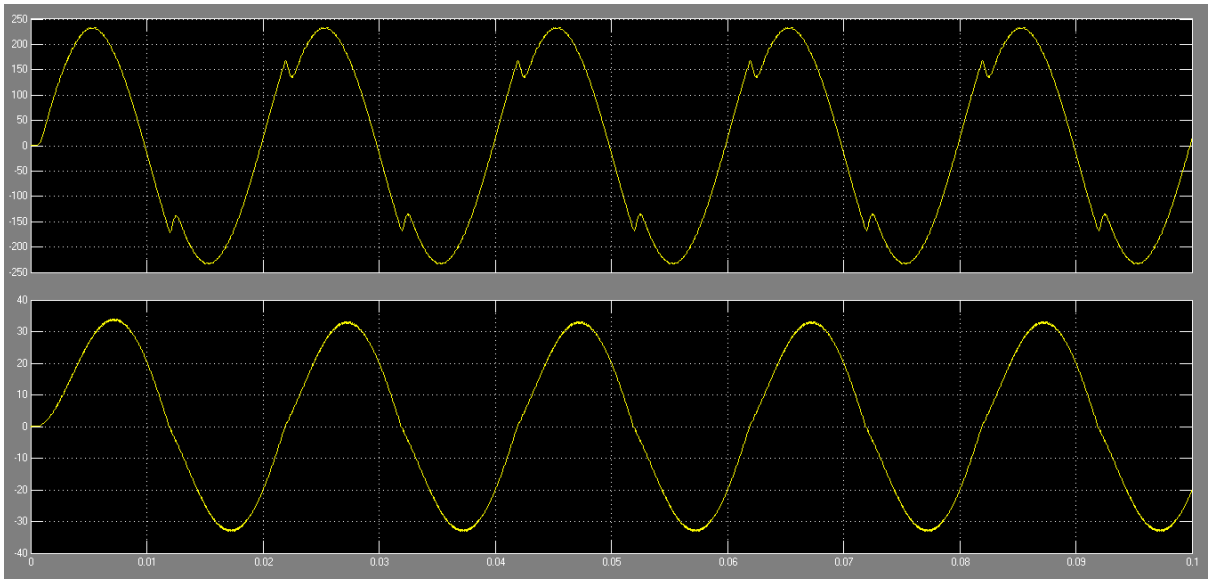

Fig.9 Phase - load neutral voltage of a 3 phase SPWM inverter with dead-time.

We can clearly see 2 notches per half cycle in the obtained waveform. These notches are due to the dead – time inserted in our model.

A Dead-Time Elimination Strategy (by Lihua Chen and Fang Zheng Peng) [5]

As discussed in section about dead-time and its effects, it was concluded that dead time can cause significant distortion to the voltage waveform. To counteract these problems, the aforementioned authors suggested the following solution. In the model proposed, an inverter leg containing two switches is replaced by that with a switch and a diode. The relative position of switch and diode depended on the current direction, which requires a current sensor.

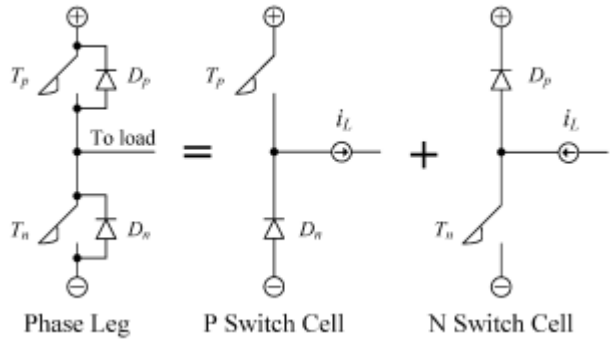

Fig.10 Decomposition of ideal inverter leg.

Which of the following two configurations is to be used is dictated by the direction of current flow. If the current is positive (i.e. flowing out of the leg) then diode should be at the bottom (which is obvious from the topology) and at the top if it is negative (i.e. flowing in to the leg)

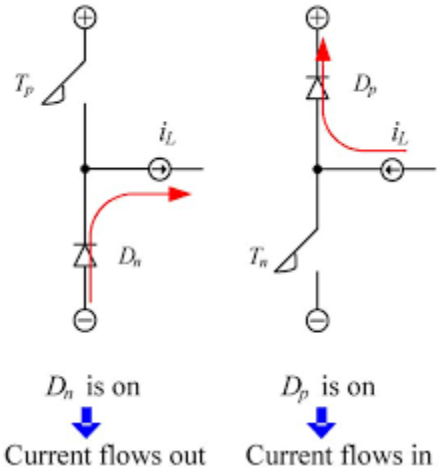

Fig.11 Switching between configurations.

In either of the configuration, since only one switch is working at a time, absolutely no dead time is required at all. This eliminates the voltage waveform distortion due to dead time.

Simulink Implementation of Dead-Time Elimination Strategy

The discussed model was implemented in Simulink. Since inverters designed in it used IGBTs, it is simple to use its antiparallel as operational diode of the discussed model.

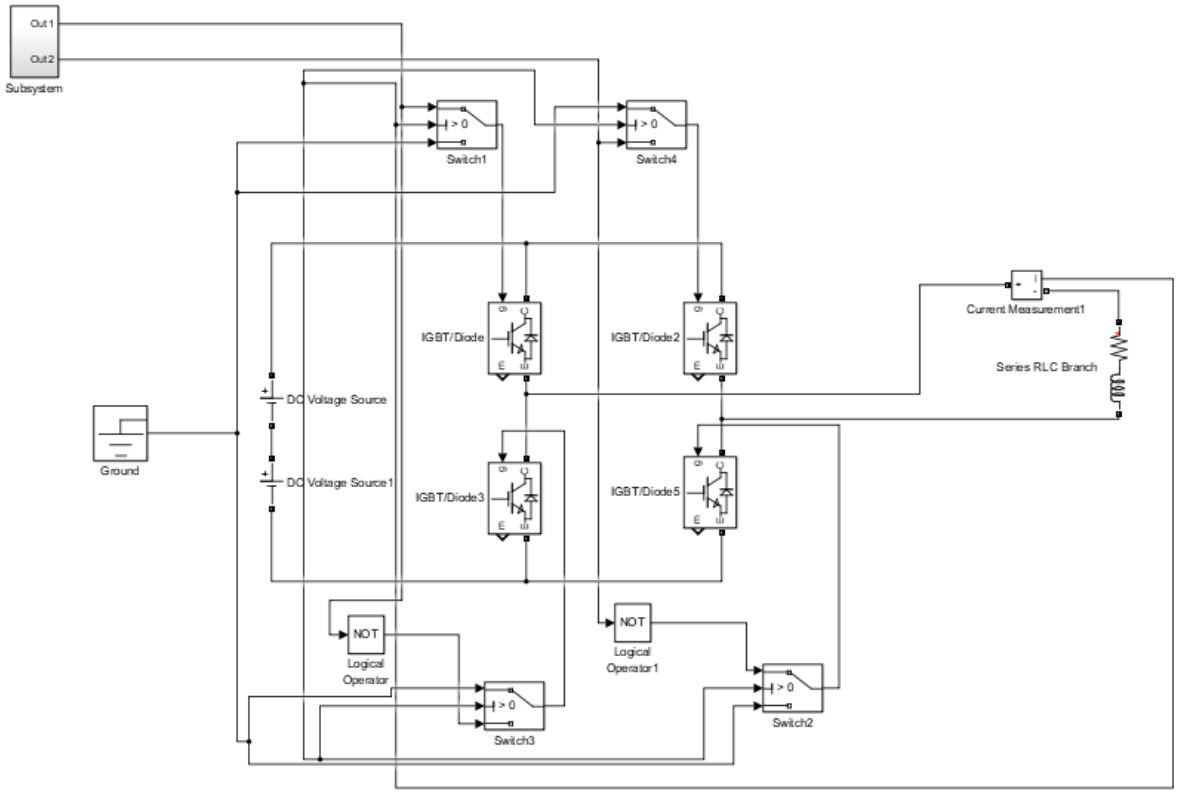

Fig.12 Simulink model for dead-time elimination by Chen and Peng.

In the above diagram, an SPWM inverter is shown as a Simulink model. A current sensor senses the direction of the current which is connected to a switch. The switch either grants an access to the SPWM pulses to gating input of IGBTs or to the zero voltage, if the access is to the zero voltage then the IGBT act as a simple diode. The entire connection is arranged in such a way that it fulfils the Dead-time elimination scheme discussed in the previous section.

Results

Upon simulation of the described strategy, it was observed that the notches completely disappeared as was desired.

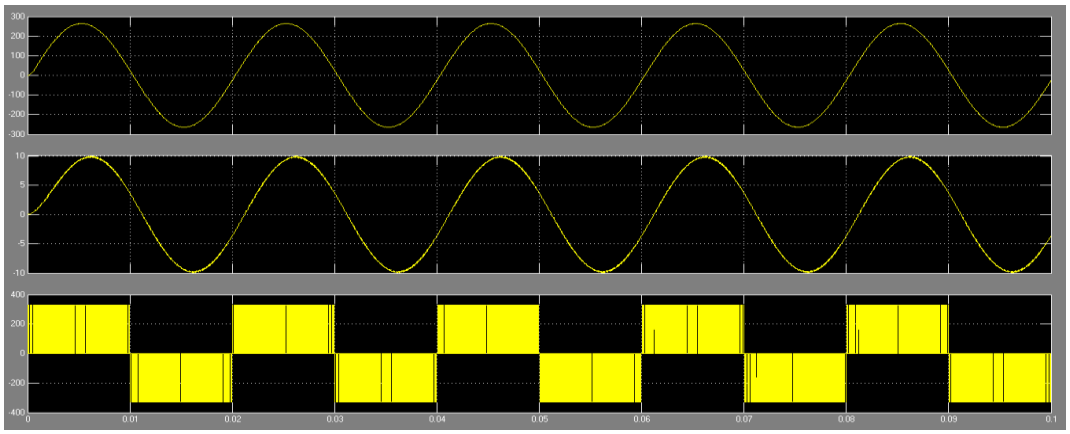

Fig.13 Peng output voltage waveform.

Also, an operation curve was plotted which is a curve of Modulation Index vs L/R ratio. The resultant curve in a way gives the domain of operation of the discussed model.

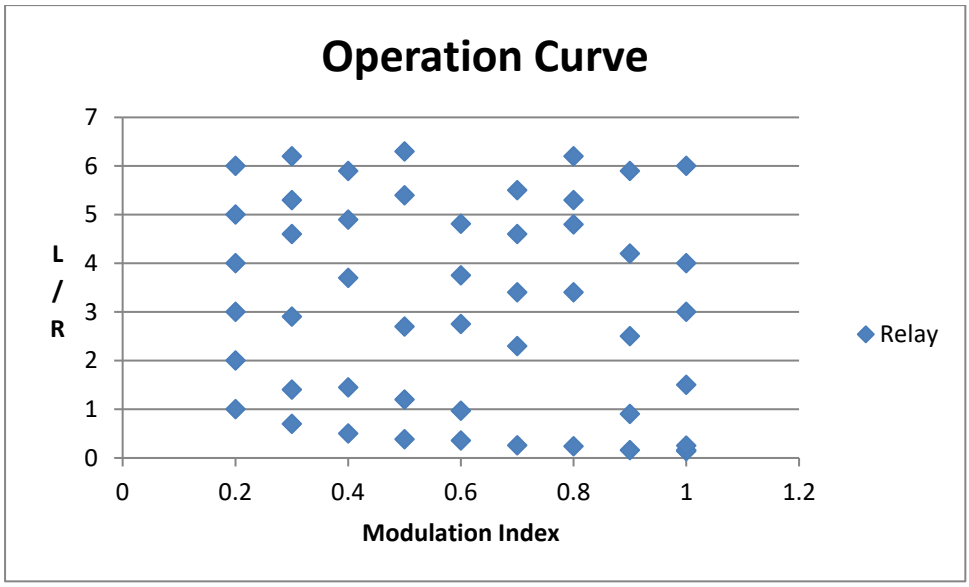

Fig.14 all region above the blue base line lies within operation zone.

Conclusion

Dead time is required to avoid negative consequences of current shoot-through across the IGBTs. But dead-time itself causes certain periodic distortions in voltage waveform which appear as sharp notches. It was inferred that there exists a strategy that can be used to overcome this issue. In the strategy discussed only one of the switches in the leg was operated,the other being dormant until the current direction changes . This leaves no requirement for the dead time as there are no two IGBTs working simultaneously at any time. But it was also determined that performance of the discussed model detoriated as L/R ratio lowered or Modulation Index reduced.

At extremely low values of L/R, time constant becomes smaller than the the pulse width, forcing the pole voltage to float. This causes detoeiation in performances. Efforts can be made to ensure operation at such low L/R ratio.

References:

[1] Tapas Roy[1], V. S. S. Pavan Kumar Hari[2] and G. Narayanan3Department of Electrical Engineering, Indian Institute of Science, Bangalore 560 012, INDIA E-mail: tapas18roy@gmail.com[1], pavan@ee.iisc.ernet.in[2], gnar@ee.iisc.ernet.in[3]

[2]https://www.researchgate.net/figure/Effect-of-dead-time-blanking-time_fig3_309039984

[3],[6],[7] Simulation of single phase SPWM (Unipolar) inverter SACHIN MAHESHRI & PRABODH KHAMPARIYA

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[5] Lihua Chen and Fang Zheng Peng, IEEE Transactions on Power Electronics, March 2008