Data Structures

Makefile – Introduction

CODE
FORTHINGS

Makefile

Introduction

- Why Makefile?
- What is Makefile?
- Implementation

Introduction

Introduction

Introduction

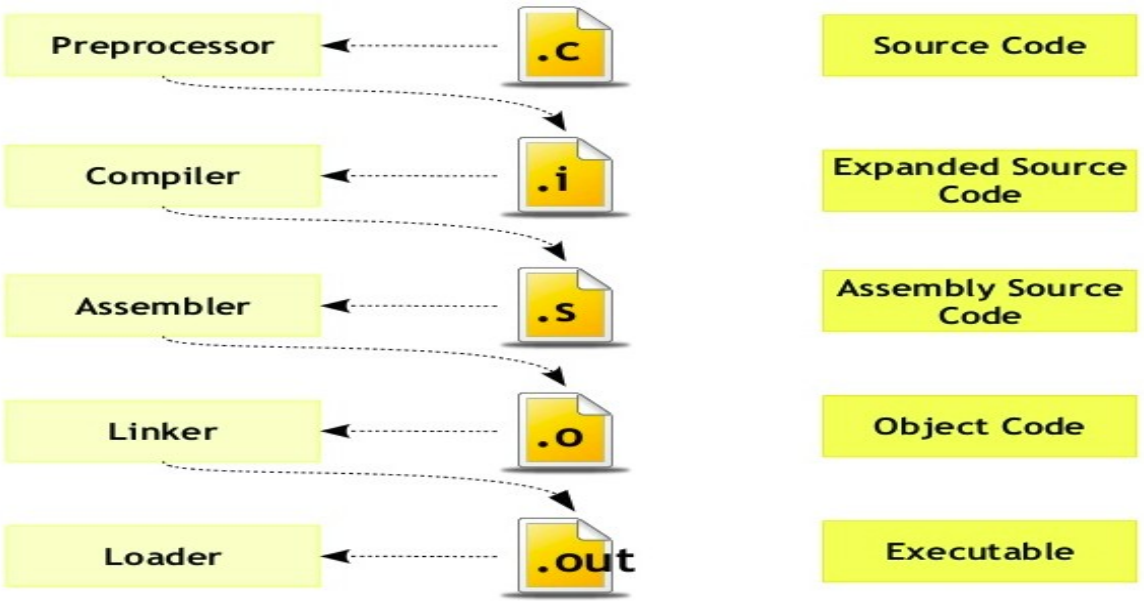
Different Stages of Compliation

- Preprocessor
- Compiler
- Assembler
- Linker
- Loader

Introduction

1.c ⟶ a.out

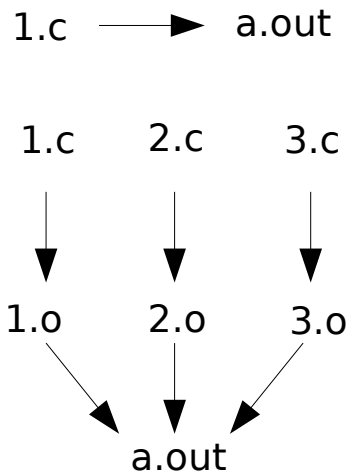
Compilation Stages



Introduction

1.c 2.c 3.c

Introduction



Introduction

Why?

Project ⟶ 1000 source file

Introduction

Why?

Project ⟶ 1000 source file

- gcc <all source files>
- gcc *.c

Introduction

What?

Makefiles are simple ways to organize code compilation

A makefile is a file containing a set of directives used by a make build automation tool to generate a target/goal.

Name

- Makefile
- makefile
- My_makefile make -f <MY_makefile>
- A makefile is executed using make command

Introduction

Rule

Target : Dependencies

<Tab> reciepe

Sub Target: Dependencies

<Tab> reciepe

clean:

<Tab>reciepe

Introduction

main.c add.c mul.c sub.c

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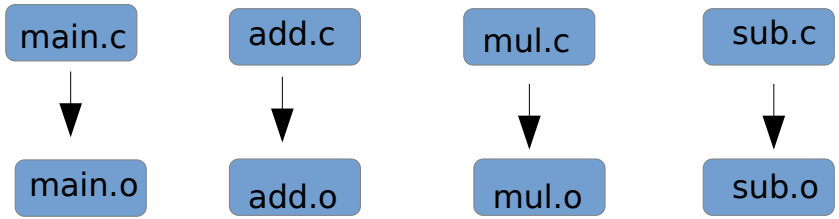

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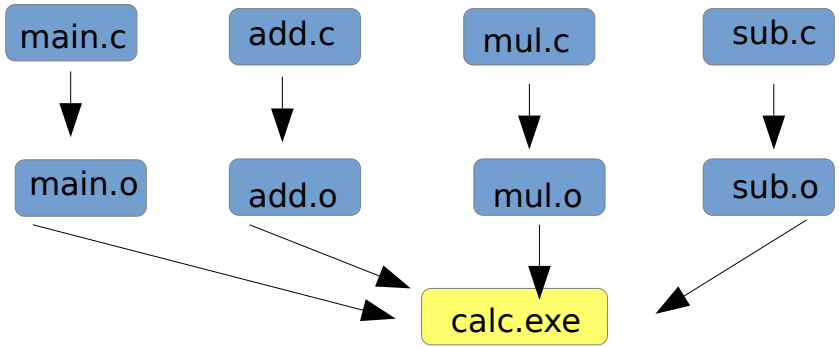

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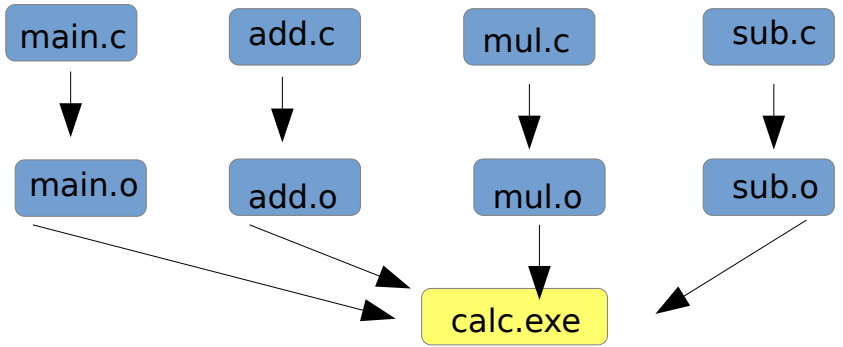


```
calc.exe : main.o add.o mul.o sub.o
<Tab>gcc -o calc.exe  main.o add.o mul.o sub.o
main.o: main.c
<Tab>gcc -c main.c
add.o: add.c
<Tab>gcc -c add.c
sub.o: sub.c
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clean:
<Tab>rm  *.exe  *.o
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Introduction

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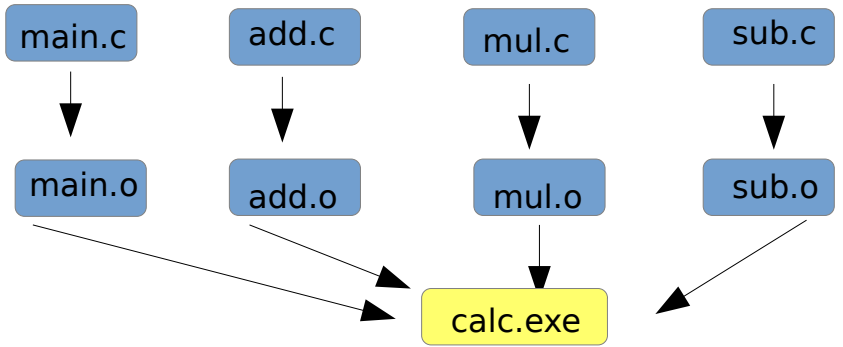


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CFT CODE FORTHINGS

Makefile -Implementation

Introduction

Rule

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<Tab> reciepe

Sub Target: Dependencies

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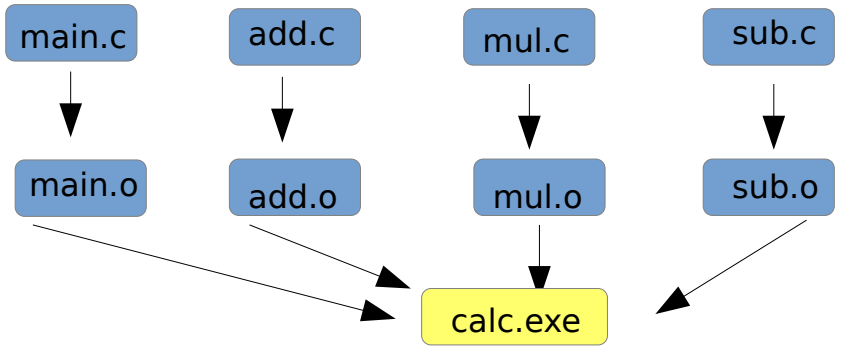
clean:

<Tab>reciepe

Alternate

```
OBJ : $(patsubst %.c, %.o, $(wildcard *.c))
calc.exe: $(OBJ)
<Tab> gcc -o  $@  $^
clean:
<Tab> rm  *.exe *.o
```

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Introduction

Advantages

- The compliation is done using single command ie make
- Re compiles only what is needed when you make a change
- Make keeps track of time

Time Complexity