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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth Semester B.Tech Degree Examination July 2021 (2019 Scheme)

Course Code:CST202

Course Name: Computer Organization and Architecture

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1	Compare auto increment and auto decrement addressing modes with examples	3
2	Outline the steps involved in the execution of an instruction.	3
3	How is the two port memory organization of processor unit better when compared to scratch pad memory organization?	3
4	Give the block diagram of circuit that implements following statements in register transfer logic: T_1; C ←A T_5: C ←B	3
5	Draw the flow chart for Booth's Multiplication Algorithm	3
6	Illustrate Read After Write (RAW) hazard with an example	3
7	Explain PLA based control organization with the help of a diagram	3
8	Differentiate between horizontal and vertical microinstructions	3
9	List and explain the different types of ROMs	3
10	Explain the term locality of reference. How is this related to cache memory?	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	Identify the addressing modes that can be used for representing the following higher level language constructs in machine level. Illustrate each addressing mode using an example. 1) Arrays 2) Pointers 3) Constants 4) Variables	4

b) Illustrate the single bus organization of processor unit with the help of suitable diagrams. Explain, listing the control signals, how the following operations are handled in this organization. 10

i) Transfer contents of register R5 to R1

ii) Move (R6), R2 (*Fetch a word from memory and move it to register R2, when the memory address is stored in register R6*)

OR

12 a) Outline the differences in instruction execution during straight line sequencing and branching using suitable examples. 7

b) Differentiate between big endian and little endian byte ordering. 7

Consider a computer that has a byte addressable memory organized as 32 bit words. A program reads ASCII characters entered at a key board and stores them in successive byte locations, starting at location 1000. Show the contents of the two memory words at locations 1000 and 1004 after the name *Johnson* has been entered in case:

i) Big Endian Byte ordering is used

ii) Little Endian Byte ordering is used

(ASCII equivalent of characters in *Johnson* in hex will be 4A, 6F, 68, 6E, 73,6F, 6E. You can indicate unused byte locations using XX).

Module -2

13 a) Illustrate and explain the organization of a processor unit where processor registers and ALU are connected through common buses. Explain how the micro operation **R2 ← R3+R4** would be performed using this organization, where R2, R3 and R4 are processor registers. 7

b) Explain with the help of a block diagram the design of a 4 bit status register for an 8 bit ALU. The four status bits are C (carry), S(sign), Z(zero) and V (overflow). Clearly indicate the purpose of each status bit and how they are set or reset. 7

OR

14 a) Design and draw a combinational logic shifter using multiplexers with two selection variables, H_1 and H_0. The operations of shifter should be as specified in the following table: 10

H_1	H_0	Operation	Function
0	0	S←0	Transfer 0's to S
0	1	S←shl F	Shift left F into S
1	0	S←shr F	Shift right F into S
1	1	S←F	No shift

b) Describe about arithmetic, logic and shift micro operations, listing the available operations in each category. 4

Module -3

15 a) Outline the hardware requirement for multiplying two binary numbers in sign magnitude format and specify a flowchart for same. Illustrate the algorithm, showing the contents of registers, for the multiplication of **11111** by **10101** 8

b) Explain the various pipeline structures available inside a computer 6

OR

16 a) Design and draw the block diagram for a 4 by 3 array multiplier. 8

b) Explain the various method available to get rid of data hazards inside the system 6

Module -4

17 a) Illustrate the working of a micro program sequencer with the help of diagrams 7

b) Outline with the help of a block diagram, how a micro program control unit can be used for controlling the processor unit. 7

OR

18 Illustrate the steps for designing a micro programmed control circuit for the addition and subtraction of binary numbers in sign magnitude form. Specify the block diagram of control circuitry and the binary micro program for control memory. 14

Module -5

19 a) Explain with examples the three types of mapping functions used in cache memory 7

b) What are interrupts? Outline the actions taking place in a processor once an interrupt has been raised. 7

OR

20 a) What is a DRAM? Compare the two types of DRAMs, highlighting their differences. 7

b) Outline how Direct Memory Access is implemented? Differentiate between cycle stealing DMA and burst mode DMA. 7

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth Semester B.Tech Degree Examination June 2022 (2019 scheme)

Course Code: CST202

Course Name: Computer Organization and Architecture

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1	Describe auto increment and decrement addressing mode with help of example?	3
2	Name the registers which are connected to both external and internal bus? What are the signals associated with these registers?	3
3	Write the register transfer logic format for a conditional control statement, Give an example?	3
4	Discuss the logic used behind the booth multiplication algorithm	3
5	Draw a 3X2 array multiplier?	3
6	Discuss about pipeline hazards?	3
7	Write a note on micro-program control?	3
8	What are different types of control organization?	3
9	What are interrupts, List the sequence of steps following an interrupt request?	3
10	Which design feature of SRAM cells helps in value retention without refresh?	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	Compare and contrast single bus and multi-bus organization of CPU?	4
	b)	Write the three-address, two-address and one-address representations of the operation below with relevant assumptions, evaluate following: i, (A+B) * (C+D) ii, C<- [A] + [B]	10
12	a)	With the help of a neat figure, describe the data path inside the processor?	6
	b)	Draw the diagram of single bus organization, write the control sequence for the instruction ADD [R2],R3 for the above mentioned single bus organization.	8

Module -2

13	a)	Describe processor organization with diagram using i) scratchpad memory ii) Two-port memory iii) Accumulator register	10
	b)	Draw and explain about true/complement circuit?	4

14 a) Give the structure of status register, which is connected to 8bit ALU . 8

b) Design 4-bit combinational logic shifter which will perform the operation given below with 2 control variable H1&H0? 6

i) Shrl

ii) clear

iii) Load all bits with 1

Module -3

15 a) Draw the flowchart and explain restoring division method with an example? 6

b) Describe in detail about data hazards and resolution techniques? 8

16 a) Draw the flowchart of Booth's multiplication algorithm and multiply -5 X -4 using booths algorithm? 8

b) Identify the various types of hazards occurring during the execution of the following program in a pipelined system. Where the pipeline consist of five stages, opcode fetch , instruction decode, operand fetch, execution, store the result. All stages take equal time duration 6

```
MOV [R1],[R2]
MOV R3,[R1]
SUB R2,R3
ADD R1,R3
CALL 5000
MOV R2,R3
```

Module -4

17 a) With the help of a diagram explain the functioning of a micro-program sequencer in a micro-programmed controlled processor? 10

b) Compare instruction formats of horizontal and vertical microinstructions? 4

18 a) Explain the organization of micro-programmed computer with a block diagram? 8

b) Explain with an example one flip-flop per state method of control organization? 6

Module -5

19 a) Explain in detail about the mechanisms for accessing I/O devices? 9

b) Discuss about different types of read only memories? 5

20 a) Explain internal organization of 1 K X 8 memory chip with suitable diagram 5

b) How does the various mapping scheme present in cache memory differ from each other. 9

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (R, S) / S2 (PT) (R, S) Examination June 2023 (2019 scheme)

Course Code: CST202

Course Name: Computer Organization and Architecture

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1	With a neat diagram explain the internal architecture of CPU?	3
2	Enumerate the sequence of actions (control signals) involved in executing an unconditional branch instruction?	3
3	What is micro-operation, With help of examples explain shift micro-operation	3
4	Check the correctens of the following statements and justify your results i)All unifunctional pipeline are static. But all static pipeline are not unifunctional. ii)All dynamic pipelines are multifunctional. But all multifunctional pipeline are not dynamic because different time	3
5	Divide (1000) 2 by (11) 2 using restoring division method.	3
6	With proper example describe about arithmetic pipelining?	3
7	Differentiate between vertical and horizontal microinstructions?	3
8	Draw and discuss about PLA control logic?	3
9	Why dynamic RAMs need constant refreshing? Give the structure also.	3
10	Differentiate about memory mapped I/O and I/O mapped I/O?	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	What do you mean by addressing modes, with proper examples explain in detail about various address modes?	10
	b)	Write down the sequence of actions needed to fetch and execute instruction: STORE R1,[R2]	4
12	a)	Draw the diagram of a multi-bus organization with 3 buses, write the control sequence for the instruction ADD [R1],R2,R3 for the above mentioned multi-bus organization.	9
	b)	What are condition codes, list the different condition codes?	5

Module -2

13	a)	Design an adder circuit with one selection variable S and 2 inputs A and B. When S=0 circuit performs A+B, when S=1 it performs A-B by taking twos complement of B?	9
	b)	Write a short note about accumulator register?	5
14	a)	Give a simple design for generating status bits for an 8-bit ALU?	6
	b)	How do a binary adder circuit can be used for the implementation of logical operation AND, OR, NOT, XOR.	8

Module -3

15	a)	What do you mean by array multiplier, design 3x3 array multiplier and list out its disadvantages?	7
	b)	Explain in detail about pipeline processors?	7
16	a)	Multiply following using booth's multiplication algorithm: -7 and -3	6
	b)	Describe in detail about instruction hazards and their solution?	8

Module -4

17	a)	With a diagram, explain how control signals are generated using hardwired control?	8
	b)	What are the different elements involved in micro-program control unit explain with a neat diagram?	6
18	a)	With the help of a flowchart for sign-magnitude addition/subtraction, explain the steps involved in developing a hardwired control unit?	10
	b)	Discuss about sequence register and decoder method of control organization?	4

Module -5

19	a)	Give the internal organization of 2MX8 memory module using 512 K X8 static memory chips	6
	b)	Explain the hit and miss condition occurring during the read and write operation on cache memory. Also give the importance of dirty bit during the writing operation.	8
20	a)	Differentiate centralized and distributed bus arbitration mechanism used in DMA?	6
	b)	With the help of example, explain different cache mapping functions?	8

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