Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree Regular and Supplementary Examination December 2022 (2019 Scheme)

Course Code: CST203

Course Name: Logic System Design

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks Marks

1		Perform the mentioned base conversions for the following numbers. (i) $(563.8125)_{10}$ to binary (ii) $(78.89)_{10}$ to octal (iii) $(EC.4)_{16}$ to decimal	(3)
2		The 2's complement representation of a binary number is 10101100. (i) Determine its decimal value. (ii) Represent it in 1's complement form.	(3)
3		Prove that $x(x + y) = x$ using Boolean algebra postulates and rules.	(3)
4		Find the number of possible unique Boolean functions which can be formed using n Boolean variables? Explain.	(3)
5		Design an even parity code generator using XOR gates for a 4-bit code.	(3)
6		Design an octal-to-binary encoder circuit using OR gates.	(3)
7		Specify the characteristics table and characteristic equation of RS flip-flop.	(3)
8		Differentiate synchronous counters and asynchronous counters. Give examples.	(3)
9		Design a 4-bit shift register using D flipflops.	(3)
10		Describe Read Only Memory with the help of a block diagram.	(3)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11	a	(i) Convert $(10111101.11100110)_2$ to octal and hexadecimal bases. (ii) Perform the binary operations 1101 **x** 110 and 10111 + 1101		(7)
	b	Convert the following decimal numbers to 8421 BCD and perform the operations. i) 528 + 374 ii) 528 - 374		(7)

12 a (i) Perform the binary subtraction 11011 – 1101 using 1's and 2's complements and verify results by direct subtraction. (10)

(ii) Perform the decimal subtraction 2210 – 3560 using 9's and 10's complements and verify results by direct subtraction.

b Add (i) Hexadecimal numbers B2A and 5C7 (ii) Octal numbers 763 and 456 (4)

Module 2

13 a The Exclusive-OR gate is represented by the Boolean algebra expression $AB' + A'B$. Using DeMorgan's theorem and other Boolean algebra rules/laws derive an expression for Exclusive-NOR gate. (5)

b Simplify the function $f(A,B,C,D) = \sum(0,1,2,8,12,13,14) + d(3,5,10,15)$ with Karnaugh map. d(.) refers to don't care conditions. Implement the simplified function using NAND gates. (9)

14 a Simplify the following function and implement using NOR gates. Assume both normal and complement inputs are available. $f(x,y,z) = \Sigma(0,4,6)$ (6)

b Express $F(x,y,z) = (xy + z)(y + xz)$ in both canonical forms. (8)

Module 3

15 a How does look-ahead carry reduce the carry propagation time in a binary parallel adder? Derive the Boolean functions for the carry outputs at different stages of a 4-bit look-ahead carry generator. (7)

b Design a 4-bit BCD adder and draw the block diagram. (7)

16 a Design a full adder circuit using a decoder and external gates. (6)

b Design a 3-bit Gray to binary code converter. (8)

Module 4

17 a With a circuit diagram, explain the working of master-slave JK flip-flop. (7)

b Explain the working of 4-bit register with parallel load with the help of a diagram. (7)

18 a Design a 4-bit binary asynchronous counter using JK flipflops. Give the state diagram and logic diagram. (8)

	b	Design a synchronous BCD Counter. Give the excitation table and circuit diagram.	(6)

Module 5

19	a	Describe the working of Programmable Logic Array (PLA) with a block diagram.	(7)
	b	Illustrate the algorithm for addition of 2's-complement numbers. State why 2's complement representation is preferred for binary arithmetic operations.	(7)
20	a	Design 4 bit Johnson counter and show its timing sequence.	(8)
	b	Explain the representation of floating point numbers. State the algorithm for floating point addition.	(6)

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