Embedded System Course Project

Title: D4 → Explicit Enumeration of design behaviors from RTL-based control-intensive design

Team Member: Vipul Sharma (B19CSE099), Raunak Gandhi (B19CSE117)

Instructor's Name: Dr. Binod Kumar

Introduction:

The project aims to write down behaviors explicitly from parsing RTL designs or can be said to convert a given Verilog file to a text file which is an enumeration of the Verilog design behaviors. We wrote a code that automatically converts these behaviors into statements that can be understood by the audience who may or may not know Verilog.

Flow of the Code:

We are checking the keywords in the code like always, if, else, etc. If any of these keywords are present in the line we are dealing with separately and write the explanation of that line in a text file. We are also handling the nested if-else statements. And assigning the value to register is handled separately. We are also numbering the behaviors by separating the blocks and numbering them accordingly.

Input Pattern:
Assumptions:

1) Some keywords, it can parse like:
    a) Always
    b) If
    c) Else
    d) Assign

    e) Begin
    f) End
    g) Logical operators
2) Spaces between parentheses and the parameters, operators and operands, assigned value and assigning a variable, etc. are required.
3) There can be a maximum of 2 operators in conditional statements with proper spaces.

Output Pattern:

The output contains a text file that consists of enumeration of the Verilog code i.e. the text will be helpful to the users who cannot understand the Verilog syntax.
