SIS1100-e/3104

User Manual

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Revision Table:

Revision	Date	Modification
0.01	01.10.08	Generated from sis3100
1.00	19.11.08	Initial Release
1.01	20.11.08	Fix in jumper description
1.02	16.07.09	System Clock bug fix/remove references to no longer existing SIS3100 J10 and J90
1.03	18.08.09	Firmware modifications for SIS3100 compatibility Firmware 0201 (1G Link) and 0x0221 (2G Link) Introduce firmware change table
1.04	27.02.12	Firmware support for 1G/2G autobaud (0x0302)

1 Table of contents

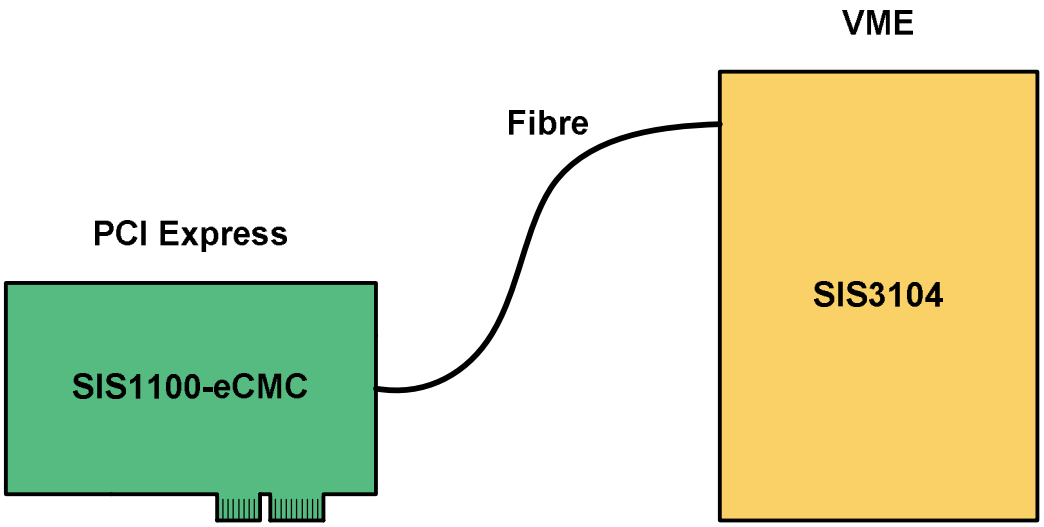
2 Introduction

The original SIS1100/3100 PCI to VME interface started shipping in 2001. It was developed to match the requirements of Particle Physics experiments, related applications and other demanding data acquisition systems. The wish for electrical decoupling resulted in the selection of a fibre optic Gigabit solution as the interconnecting technology.
The Compact PCI (cPCI) and 3,3V (and later universal) versions of the SIS1100 were added over the following years.
The introduction of PCI Express was followed by the development of the single lane PCI Express SIS1100-eCMC board, which is now complemented by the SIS3104 VME sequencer card. The SIS1100-eCMC and the SIS3104 are equipped with 1x/2x/4x SFF GBit link media. This allows for interoperate ability of SIS1100-eCMC on the PC side with SIS3100 on the VME side as well as SIS1100 on the PC side with SIS3104 on the VME side with corresponding firmware designs. The block transfer VME data throughput to PC memory is nearly doubled to some 160 MByte/s with the SIS1100-eCMC/3104 combination compared to the SIS1100/3100 (with a slave like the SIS3350 500 MS/s digitizer e.g.)
As we are aware, that no manual is perfect, we appreciate your feedback and will try to incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.html. A list of available firmware designs can be retrieved from http://www.struck.de/sis3104firm.html

Note: The SIS1100/3100 PCI to VME interface was developed in a collaborative effort between the ZEL department of the Research Center Jülich and SIS GmbH.

3 Overview

The SIS PCI Express to VME interface consists of the SIS1100-eCMC PCI Express card and the SIS3104 VME list sequencer and an interconnecting link fibre.



Photograph of SIS1100-eCMC and SIS3104

3.1 Design Concept of the SIS3104 VME side

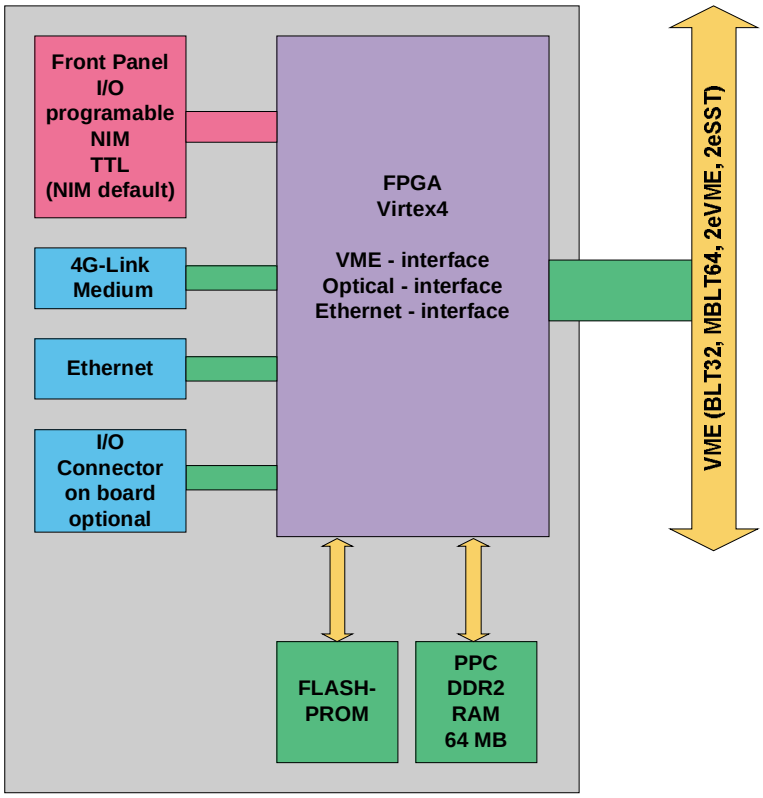
Find below a list of key features of the SIS3104.

- VME List sequencer
- VME Master: A16/A24/A32 D8/D16/D32/BLT32/MBLT64/2eMBLT64/2eSST-160 2eSST-267 and 2eSST-320
- Block transfer address auto increment on/off (for FIFO reads)
- System controller function (can be disabled by DIP switch)
- Hot swap (in conjunction with VME64x backplane)
- VME64x Connectors
- VME64x Side Shielding
- VME64x Front panel
- VME64x extractor handles (on request)
- Standard VME supply voltages (+5 V, -12V)

Possible future firmware extentions comprise

- Ethernet connectivity
- VME slave memory access
- Power PC (PPC) as list processor

A block diagram of the SIS3104 is shown below.

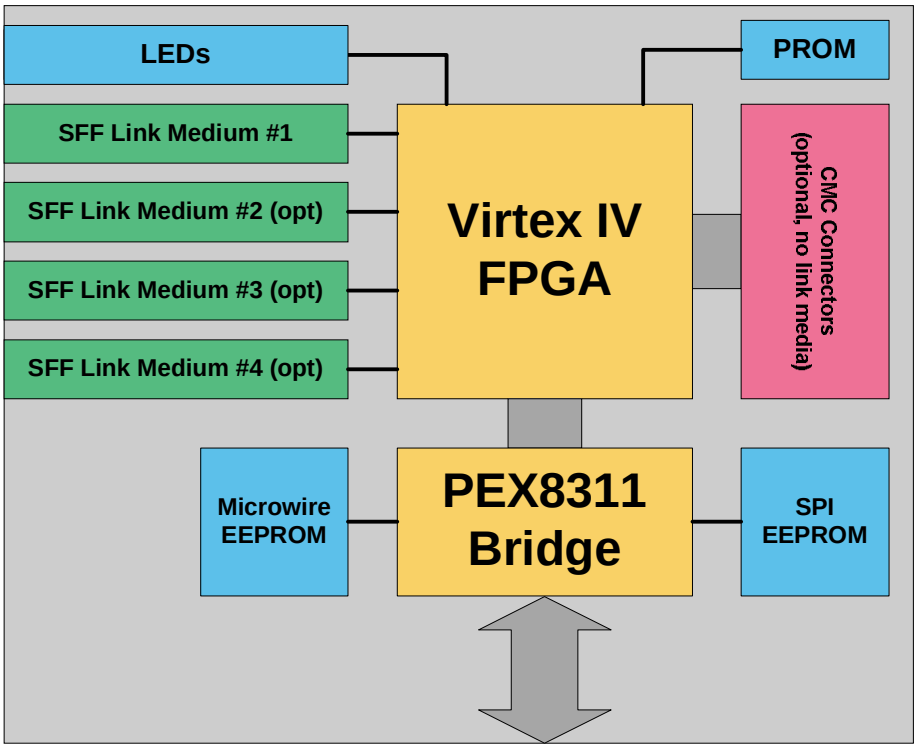


SIS3104 block diagram

3.2 Design concept of PCI Express side (SIS1100-eCMC)

A PLX Technology PEX8311 PCI Express to local bus interface chip, which is PCI Express Specification r1.0a compliant, is used as the interfacing hardware. The single lane PCI express implementation yields a bandwidth in the 160 MByte/s ballpark.

- PCI Express Specification r1.0a compliant
- Virtex IV protocol/link FPGA
- serial configuration PROMs for FPGA and PLX bridge
- JTAG port to serial PROM and FPGA (can be routed to CMC site)
- CMC (IEEE P1386 Draft 2.3) single size carrier (w/o installed link media)
- all CMC data lines routed to FPGA



Block diagram of SIS1100-eCMC

4 Gigabit Hardware

Small form factor (SFF) Gigabit link media were chosen as the physical layer of the link of the SIS PCI(e) to VME interface family. Media with LC connectors are used, patch fibres to other standards like ST are readily available for large scale connections through 19" patch fields. More recent designs like the SIS1100-eCMC and the SIS3104 boards have switchable link media which can be operated at up to 4 Gigabit/s link speed. The link is clocked at 125 MHz in the one Gigabit case (i.e. a 62.5 MHz clock is doubled by a delay locked loop in the protocol XILINX FPGA), what results in a payload of 125 Mbytes/s. With the standard multimode link media distances of up to 450 m can be covered, single mode media and fibres extend the range up to 80 km. Due to pipelining single cycle and high speed block transfer capabilities link latency will not play a significant role for most applications even at very long distances.

5 Gigabit-Link Transfer Protocol

32-bit words are transmitted over the Gigabit-Link. Loss of synchronisation or errors are reported to the corresponding host. Any transmission starts with a special word, in the case of a block transfer it can end with a special character also if the transfer length is undefined or smaller than the requested length.

One bit in the FIFOs is used to flag a special word, with Byte 0 being 0x1C (SC_PROT K28.0).
Byte loss can be detected as all 4 Bytes of a word are transmitted without interruption. All characters up to the next special character are ignored if the data link layer detects an error.

A detailed description of the implemented protocol can be found in the document gigalinkenglish PDF in the SIS1100/310x directory on the SIS product DVD.
The protocol is handled by the driver and typically you will not want to deal with it unless you look into porting the driver to another platform or extending the functionality.

6 Software/Getting started

For most applications it will be good enough to install driver and example software and to run accompanying example code to get started with the interface without dealing with the details of the hardware registers. The supported software platforms are Windows (tested with Windows 2000, XP and Vista) and LINUX.
The documentation and the software can be found on the accompanying DVD in the sis1100310x directory.

6.1 Hardware installation

Power down both the PC and the VME crate to install the SIS1100 and SIS3104 cards and observe electrostatic precautions during installation. The optical fiber has to be handled with care and a minimum bending radius of 5 cm has to be obeyed.

6.2 Windows

The Windows DLLs are based on the PLX Technology API.

At this point in time example code is available for

- Labwindows CVI
- Labview
- VisualC++

The Windows code resides in the driver/win directory

6.3 LINUX

The LINUX driver is supported by Dr. Peter Wüstner from the ZEL department of the research center Jüclich (FZ Jülich) in the context of the Struck-FZ Jülich co-operation of the original SIS1100-SIS3100 development.

The LINUX code resides in the driver/LINUX directory

7 SIS3104 Access through the Optical Interface

7.1 Control register space

Offset	Access	Function
0x000	R	Type-Identifier/Version register
0x004	R/W	Optical Status register
0x008	R/W	Optical Control register (reserved functions)
0x080	R/W	OPT-IN/OUT Register (FLAT/LEMO I/O)
0x084	R/W	OPT-IN-LATCH_IRQ Register
0x088	R/W	LEMO IO level control register
0x100	R/W	OPT-VME-Master Status/Control register
0x104	R/W	OPT-VME-Master Interrupt Status/Control register

Control register space can be accessed with the routines:

```
int s3100_control_read(int p, int offset, u_int32_t* data)
int s3100_control_write(int p, int offset, u_int32_t data)
```

Note: long word access, the offset has to be long word aligned (0x0, 0x4, 0x8 ...)

7.1.1 Type-Identifier/Version register(0x0, read)

This read only register holds information on the SIS3104 firmware version, hardware version and the identifier. The identifier allows for a distinction between different interface types. It is 2 for VME controllers.
Find below a table with the bit assignments of the register and a list of identifiers.

BIT	access	Name	Function
31-24 FF000000	RO	Firmware Version	1..255
23-16 00FF0000	RO	Firmware Id.	1 = universal other Ids. for dedicated firmware
15-8 0000FF00	RO	Hardware Version	1..255
7-0 000000FF	RO	Identifier 0x02	1 = PCI(e)/PLX Interface (SIS1100) 2 = VME Controller (SIS3100/SIS3104) 3 = CAMAC Controller (SIS5100) 4 = LVDS Readout system 5 = Pandapixel

Example: The initial version of the SIS3104 reads 0x 01 01 02 02

7.1.2 Optical status register (0x4, r/w)

BIT	Name	access	Function
31-16 FFFF0000	reserved	RO	0x0000
15 00008000	BAND_ERROR	WR: sel clr	VSC: Out-of-Band Error (not reseted after powerup and Link reset)
14 00004000	DISPAR_ERROR	WR: sel clr	VSC: Disparity Error (not reseted after powerup and Link reset)
13 00002000	UORUN_ERROR	WR: sel clr	VSC: Under/Overrun error (not reseted after powerup and Link reset)
12 00001000	TBERR_ERROR	WR: sel clr	VSC: Transmit Buffer Error(not reseted after powerup and Link reset)
11 00000800			0
10 00000400	LWORD_ERROR	WR: sel clr	Lword aligned error on optical interface
9 00000200			0
8 00000100	LINKSPEED	R	0 - 1G; 1 - 2G
7 00000080	REC_VIOLATION		0 (reserved)
6 00000040	SEMA_CHG		0 (reserved)
5 00000020	INH_CHG	WR: sel clr	INHIBIT signal has changed (to inhibit)
4 00000010	SYNCH_CHG	WR: sel clr	RX/TX_SYNCH has changed
3 00000008	CONFIGURED	RO	allows remote side to detect RESET or power up (1 after reset or power up)
2 00000004	INHIBIT	RO	Transfer to remote side locked (TRANS_WAIT_FLAG_L) remote has send xoff or TRANSMIT_LINK_WAIT is active
1 00000002	TX_SYNCH	RO	Optical remote receiver is synchronised (TRANSMIT_LINK_OK)
0 00000001	RX_SYNCH	RO	Optical receiver is synchronised (RECEIVE_LINK_OK)

7.1.3 Optical control register (0x8, r/w)

This register is implemented as a selective J/K register. The user has to avoid writing a 1 to the clear and set bit of the same output at the same time, as an undefined toggle state may result.
The functions are reserved. They will be used in applications like VME to VME coupling.

Bit	Write Function	Read Function
31:16	Clear reserved bit [15:0]	0x0000
15:0	Set reserved bit [15:0]	Status reserved bit [15:0]

7.1.4 OPT-IN/OUT Register (0x80,read /write)

On read access the status of the outputs and the current level on the inputs can be obtained, on write access the level of the outputs can be set. The register is implemented as a selective J/K register, the specific function (set/clear output) is executed by writing a 1 to the corresponding bit location, writes with a 0 have no effect. The user has to avoid to write a 1 to the clear and set bit of the same output at the same time, as an undefined toggle state may result.

Bit	Write Function	Read Function
31	no function	0
30	no function	0
29	no function	0
28	no function	0
27	Generate pulse TTL Output 2	0
26	Generate pulse TTL Output 1	0
25	Generate pulse NIM Output 2	0
24	Generate pulse NIM Output 1	0
23	no function	0
22	no function	0
21	no function	0
20	no function	0
19	Clear TTL Output 2	Status TTL Input 2
18	Clear TTL Output 1	Status TTL Input 1
17	Clear NIM Output 2	Status NIM Input 2
16	Clear NIM Output 1	Status NIM Input 1
15	no function	0
14	no function	0
13	no function	0
12	no function	0
11	no function	0
10	no function	0
9	no function	0
8	no function	0
7	no function	0
6	no function	0
5	no function	0
4	no function	0
3	Set TTL Output 2	Status TTL Output 2
2	Set TTL Output 1	Status TTL Output 1
1	Set NIM Output 2	Status NIM Output 2
0	Set NIM Output 1	Status NIM Output 1

Note 1: the pulse length is approximately 32 ns
Note 2: The pulse polarity can be inverted by setting the corresponding output bit
Note 3: Whether an in/output is addressed/seen under NIM or TTL depends on the setting of JP123/JP133 and/or the setting of the LEMO IO level control register.

7.1.5 OPT-IN-LATCH_IRQ Register (0x84,read /write)

The register controls front panel input interrupt generation and allows reading the current and the latched status of the inputs.
On read access you can obtain the current level on the inputs and the latched status. On write access interrupts for the inputs can be enabled and disabled and the latched input status can be cleared. The register is implemented as a selective J/K register, the specific function (enable/disable IRQ source) is executed by writing a 1 to the corresponding bit location, writes with a 0 have no effect. The user has to avoid writing a 1 to the clear and set bit of the same output at the same time, as an undefined toggle state may result.

Bit	Write Function	Read Function	
31	no function	0	Doorbell
30	no function	0	
29	no function	0	
28	no function	0	
27	Clear TTL Input 2 LATCH bit	TTL Input 2 LATCH bit	
26	Clear TTL Input 1 LATCH bit	TTL Input 1 LATCH bit	
25	Clear NIM Input 2 LATCH bit	NIM Input 2 LATCH bit	
24	Clear NIM Input 1 LATCH bit	NIM Input 1 LATCH bit	
23	no function	0	
22	no function	0	
21	no function	0	
20	no function	0	
19	TTL Input 2 IRQ diable bit	Status TTL Input 2	
18	TTL Input 1 IRQ disable bit	Status TTL Input 1	
17	NIM Input 2 IRQ disable bit	Status NIM Input 2	
16	NIM Input 1 IRQ disable bit	Status NIM Input 1	
15	1 Shot: IRQ_UPDATE	0	
14	no function	0	
13	no function	0	
12	no function	0	
11	no function	0	
10	no function	0	
9	no function	0	
8	no function	0	
7	no function	0	
6	no function	0	
5	no function	0	
4	no function	0	
3	TTL Input 2 IRQ enable bit	Status TTL Input 2 IRQ Enable bit	
2	TTL Input 1 IRQ enable bit	Status TTL Input 1 IRQ Enable bit	
1	NIM Input 2 IRQ enable bit	Status NIM Input 2 IRQ Enable bit	
0	NIM Input 1 IRQ enable bit	Status NIM Input 1 IRQ Enable bit	

for PCI-Doorbell IRQ generation see 6.1.7 OPT-VME-Interrupt Status/Control register (0x104,read /write)

Note: Whether an input is addressed/seen under NIM or TTL depends on the setting of JP123 and/or the setting of the LEMO IO level control register.

7.1.6 LEMO IO level control register (0x88,read/write)

The register is implemented in a J/K fashion also and allows to check the status of the logic level setting of the front panel inputs and outputs. In addition it can be used to control the levels by software. Please note, that the actual control over the status of the inputs and outputs is controlled via the LEMO I/O register

Bit	Write Function	Read Function/value
31	Disable Software Level Control (*)	0
30	unused	0
29	…	0
28	unused	0
27	unused	0
26	…	0
25	…	0
24	unused	0
23	unused	0
22	…	0
21	…	0
20	unused	0
19	Set input 2 to NIM level (*)	0
18	Set input 1 to NIM level (*)	0
17	Set output 2 to NIM level (*)	0
16	Set output 1 to NIM level (*)	0
15	Enable Software Level Control	Status Software Level Control
14	unused	0
13	…	0
12	unused	0
11	unused	0
10	…	0
9	…	0
8	unused	0
7	unused	0
6	…	0
5	…	0
4	unused	0
3	Set input 2 to TTL level	Status of level input 2 (0=NIM, 1=TTL)
2	Set input 1 to TTL level	Status of level input 1 (0=NIM, 1=TTL)
1	Set output 2 to TTL level	Status of level output 2 (0=NIM, 1=TTL)
0	Set output 1 to TTL level	Status of level output 1 (0=NIM, 1=TTL)

The power up value is 0x00000000 (with the I/Os jumper configured to NIM level)

(*) denotes the power up default setting
Note 1: Enable software control by setting bit 15 to gain software control over the logic levels of the I/Os. By default the level is defined by jumpers JP123 and JP133

Note 2: for the typical application it will be good enough to set the logic levels to the desired levels in hardware by setting JP123 and JP133 accordingly.

7.1.7 OPT-VME-Master Status/Control register (0x100,read/write)

The control register is in charge of the control of most of the basic properties of the SIS3100 board in write access. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which location is 16-bit higher in the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time.

Bit	Write Function	Read Function
31	Clear SYSTEM VME BERR TIMER BIT1	0
30	Clear SYSTEM VME BERR TIMER BIT0	0
29	Clear LONG TIMER BIT1	0
28	Clear LONG TIMER BIT0	0
27	no function	0
26	Clear Force Dearbit	0
25	Disable System Controller BERR Info	0
24	Disable VME retry	0
23	no function	0
22	Clear VME REQUESTER TYPE BIT	0
21	Clear VME_REQ_LEVEL BIT1	0
20	Clear VME_REQ_LEVEL BIT0	0
19	Clear POWER_ON_RESET bit	0
18	Clear LEMO_OUT_RESET bit	0
17	Clear VME_SYSRESET bit	0
16	Clear VME System Controller Enable bit	Status VME System Controller (*2)
15	Set SYSTEM VME BERR TIMER BIT1	Status SYSTEM VME BERR TIMER BIT1
14	Set SYSTEM VME BERR TIMER BIT0	Status SYSTEM VME BERR TIMER BIT0
13	Set LONG TIMER BIT1	Status LONG TIMER BIT1
12	Set LONG TIMER BIT0	Status LONG TIMER BIT0
11	Enable System Controller BERR Info (*6)	Status System Controller BERR Info
10	Set Force Dearbit (*5)	0
9	no function	0
8	Enable VME retry (*4)	Status VME retry
7	no function	0
6	Set VME REQUESTER TYPE BIT	Status VME REQUESTER TYPE BIT
5	Set VME_REQ_LEVEL BIT1	Status VME_REQ_LEVEL BIT1
4	Set VME_REQ_LEVEL BIT0	Status VME_REQ_LEVEL BIT0
3	no function	0
2	no function	0
1	Set VME_SYSRESET bit (*3)	Status VME_SYSRESET bit
0	Set VME System Controller Enable bit (*1)	Status VME System Controller Enable bit

The power up value is 0x0000C100 (may depend on the SIS3104 firmware version)

Notes:

(*1) is ored with switch 5 of SW80; Caution: if the jumper is not installed and the VME system controller functionality is enabled by software, the 16 MHz clock is not active during power up. This may result in problems with peculiar VME slave designs that use the VME clock to initialise on board logic.
(*2) is set with switch 5 of SW80 on or if VME System Controller Enable bit is set
(*3) if switch 6 of SW80 is in on position and the VME_SYSRESET bit is set then VME_SYSRESET is issued at power up

(*4) A retry error (error code 0x212) may be caused by older VME backplanes, which do not properly terminate this previously reserved (pin B3 on connector P2) if retry is enabled. Retry can be disabled by setting bit 24. Retry had to be activated by setting bit 8 on the SIS3100, this behaviour is not compatible with SST transfers.
(*5) Setting bit 10 causes the SIS3104 to release busy for 170 ns in between of blockletts during a block transfer. This gives another master the possibility to gain busmastership during the block transfer. The SIS3104 will terminate the block transfer with an arbitration timeout if the other master does not release busmastership within the long timer period. The AS-AS gap of 90 ns will be extended by the 170 ns release period, i.e. the reduction in transfer speed is negligible.
(*6) Setting bit 11 allows for distinction of the bus error source if the SIS3104 is system controller. This functionality is useful to distinguish between a transfer that is terminated with a bus error by a slave and a transfer terminated with a bus error originating from the system controller timeout.

Error Code	Condition
0x211	Bus error but no SYS_BERR (with bit 11 set)
	Any bus error (with bit 11 not set, identical to SIS3100)
0x219	Bus error generated by SYS_BERR (with bit 11 set)

SYSTEM VME BERR TIMER BIT1	SYSTEM VME BERR TIMER BIT0	VME Bus Error after
0	0	1,25 µs
0	1	6,25 µs
1	0	12,5 µs
1	1	100 µs (default)

Note: The default value of 100 µs will be fine with all VME slaves on the market, you may want to use a shorter value for your system however. Be aware, that driver software may change the default setting during the initialization phase. The bus error code is 0x211.

LONG TIMER BIT1	LONG TIMER BIT0	LONG Timeout after
0	0	1 ms (default)
0	1	10 ms
1	0	50 ms
1	1	100 ms

LONG Timeout: arbitration timeout, no reply from current VME master or VME bus mastership not granted
The arbitration timeout error code is ox214.

VME_REQ_LEVEL BIT1	VME_REQ_LEVEL BIT0	VME Bus Request Level
0	0	BR3 (highest Level, default)
0	1	BR2
1	0	BR1
1	1	BR0

VME REQUESTER TYPE BIT	VME Bus Requester Type
0	Release on Request (default)
1	Release when Done

7.1.8 OPT-VME Interrupt Status/Control register (0x104,read /write)

The VME interrupts are enabled with their corresponding bit in this register. In addition the user can check on the status of the interrupt sources.

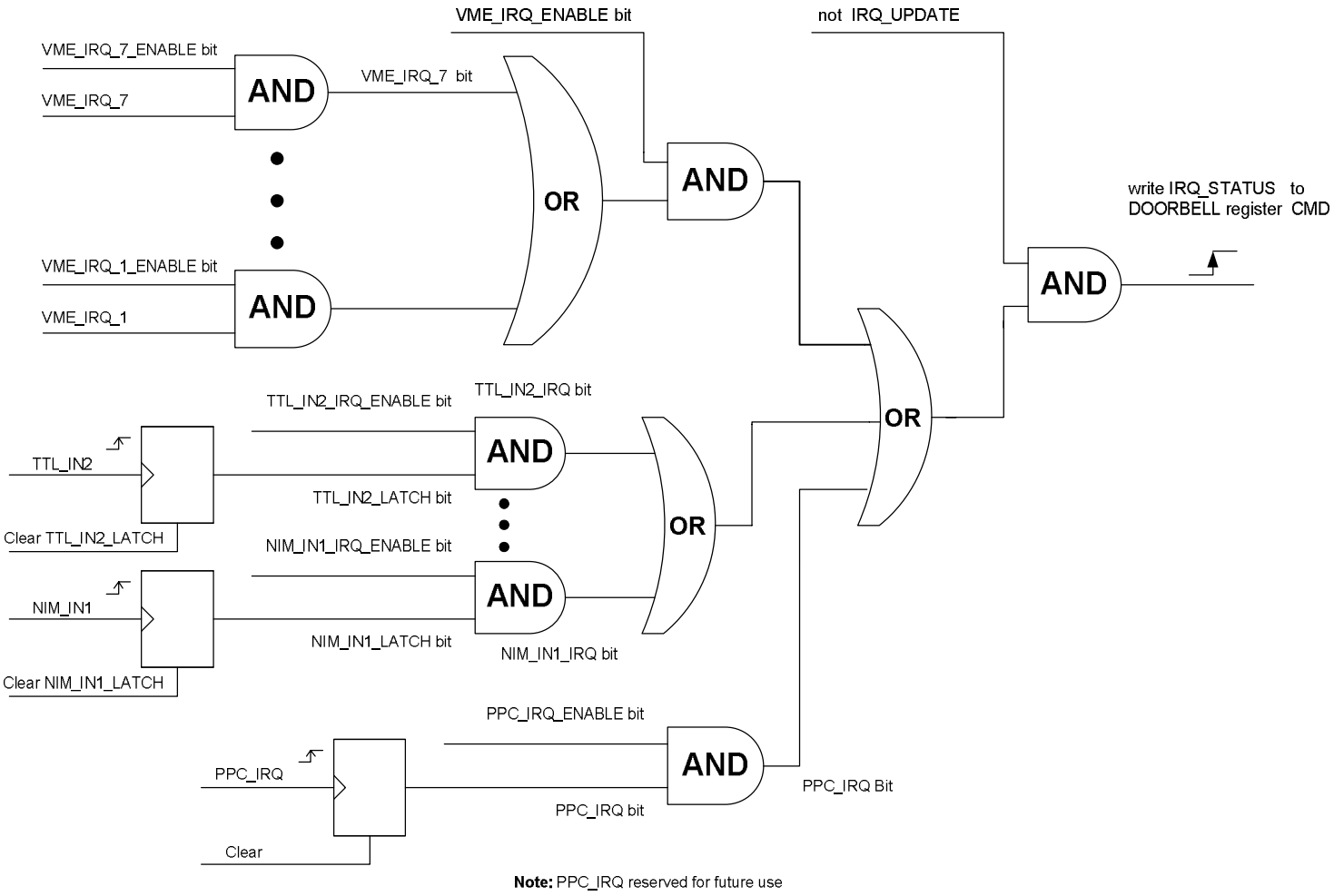
Bit	Write Function	Read Function
31		Status VME IRQ 7 on VME BUS
30		Status VME IRQ 6 on VME BUS
29		Status VME IRQ 5 on VME BUS
28		Status VME IRQ 4 on VME BUS
27		Status VME IRQ 3 on VME BUS
26		Status VME IRQ 2 on VME BUS
25		Status VME IRQ 1 on VME BUS
24		
23	Clear VME IRQ 7 Enable Bit	Status VME IRQ 7 bit
22	Clear VME IRQ 6 Enable Bit	Status VME IRQ 6 bit
21	Clear VME IRQ 5 Enable Bit	Status VME IRQ 5 bit
20	Clear VME IRQ 4 Enable Bit	Status VME IRQ 4 bit
19	Clear VME IRQ 3 Enable Bit	Status VME IRQ 3 bit
18	Clear VME IRQ 2 Enable Bit	Status VME IRQ 2 bit
17	Clear VME IRQ 1 Enable Bit	Status VME IRQ 1 bit
16	Clear VME IRQ Enable Bit	0
15	1 Shot: IRQ_UPDATE	0
4		0
13		0
12		0
11		0
10		0
9		0
8		0
7	Set VME IRQ 7 Enable Bit	Status VME IRQ 7 Enable Bit
6	Set VME IRQ 6 Enable Bit	Status VME IRQ 6 Enable Bit
5	Set VME IRQ 5 Enable Bit	Status VME IRQ 5 Enable Bit
4	Set VME IRQ 4 Enable Bit	Status VME IRQ 4 Enable Bit
3	Set VME IRQ 3 Enable Bit	Status VME IRQ 3 Enable Bit
2	Set VME IRQ 2 Enable Bit	Status VME IRQ 2 Enable Bit
1	Set VME IRQ 1 Enable Bit	Status VME IRQ 1 Enable Bit
0	Set VME IRQ Enable Bit	Status VME IRQ Enable Bit

The power up default value reads 0x 00000000

Status internal VME IRQ 1 = Status VME IRQ 1 Enable Bit and Status VME IRQ 1 on VME BUS
Status VME IRQ 1 = Status internal VME IRQ 1

PCI-Doorbell:
The leading edge of an IRQ issues an optical request, which writes the IRQ status in the doorbell register of the PLX PCI bridge chip.
With the command "IRQ_UPDATE " (write 0x8000 to `OPT-IN-LATCH_IRQ Register` or to `OPT-VME-Interrupt Status/Control register)` a pending IRQ is disabled shortly (if more than one IRQs are pending) what results in another leading edge generated by the other pending IRQ with consecutive doorbell register update.

Doorbell register bit	Function
31:16	0 (reserved)
15	Status DSP_IRQ
14	Status LEMO_ IN3_IRQ latch bit
13	Status LEMO_ IN2_IRQ latch bit
12	Status LEMO_ IN1_IRQ latch bit
11	Status FLAT_ IN4_IRQ latch bit
10	Status FLAT_ IN3_IRQ latch bit
9	Status FLAT_ IN2_IRQ latch bit
8	Status FLAT_ IN1_IRQ latch bit
7	Status VME IRQ 7 bit
6	Status VME IRQ 6 bit
5	Status VME IRQ 5 bit
4	Status VME IRQ 4 bit
3	Status VME IRQ 3 bit
2	Status VME IRQ 2 bit
1	Status VME IRQ 1 bit
0	0 (reserved)



SIS3104 PCI Doorbell IRQ block diagram

7.1.9 OPT-VME-Master DMA_WRITE_BYTE_counter register (0x204,read)

This register holds the counter of written Bytes upon a bus error terminated block transfer write cycle. . It is cleared with the start of a block transfer write cycle.

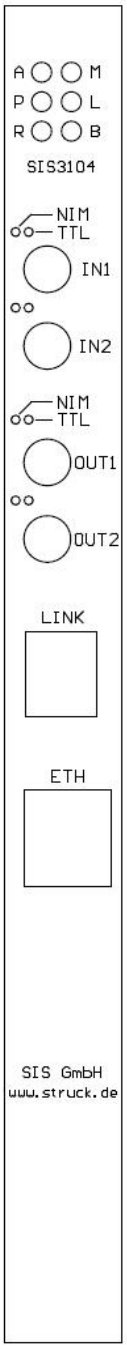
Bit	Function
31	0
30	0
29	Byte counter bit 29
...	
0	Byte counter bit 0

8 VME slave access (future option)

The SIS3104 has 64 MBytes of DDR II SDRAM memory.
The memory can be used as memory for the Power PC in the FPGA and/or as VME slave.
Both options are possible extensions for future firmware implementations.

9 SIS3104 front panel elements

The aluminium part (without mounting fixtures) of the SIS3104 is shown below.



9.1.1 Front panel LEDs

The six LEDs close to the top of the SIS3104 have the following function.

LED	Color	Description
A	Yellow	VME access to VME slave port of SIS3104 (future option)
M	Yellow	VME master, lit whenever the SIS3104 accesses the VME bus
P	Red	Power, signals presence of +5 V supply voltage
L	Red	Link up, lit when connection to PCI side (or loopback connection) is established
R	Green	Ready, lit when on board logic is configured (off during power up LED self test)
B	Green	BERR Bus Error

During power up self test and FPGA configuration all LEDs except the Ready (R) LED are on. After the initialisation phase is completed, all LEDs except the Ready (R) LED and the Power (P) have to go off. The status of the L LED depends on the status of the optical link. Starting with the 0302 firmware version, the L LED will represent the negotiated linkspeed during the first 10 seconds after establishing the link. A linkspeed of 1Gb results in a 1Hz blinking frequency. A linkspeed of 2Gb results in a blinking frequency of 4Hz. Differing behaviour indicates either a problem with the download of the firmware boot file, the FPGA, the download logic or the power circuitry.

Four pairs of green surface mounted LEDs are used to indicate the logic level of the front panel inputs and outputs.

Lit LED	Description	
NIM	In/output set to NIM level	
	logic state	voltage
	0	0 V
	1	< -0.8 V
TTL	In/output set to TTL level	
	logic state	voltage
	0	< 0.7 V
	1	> 2.4 V

Note 1: the factory default power up logic level is NIM: The input default levels can be set on JP123, the default output levels on JP133. In addition the logic level can be set in the LEMO IO control register

Note 2: the inputs are factory terminated with 50 Ω, the outputs drive a load of 50 Ω

10 PCB LEDs

Surface mounted red LEDs are used to signal power status and Ethernet link information.
A table with the SMD LEDs is given below.

Designator	Function
D128A	Ethernet Link 10Mbit
D300A	Power D+2.5V
D301A	Power D+3.3V
D309A	Power_Sequence_OK
D309B	Power_Fault_Sequencer
D400A	Power D+12V
D410A	Power D-12V
D500B	Power D+1,8V
D600B	Power D+1,2V

10.1 Fuses

The SIS3104 card is powered through 3 SMD fuses. The 3.3, 2.5, 1.8 and 1.2 V voltages are generated from the 5V supply.

Designator	Fusing	Current	Littelfuse Part number	Struck Part number
F1	+5V	7A	R451007MRL	00064
F3	+12V	2A	R451002MRL	00063
F4	-12V	2A	R451002MRL	00063

11 SIS3104 Jumpers, Switches and Connectors

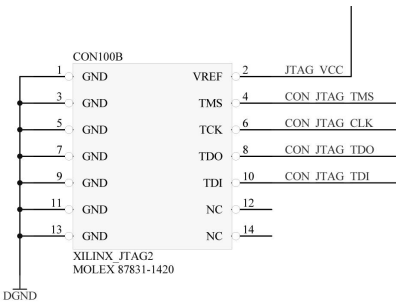
The SIS3104 card has three jumper arrays, one DIP switch, 2 rotary switches and a pin header connector. SW80 controls VME slave port access. A more detailed description of the two arrays and their factory default settings is given in the tables below.

11.1 CON100B JTAG

The SIS3104's on board logic can load its firmware from a serial PROMs or via the JTAG port on connector CON100B

Hardware like the HW-USB-II-G-JTAG in connection with the appropriate software will be required for in field JTAG firmware upgrades. The JTAG chain configuration is selected with jumper JP101.

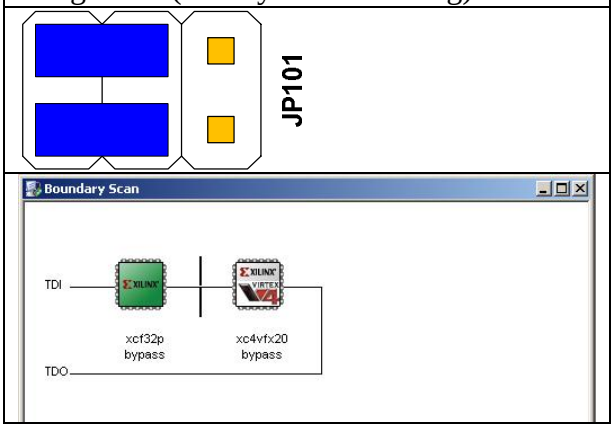
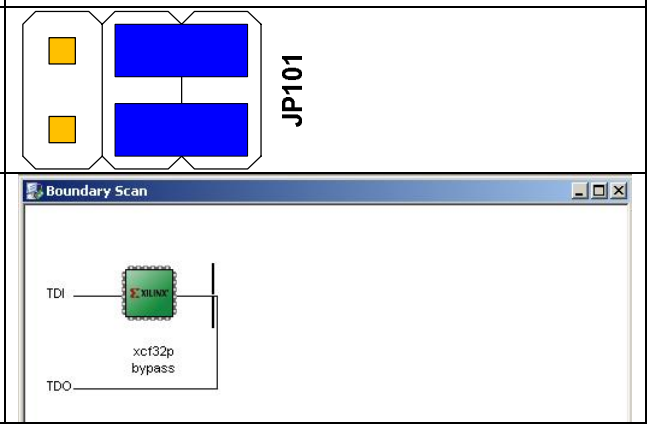
CON100B is a 2mm (i.e. metric) 14 pin header that allows you to reprogram the firmware of the SIS3104 board with a JTAG programmer. The pinout is shown in the schematic below. It is compatible with the cable that comes with the XILINX HW-USB-II-G-JTAG platform cable.



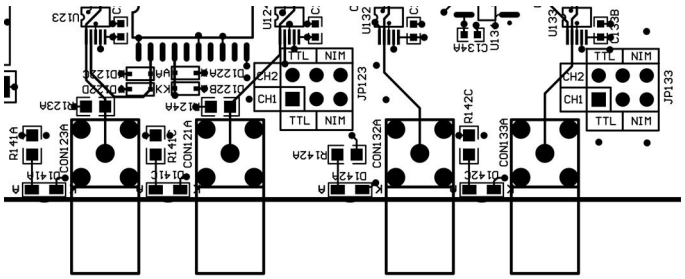
Note: The board has to be powered for reprogramming over JTAG

11.2 JP101 JTAG Chain Configuration

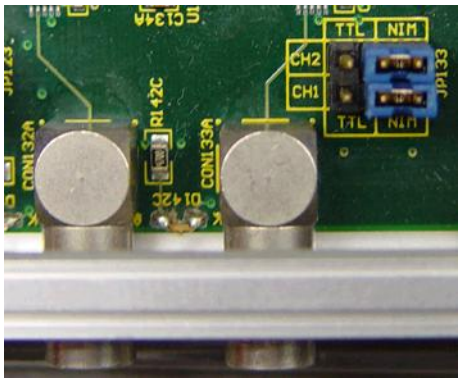
You can switch between the JTAG chain with serial RPOM and FPGA (long chain) and the chain with the FPGA connected only (short chain) with jumper JP101 as illustrated below.

Long chain (factory default setting):	Short chain:
	

11.3 JP123 LEMO input, JP133 LEMO output logic level



Example: JP133 both outputs configured for NIM (i.e. at factory default setting)

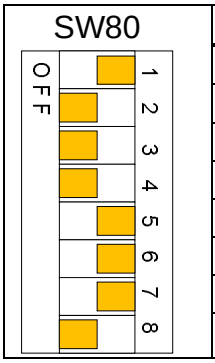


11.4 SW1/SW2 VME Slave Address (future feature)

The two rotary hexadecimal rotary encoders SW1 and SW2 are used to define the VME slave address. The function depends on the setting of switch SW80 also.

11.5 SW80 Dip switch System Controller/Reset Behavior/Slave Addressing

The 8 switches of SW80 are in charge of system controller function, reset behaviour and slave addressing as listed in the table below. Factory default settings are illustrated on the left hand side of the table.



Function
EN_A32 reserved for future slave use
EN_A16 reserved for future slave use
EN_GEO reserved for future slave use
EN_VIPA reserved for future slave use
System controller enable
Connect FPGA reset to VME SYSRESET
Watchdog enable
Connect VME SYSRESET to FPGA reset

Note 1: do not set switch 6 and 8 to the on position at the same time (deadlock). The recommended setting is switch 6 on/8 off for a master/system controller and switch 6 off/8 on for non system controller units.

Note 2: switch off position 7 (watchdog enable) for firmware upgrades

12 VME master/system controller

12.1 Multi master operation

VME is a multi master system, what allows you to use several SIS3104 modules or a mixture of SIS3104 VME sequencers and other VME master hardware in one crate. The sections below have to be taken into account for successful multi master operation.

12.1.1 System Controller

The SIS3104 can act as VME system controller. The 16 MHz VME system clock is generated by the SMD oscillator U10. and enabled/disabled by switch 5 of switch array SW80.
Make sure not to have more than one system controller on the VME backplane. The system controller has to be the leftmost master in the crate (typically it will reside in slot 1). In the case of the SIS3104 the system controller is enabled/disabled with switch 5 of SW80 . SIS3100 system controller functionality can also be enabled/disabled via the OP-VME control register. The system controller on/off status is an OR of the control register setting and the jumper and can be read back from the status register. The factory default is system controller enabled (as most SIS3104 cards are used in a single master environment.

Note: A VME diagnosis module like the VDIS or a measurement with a VME bus extender can be used to check, whether a particular CPU or interface generates system clock (with all other interfaces/CPUs unplugged from the VME backplane. Some VME slave modules may use the system clock to initialize on board resources, this mechanism may fail if the system clock is generated by more than one board in the crate. The system clock can also be activated by software if the switch is in off position. In this case the user has to be aware, that no SYSCLOCK will be generated during the power up phase of the crate. A SYSRESET may be required by certain VME slaves for proper initialization of on board circuitry after SIS3104 SYSCLOCK generation was enabled.

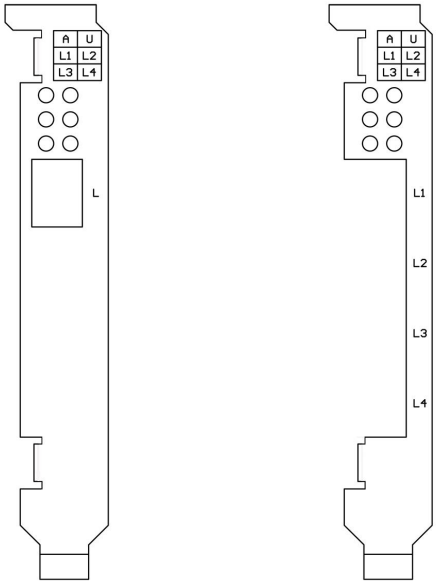
12.1.2 Bus grant/bus mastership

- make sure to set the jumpers on the bus grant (BG) daisy chain properly unless your crate has an automatic daisy chain backplane (refer to the VME specification).
- Make sure, that no VME master locks bus mastership. It may be a good idea to use release when done instead of release on request where possible. It may be necessary to use a higher arbitration timeout than the standard value of 1 ms (selected via the OPT-VME control register).
- use different bus request (BR) levels as needed. The bus request level of the SIS3104 is programmed with the OPT-VME control register. The BR level of the SIS3104 defaults to 3 (highest level)

13 SIS1100-eCMC Hardware Description

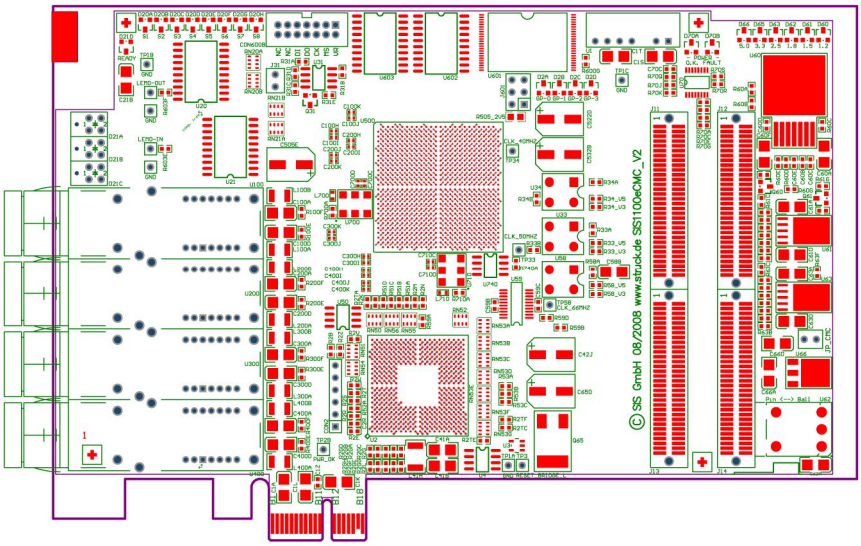
13.1 Front panel

The SIS1100-eCMC uses a standard PCI front panel. The front panel as seen from the rear of the PC is shown in the graph below. The front panel to the left is the version with one link medium, the right hand side shows the four link medium version.



13.2 Board Layout

The silk screen of the SIS1100-eCMC V2 is shown below.



13.3 SIS1100-eCMC LEDs

Several LEDs were implemented to assist debugging in case of problems.

13.3.1 Front panel LEDs

The green front panel LEDs of the board are grouped in 3 rows of 2 LEDs each. Find below a table of the LEDs as seen from the rear of the module.

Left	Right
A	U
L1	L2
L3	L4

The function of the LEDs is explained in a little more detail in the table below.

LED	Function
A=Access	Lit with access to the SIS1100-OPT carrier board
U=User	To be set and cleared under user program control
L1	Signals link connection to SIS3104 or other link partner on link 1
L2	Same as L1 for link 2
L3	Same as L1 for link 3
L4	Same as L1 for link 4

13.3.2 SIS1100-eCMC PCB LEDs

The SIS1100-eCMC carrier has SMD LEDs to visualize part of the board status.
The table below shows the LEDs for hardware Version V2

Designator	Label	Function
D20A…D20H	S1…S8	
D21D	Ready	Lit if FPGA configured
D2A	GP-0	General purpose IO-0 of PEX8311
D2B	GP-1	General purpose IO-1 of PEX8311
D2C	GP-2	General purpose IO-2 of PEX8311
D2D	GP-3	General purpose IO-3 of PEX8311
D70A	Power O.K.	Lit after completion of power up sequence
D70B	Power Fault	Lit if fault condition during power up sequence is detected
D60	1.2	Lit if 1.2V power is on
D61	1.5	Lit if 1.5V power is on
D62	1.8	Lit if 1.8V power is on
D63	2.5	Lit if 2.5V power is on
D65	3.3	Lit if 3.3V power is on
D66	5.0	Lit if 5.0V power is on

Differences in hardware Version V1

Designator	Label	Function
D64	D3.3	Lit if D3.3V power is on
D65	P3.3	Lit if P3.3V power is on

13.4 SIS1100-eCMC Connectors/Jumpers

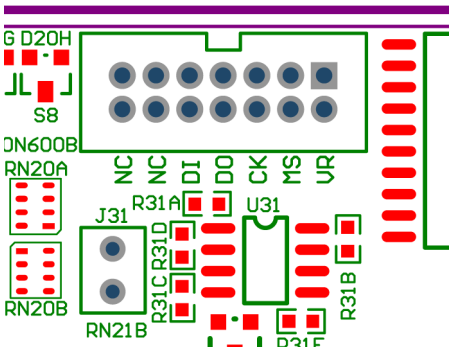
The connectors and jumpers of the SIS1100-eCMC are described in the following subsections.

13.4.1 CON600B JTAG

Same as CON100B JTAG on SIS3104.

13.4.2 J31 Watchdog Reset

J31 can be found next to the JTAG connector CON600B. With J31 closed the boards watchdog reset is connected to the reset logic. J31 should be opened for JTAG firmware programming.



13.4.3 JP_CMC

JP_CMC is stuffed on SIS1100-eCMC boards with CMC connectors only (i.e. cards without optical link media). With JP_CMC closed the JTAG chain is closed on the carrier card, with JP_CMC open the JTAG chain is routed to the CMC connectors.

14 Appendix

14.1 Power consumption

14.1.1 SIS3104

The SIS3104 can be operated in any 6U standard VME crate. The table below lists the required voltages and their respective current.

Voltage	Current
+5 V	1,6 A
-12 V	20 mA

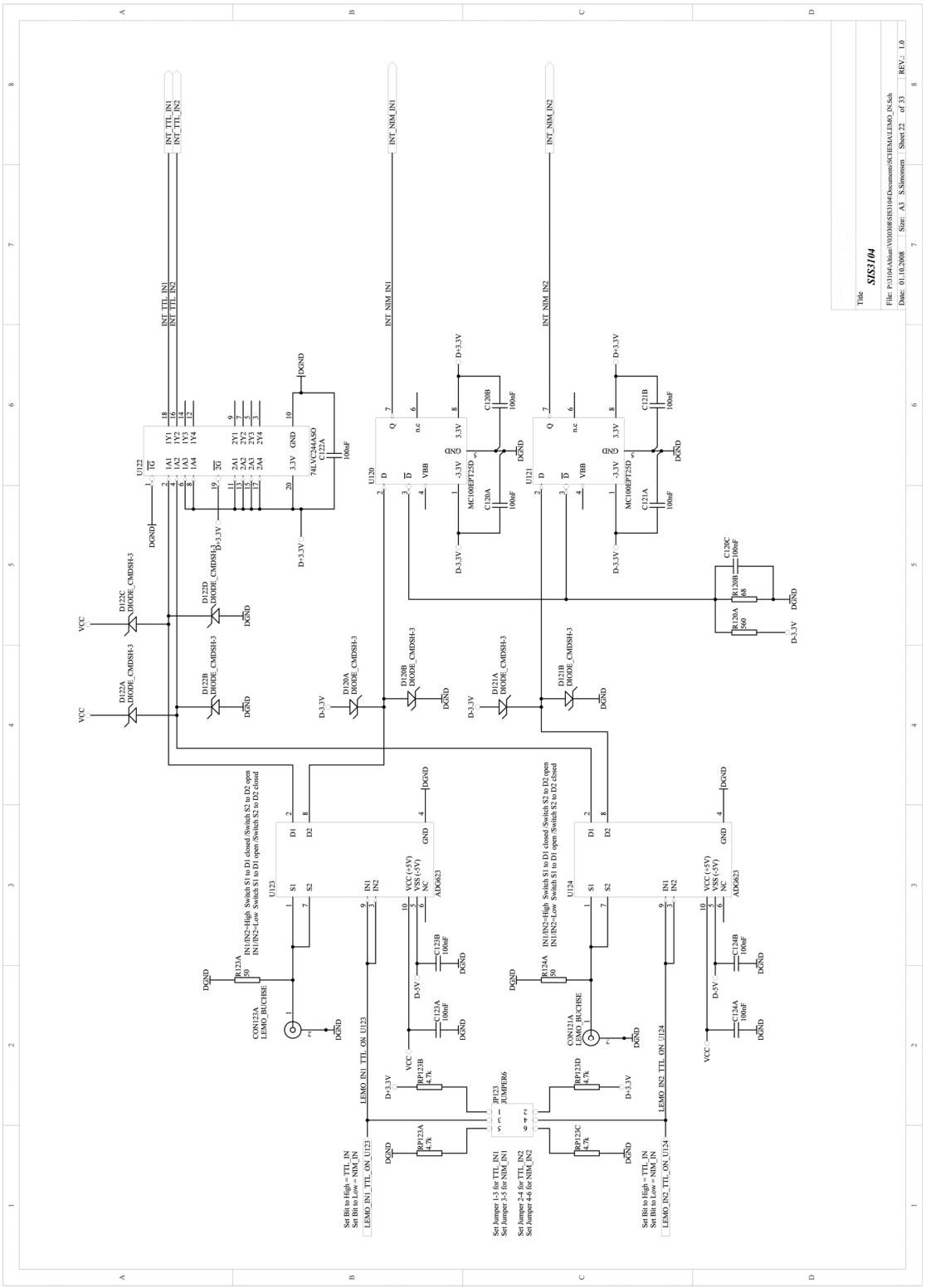
Note: the -12V supply is used for LEMO in/output logic level switch circuitry only

14.1.2 SIS1100-eCMC

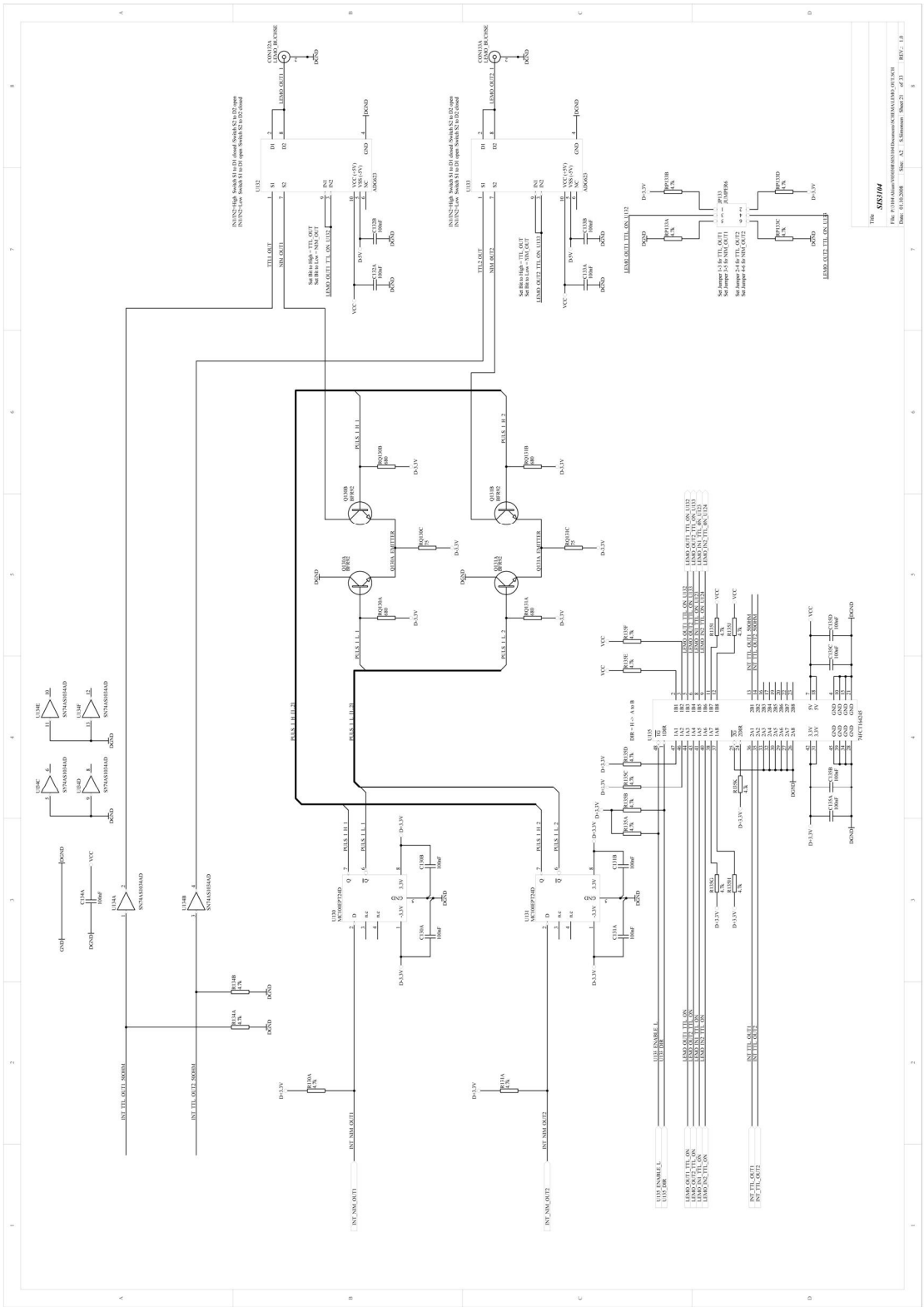
The SIS1100-eCMC V1 power consumption in one link medium configuration is given below.

Voltage	Current
+3,3 V	1,7 A

14.1.3 Schematic of LEMO Input section



14.1.4 Schematic of LEMO Output section



14.2 Connector types

Find below a list of the used connector types of the SIS3104.

Designation	Function	Manufacturer	Part Number
U200	Optical Link	Finisar	FTLF8524E2KNL
CON20A	Ethernet	Erni	203215L9
CON23A, CON21A, CON32A, CON33A	LEMO I/O	LEMO	EPL.00.250.NTN
P1/P2	VME connector	Harting	02011602101.00
CON100B	JTAG Connector	Molex	87831-1420

14.3 Ordering Options

Find below a list with standard parts from the SIS1100-e/3104 family.
Feel free to inquire about custom versions.

SIS3104	
Component	Struck Part Number
SIS3104 VME Master/Sequencer	02095
SIS3104 VME Master/Sequencer with VME64x handles	03089
SIS1100-eCMC	
Component	Struck Part Number
SIS1100-eCMC Single Lane PCI Express CMC Carrier	03088
SIS1100-eCMC Single Lane PCI Express, 1-Link	02981
SIS1100-eCMC Single Lane PCI Express, 4-Link	02980
Fibers	
Component	Struck Part Number
LC-LC Fiber 5m	00461
LC-LC Fiber 10m	00460
LC-LC Fiber 15m	01536
LC-LC Fiber 20m	00459
LC-LC Fiber 25m	00458
LC-LC Fiber 30m	02643
LC-LC Fiber 150m	02186
LC-ST Fiber 5m	01746
LC-ST Fiber custom length <5m	01747
ST-ST front panel mount bulk head adaptor	01748

14.4 Firmware Revisions/Changes

Find below a list with firmware changes.

Revision	Changes
01x1	Original Design
02x1	SIS3100 compatibility fixes and bus error extension • Make VME D8/D16 compatible to SIS3100 • Bug fix software VME system controller enable • Introduce new bus error distinction 0x211/0x219 for system controller operation • Make VME retry compatible to SIS3100 (with the difference that retry is enabled by default on the SIS3104)
0302	Unified 1G/2G firmware versions, autobaud

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