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EdgeBoard-Lite FZ3

Hardware Manual

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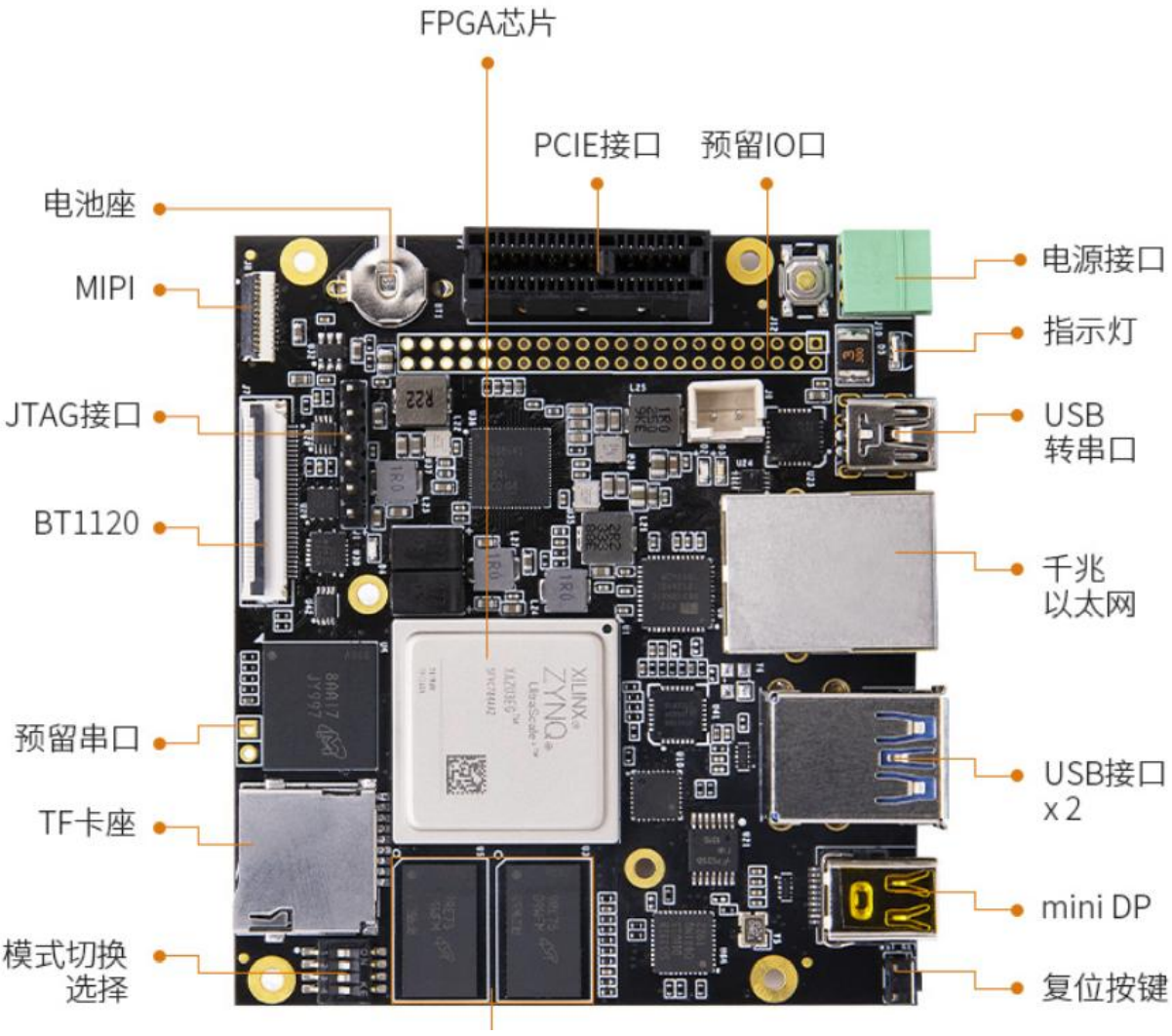
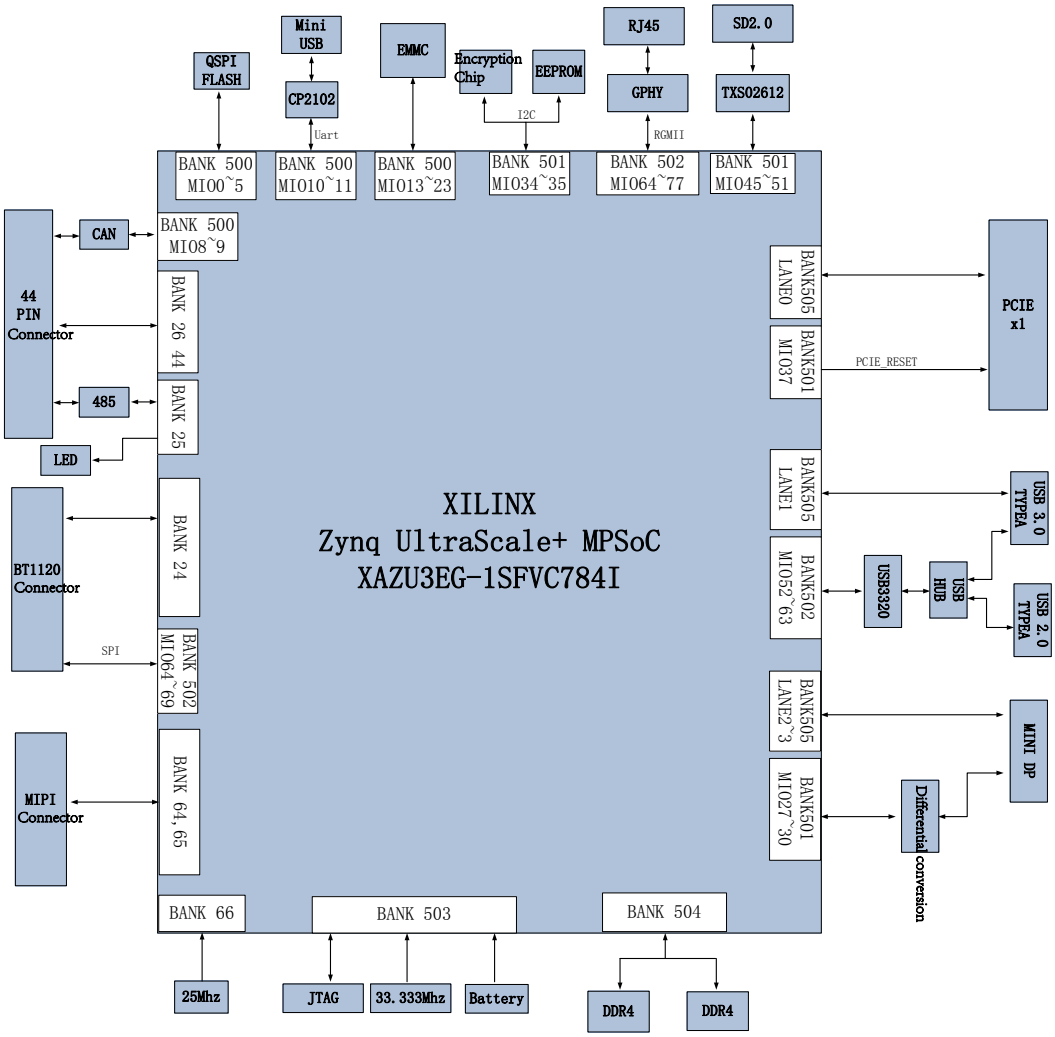
1. Introduction to EdgeBoard-Lite

EdgeBoard-Lite is characterized by small size and expanded rich peripherals. The main chip uses Xilinx's Zynq UltraScale+ MPSoCs EG series chip, the model is XAZU3EG-1SFVC784I. Two DDR4 (2GB, 32bit), one 8GB eMMC FLASH memory chip and one 256Mb QSPI FLASH are mounted on the PS side.

Peripheral interface includes 2 USB interfaces (1 USB3.0, 1 USB2.0), 1 MINI DP interface, 1 Gigabit Ethernet interface, 1 USB serial port, 1 PCIE interface, 1 TF card interface , 1 44-pin expansion port, 1 MIPI interface, 1 BT1120 interface and button LED.



The following figure is a schematic diagram of the structure of the entire development system:



2. ZYNQ Chip

The PS system of the XAZU3EG-1SFVC784I chip The PS system integrates 4 ARM Cortex™-A53 processors with a speed of up to 1.2Ghz and supports Level 2 Cache; it also contains 2 Cortex-R5 processors with a speed of up to 500Mhz.

XAZU3EG supports 32-bit or 64-bit DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 memory chips, with rich high-speed interfaces such as PCIE Gen2, USB3.0, SATA 3.1, DisplayPort on the PS side; also supports USB2.0, Gigabit Ethernet, SD/SDIO, I2C, CAN, UART, GPIO and other interfaces. The PL terminal contains abundant programmable logic units, DSP and internal RAM. The overall block diagram of the XAZU3EG chip is shown in the figure below

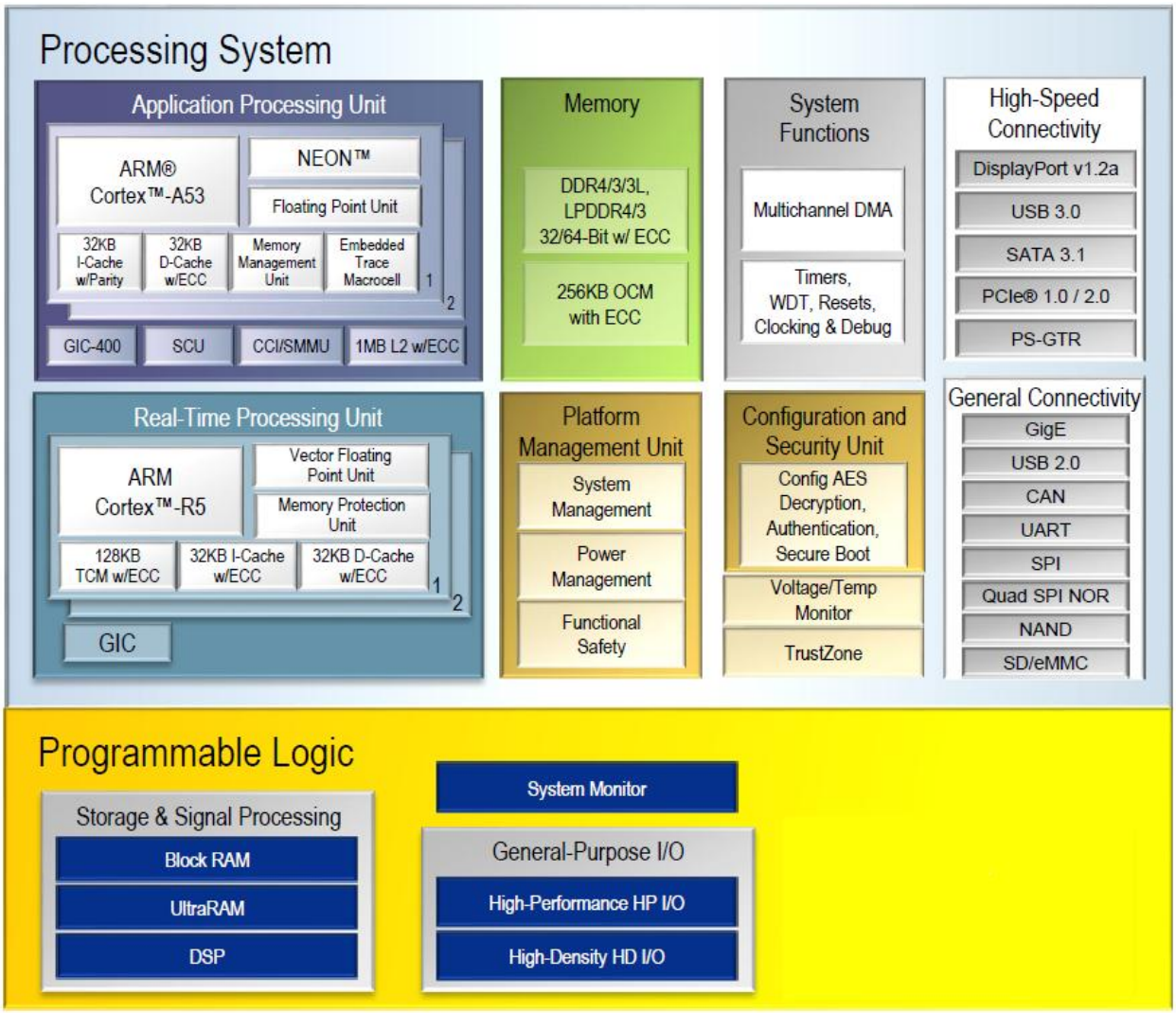


Figure ZU3EG overall block diagram of the chip

The main parameters of the PS system are as follows:

-ARM quad-core Cortex™-A53 processor, speed up to 1.2GHz, 32KB level 1 instruction and count per CPU

According to the cache, 1MB level 2 cache is shared by 2 CPUs.

-ARM dual-core Cortex-R5 processor, speed up to 500MHz, 32KB level 1 instruction and data per CPU

Cache, and 128K tightly coupled memory.

-External storage interface, support 32/64bit DDR4/3/3L, LPDDR4/3 interface.

-Static storage interface, support NAND, 2xQuad-SPI FLASH.

-High-speed connection interface, support PCIe Gen2 x4, 2xUSB3.0, Sata 3.1, DisplayPort, 4x Tri-mode

Gigabit Ethernet。

- Common connection interface：2xUSB2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO。
- Power management: support the division of the four parts of Full/Low/PL/Battery.

-Encryption algorithm: support RSA, AES and SHA.

-System monitoring: 10-bit 1Mbps AD sampling for temperature and voltage detection. The main parameters of the PL logical part are as follows:

-Logic Cells: 154K;

-Flip-flops: 141K;

-Lookup table LUTs: 71K;

-Block RAM: 9.4Mb;

-Clock management units (CMTs): 3

-Multipliers 18x25MACCs: 360

The speed grade of XAZU3EG-1SFVC784I chip is -1, industrial grade, and the package is SFVC784.

3. DDR4 DRAM

The PS side of the EdgeBoard-Lite board is equipped with 2 Micron (Micron) 1GB DDR4 chips, model MT40A512M16LY-062EIT, which constitutes a 32-bit data bus bandwidth and 2GB capacity. The maximum operating speed of DDR4 SDRAM on the PS side can reach 1200MHz (data rate 2400Mbps). The specific configuration of DDR4 SDRAM is shown below.

Tag	Chip Model	Capacity	Factory
U3,U5	MT40A512M16LY-062EIT	512M x 16bit	Micron

Table 3-1 DDR4 SDRAM configuration The hardware connection of DDR4 on the PS side is shown below:

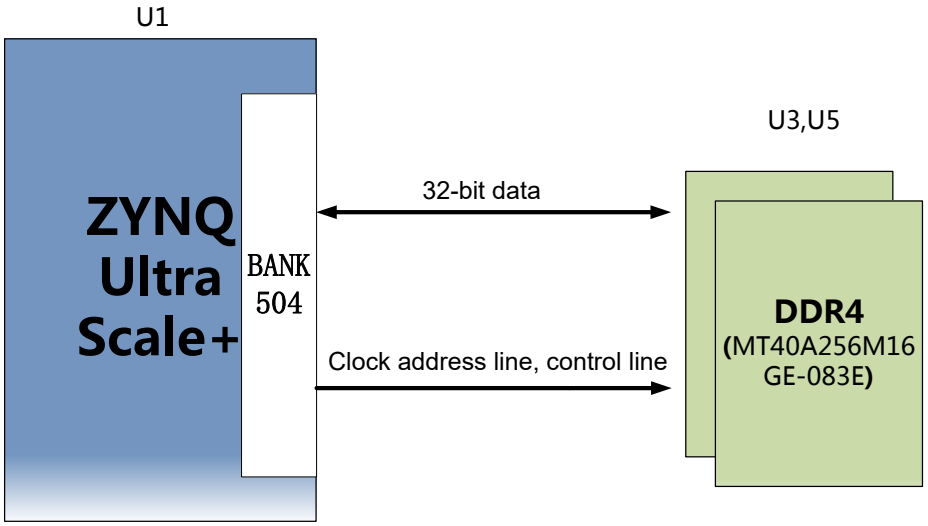


Figure 3-1 PS side DDR4 DRAM schematic part

Pin assignment of PS DDR4 SDRAM:

Signal name	Pin name	Pin number
PS_DDR4_DQS0_P	PS_DDR_DQS_P0_504	AF21
PS_DDR4_DQS0_N	PS_DDR_DQS_N0_504	AG21
PS_DDR4_DQS1_P	PS_DDR_DQS_P1_504	AF23
PS_DDR4_DQS1_N	PS_DDR_DQS_N1_504	AG23
PS_DDR4_DQS2_P	PS_DDR_DQS_P2_504	AF25
PS_DDR4_DQS2_N	PS_DDR_DQS_N2_504	AF26
PS_DDR4_DQS3_P	PS_DDR_DQS_P3_504	AE27
PS_DDR4_DQS3_N	PS_DDR_DQS_N3_504	AF27
PS_DDR4_DQ0	PS_DDR_DQ0_504	AD21
PS_DDR4_DQ1	PS_DDR_DQ1_504	AE20
PS_DDR4_DQ2	PS_DDR_DQ2_504	AD20
PS_DDR4_DQ3	PS_DDR_DQ3_504	AF20
PS_DDR4_DQ4	PS_DDR_DQ4_504	AH21
PS_DDR4_DQ5	PS_DDR_DQ5_504	AH20
PS_DDR4_DQ6	PS_DDR_DQ6_504	AH19
PS_DDR4_DQ7	PS_DDR_DQ7_504	AG19
PS_DDR4_DQ8	PS_DDR_DQ8_504	AF22
PS_DDR4_DQ9	PS_DDR_DQ9_504	AH22
PS_DDR4_DQ10	PS_DDR_DQ10_504	AE22
PS_DDR4_DQ11	PS_DDR_DQ11_504	AD22
PS_DDR4_DQ12	PS_DDR_DQ12_504	AH23
PS_DDR4_DQ13	PS_DDR_DQ13_504	AH24
PS_DDR4_DQ14	PS_DDR_DQ14_504	AE24
PS_DDR4_DQ15	PS_DDR_DQ15_504	AG24
PS_DDR4_DQ16	PS_DDR_DQ16_504	AC26
PS_DDR4_DQ17	PS_DDR_DQ17_504	AD26
PS_DDR4_DQ18	PS_DDR_DQ18_504	AD25
PS_DDR4_DQ19	PS_DDR_DQ19_504	AD24
PS_DDR4_DQ20	PS_DDR_DQ20_504	AG26
PS_DDR4_DQ21	PS_DDR_DQ21_504	AH25
PS_DDR4_DQ22	PS_DDR_DQ22_504	AH26
PS_DDR4_DQ23	PS_DDR_DQ23_504	AG25

PS_DDR4_DQ24	PS_DDR_DQ24_504	AH27
PS_DDR4_DQ25	PS_DDR_DQ25_504	AH28
PS_DDR4_DQ26	PS_DDR_DQ26_504	AF28
PS_DDR4_DQ27	PS_DDR_DQ27_504	AG28
PS_DDR4_DQ28	PS_DDR_DQ28_504	AC27
PS_DDR4_DQ29	PS_DDR_DQ29_504	AD27
PS_DDR4_DQ30	PS_DDR_DQ30_504	AD28
PS_DDR4_DQ31	PS_DDR_DQ31_504	AC28
PS_DDR4_DM0	PS_DDR_DM0_504	AG20
PS_DDR4_DM1	PS_DDR_DM1_504	AE23
PS_DDR4_DM2	PS_DDR_DM2_504	AE25
PS_DDR4_DM3	PS_DDR_DM3_504	AE28
PS_DDR4_A0	PS_DDR_A0_504	W28
PS_DDR4_A1	PS_DDR_A1_504	Y28
PS_DDR4_A2	PS_DDR_A2_504	AB28
PS_DDR4_A3	PS_DDR_A3_504	AA28
PS_DDR4_A4	PS_DDR_A4_504	Y27
PS_DDR4_A5	PS_DDR_A5_504	AA27
PS_DDR4_A6	PS_DDR_A6_504	Y22
PS_DDR4_A7	PS_DDR_A7_504	AA23
PS_DDR4_A8	PS_DDR_A8_504	AA22
PS_DDR4_A9	PS_DDR_A9_504	AB23
PS_DDR4_A10	PS_DDR_A10_504	AA25
PS_DDR4_A11	PS_DDR_A11_504	AA26
PS_DDR4_A12	PS_DDR_A12_504	AB25
PS_DDR4_A13	PS_DDR_A13_504	AB26
PS_DDR4_WE_B	PS_DDR_A14_504	AB24
PS_DDR4_CAS_B	PS_DDR_A15_504	AC24
PS_DDR4_RAS_B	PS_DDR_A16_504	AC23
PS_DDR4_ACT_B	PS_DDR_ACT_N_504	Y23
PS_DDR4_ALERT_B	PS_DDR_ALERT_N_504	U25
PS_DDR4_BA0	PS_DDR_BA0_504	V23
PS_DDR4_BA1	PS_DDR_BA1_504	W22
PS_DDR4_BG0	PS_DDR_BG0_504	W24
PS_DDR4_CS0_B	PS_DDR_CS_N0_504	W27

PS_DDR4_ODT0	PS_DDR_ODT0_504	U28
PS_DDR4_PARITY	PS_DDR_PARITY_504	V24
PS_DDR4_RESET_B	PS_DDR_RST_N_504	U23
PS_DDR4_CLK0_P	PS_DDR_CK0_P_504	W25
PS_DDR4_CLK0_N	PS_DDR_CK0_N_504	W26
PS_DDR4_CKE0	PS_DDR_CKE0_504	V28

4. QSPI Flash

EdgeBoard-Lite is equipped with a 256MBit Quad-SPI FLASH chip, the model is MT25QU256ABA1EW9-0SIT. QSPI FLASH is connected to the GPIO port of BANK500 in the PS part of the ZYNQ chip. Figure 4-1 shows the part of QSPI Flash in the schematic diagram.

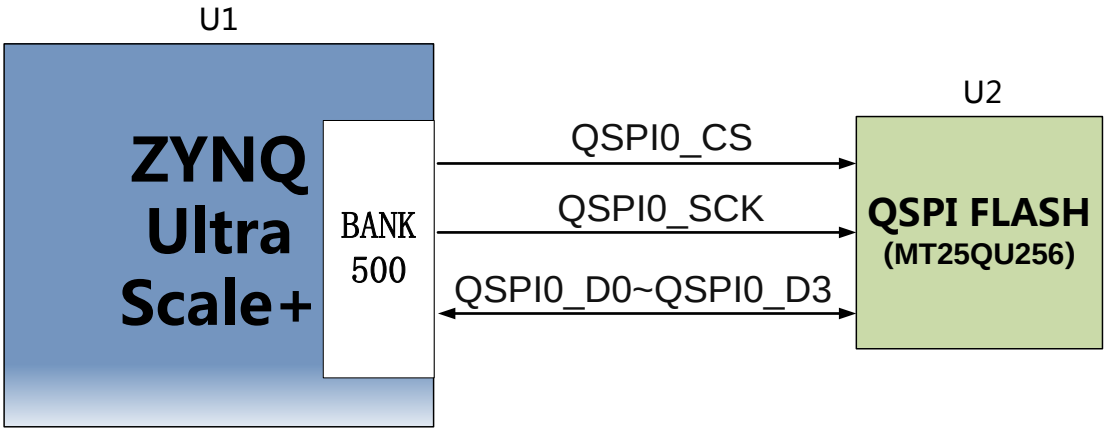


Figure 4-1 QSPI Flash connection diagram

Configure chip pin assignment:

Signal name	Pin name	Pin number
MIO0_QSPI0_SCLK	PS_MIO0_500	AG15
MIO1_QSPI0_IO1	PS_MIO1_500	AG16
MIO2_QSPI0_IO2	PS_MIO2_500	AF15
MIO3_QSPI0_IO3	PS_MIO3_500	AH15
MIO4_QSPI0_IO0	PS_MIO4_500	AH16
MIO5_QSPI0_SS_B	PS_MIO5_500	AD16

5. eMMC Flash

EdgeBoard-Lite is equipped with an eMMC FLASH chip with a capacity of 8GB. eMMC FLASH is connected to

PS part of ZYNQ UltraScale+ On the GPIO port of BANK500, Figure 5-1 shows the part of eMMC Flash in the schematic diagram.

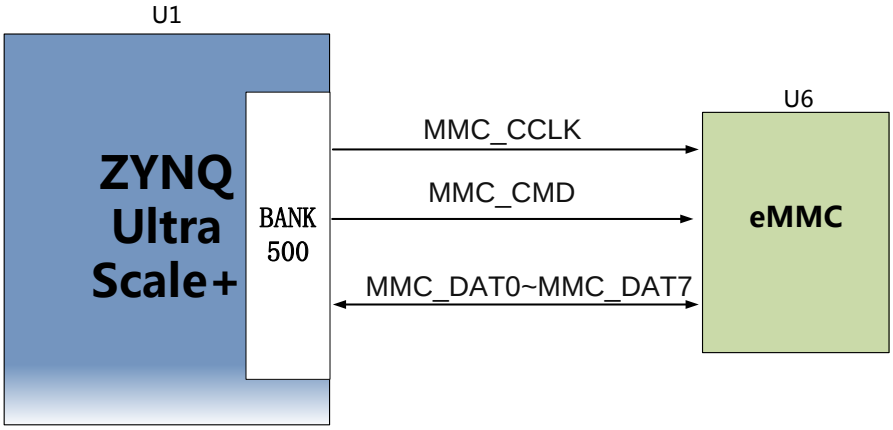


Figure 5-1 eMMC Flash connection diagram

Configure chip pin assignment:

Signal name	Pin name	Pin number
MMC_DAT0	PS_MIO13_500	AH18
MMC_DAT1	PS_MIO14_500	AG18
MMC_DAT2	PS_MIO15_500	AE18
MMC_DAT3	PS_MIO16_500	AF18
MMC_DAT4	PS_MIO17_500	AC18
MMC_DAT5	PS_MIO18_500	AC19
MMC_DAT6	PS_MIO19_500	AE19
MMC_DAT7	PS_MIO20_500	AD19
MMC_CMD	PS_MIO21_500	AC21
MMC_CCLK	PS_MIO22_500	AB20
MMC_RSTN	PS_MIO23_500	AB18

6. EEPROM

The EdgeBoard-Lite development board has an onboard EEPROM, model 24LC04. The I2C signal of the EEPROM is connected to the MIO port of the ZYNQ PS terminal. Figure 6-1 is the schematic diagram of EEPROM

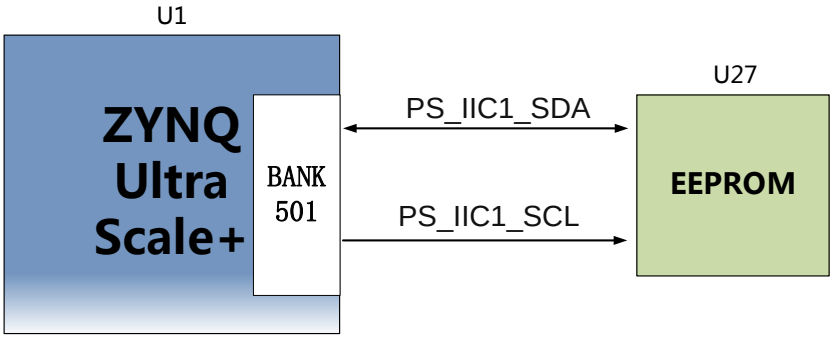


Fig 7-5 EEPROM Schematic part

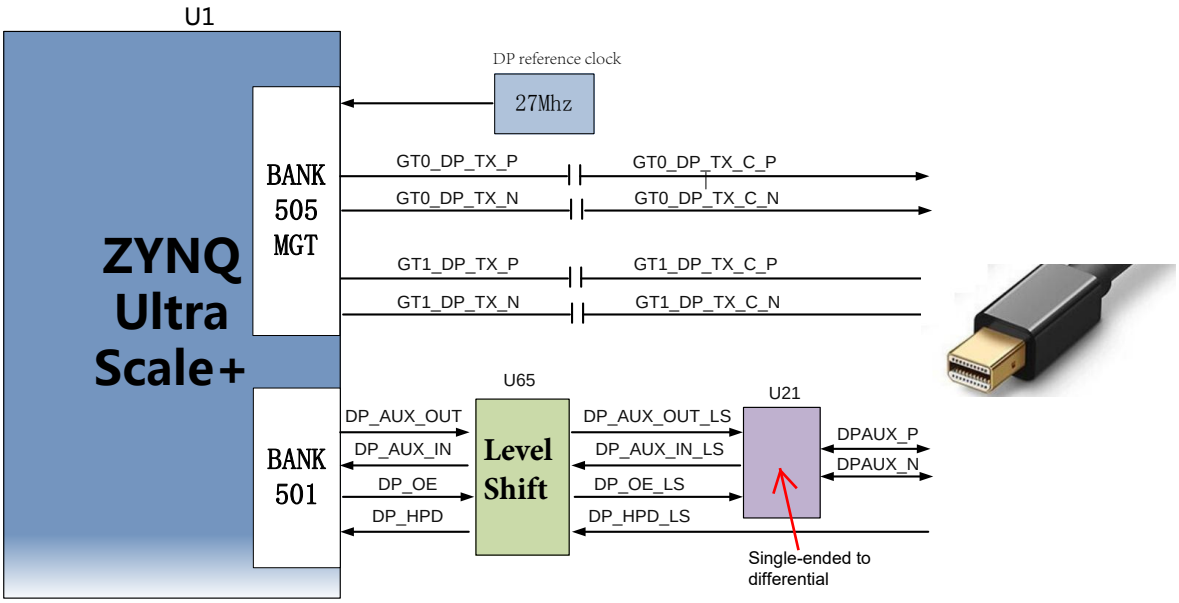
EEPROM pin assignment:

Signal name	Pin name	Pin number
PS_IIC1_SCL	PS_MIO32_501	J16
PS_IIC1_SDA	PS_MIO33_501	L16

7. DP Display Interface

EdgeBoard-Lite has a 1-port MINI-type DisplayPort output display interface for video image display, and supports up to 4K x 2K@30Fps output. ZU3EG PS MGT's LANE0 and LANE1 TX signals are differential signals

To the DP connector. The DisplayPort auxiliary channel is connected to the MIO pin of the PS. The schematic diagram of the DP output interface is shown in Figure 7-1:



7-1 DP interface design diagram

DisplayPort interface ZYNQ pin assignments are as follows:

Signal name	ZYNQ pin name	Pin number	Remarks
GT0_DP_TX_P	PS_MGTTXP3_505	B23	DP Data low bit is sent positive
GT0_DP_TX_N	PS_MGTTXN3_505	B24	DP data low bit send negative
GT1_DP_TX_P	PS_MGTTXP2_505	C25	DP data is sent high
GT1_DP_TX_N	PS_MGTTXN2_505	C26	DP data high bit send negative
505_DP_CLKP	PS_MGTREFCLK2P_505	C21	DP reference clock
505_DP_CLKP	PS_MGTREFCLK2N_505	C22	DP reference clock negative
DP_AUX_OUT	PS_MIO27	J15	DP auxiliary data output
DP_AUX_IN	PS_MIO30	F16	DP auxiliary data input
DP_OE	PS_MIO29	G16	DP auxiliary data output enable
DP_HPD	PS_MIO28	K15	DP insertion signal detection

8. USB Interface

There are 2 USB ports (including one USB2.0 and one USB3.0) on the EdgeBoard-Lite board, the port is HOST
Working mode (Type A), the data transmission speed is up to 5.0Gb/s. USB2.0 connects external USB PHY chip and USB2.0 HUB chip through ULPI interface to realize high-speed USB3.0 and USB2.0 data communication.

The schematic diagram of USB connection is shown in 8-1:

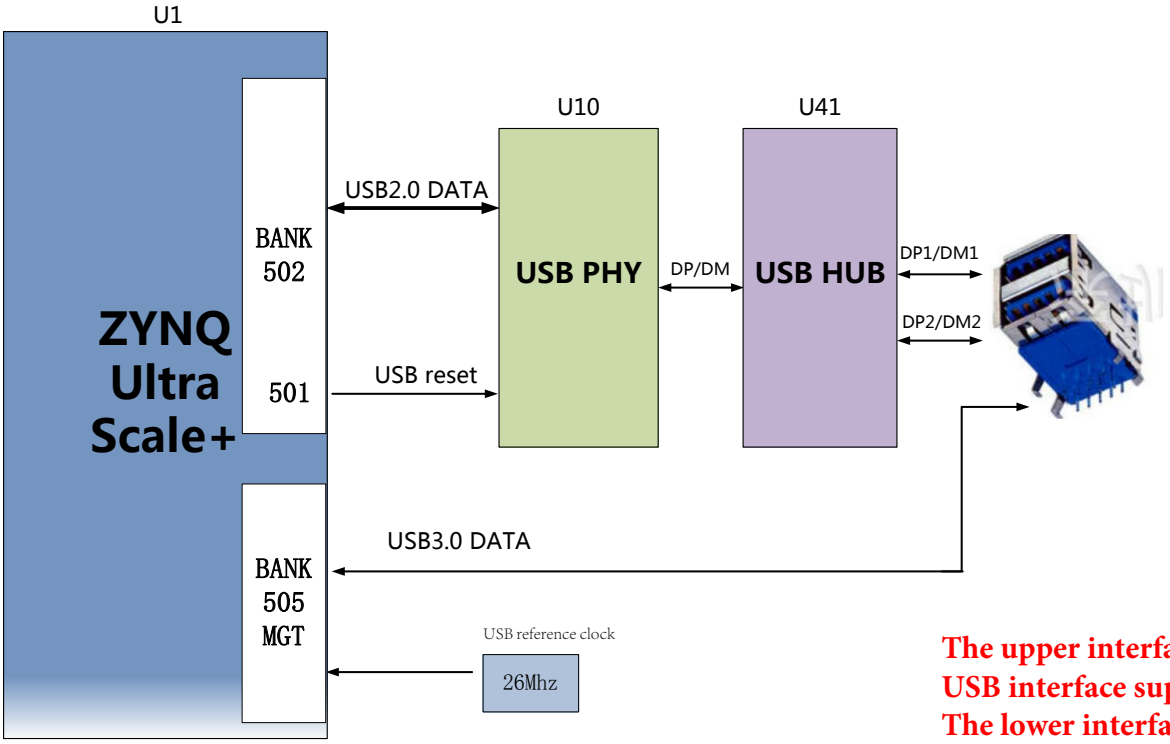


Figure 8-1 Schematic diagram of USB interface

The upper interface of the USB interface supports 3.0. The lower interface of the USB interface only supports 2.0.

USB pin assignment:

Signal name	Pin name	Pin number	Remarks
USB_SSTXP	PS_MGTTXP2_505	D23	**USB3.0 data sending**
USB_SSTXN	PS_MGTTXN2_505	D24	**USB3.0 data transmission negative**
USB_SSRXP	PS_MGTRXP2_505	D27	**USB3.0 data receiving**
USB_SSRXN	PS_MGTRXN2_505	D28	**USB3.0 data receiving negative**
505_USB_CLKP	PS_MGTREFCLK2P_505	E21	**USB3.0 reference clock**
505_USB_CLKN	PS_MGTREFCLK2N_505	E22	**USB3.0 reference clock negative**
USB_DATA0	PS_MIO56	C16	**USB2.0 data Bit0**
USB_DATA1	PS_MIO57	A16	**USB2.0 data Bit1**
USB_DATA2	PS_MIO54	F17	**USB2.0 data Bit2**
USB_DATA3	PS_MIO59	E17	**USB2.0 data Bit3**
USB_DATA4	PS_MIO60	C17	**USB2.0 data Bit4**
USB_DATA5	PS_MIO61	D17	**USB2.0 data Bit5**
USB_DATA6	PS_MIO62	A17	**USB2.0 data Bit6**
USB_DATA7	PS_MIO63	E18	**USB2.0 data Bit7**
USB_STP	PS_MIO58	F18	**USB2.0 Stop signal**
USB_DIR	PS_MIO53	D16	**USB2.0 Data direction signal**
USB_CLK	PS_MIO52	G18	**USB2.0 Clock signal**
USB_NXT	PS_MIO55	B16	**USB2.0 Next data signal**

9. Gigabit Ethernet Interface

There is one Gigabit Ethernet interface on the EdgeBoard-Lite. The Ethernet interface is on the BANK502 of PS connected by GPHY chip. GPHY chip adopts KSZ9031RNXIC Ethernet PHY chip of Micrel Company, PHY Address is 001. Figure 9-1 shows the connection diagram of the ZYNQ PS-end Ethernet PHY chip:

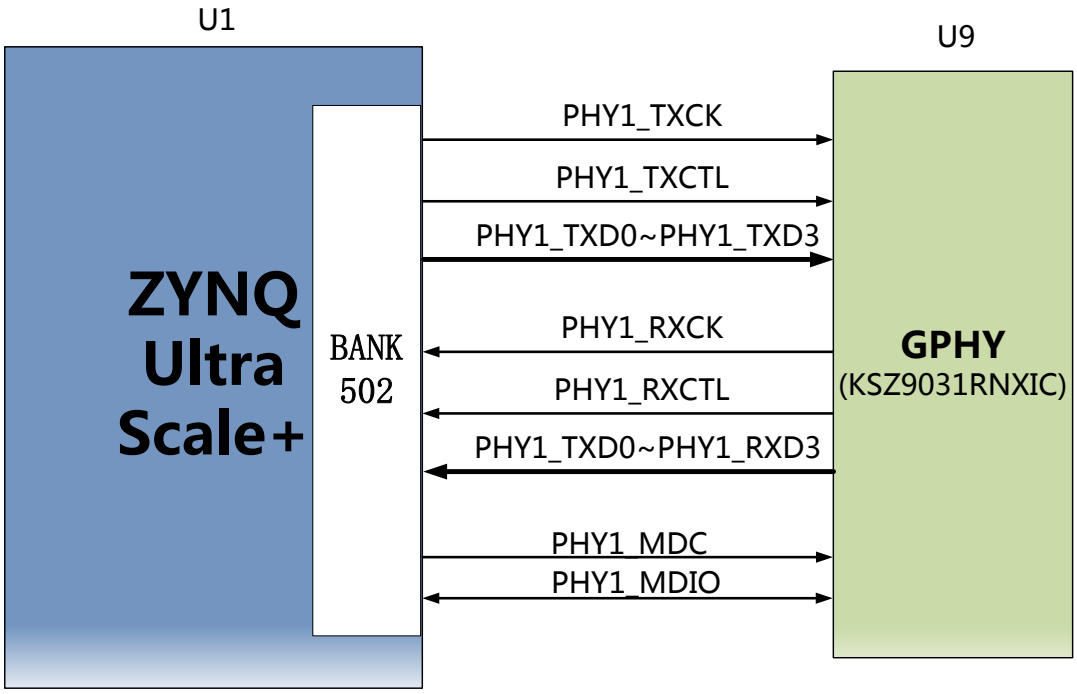


Figure 9-1 Connection diagram of ZYNQ PS system and GPHY

The Gigabit Ethernet pin assignment is as follows:

Signal name	Pin name	Pin number	Remarks
PHY1_TXCK	PS_MIO64	E19	RGMII transmit clock
PHY1_TXD0	PS_MIO65	A18	Send Data bit0
PHY1_TXD1	PS_MIO66	G19	Send Data bit1
PHY1_TXD2	PS_MIO67	B18	Send Databit2
PHY1_TXD3	PS_MIO68	C18	Send Databit3
PHY1_TXCTL	PS_MIO69	D19	Send enable signal
PHY1_RXCK	PS_MIO70	C19	RGMII receive clock
PHY1_RXD0	PS_MIO71	B19	Receive Data Bit0
PHY1_RXD1	PS_MIO72	G20	Receive Data Bit1
PHY1_RXD2	PS_MIO73	G21	Receive Data Bit2
PHY1_RXD3	PS_MIO74	D20	Receive Data Bit3
PHY1_RXCTL	PS_MIO75	A19	Receive data valid signal
PHY1_MDC	PS_MIO76	B20	MDIO management clock
PHY1_MDIO	PS_MIO77	F20	MDIO management data

10. USB-UART Interface

The EdgeBoard-Lite board is equipped with a Uart to USB interface for system debugging. The conversion chip adopts the USB-UAR chip of Silicon Labs CP2102, and the USB interface adopts the MINI USB interface. It can be connected to the USB port of the upper PC with a USB cable for independent power supply of the core board and serial data communication. The schematic diagram of the USB Uart circuit design is shown below:

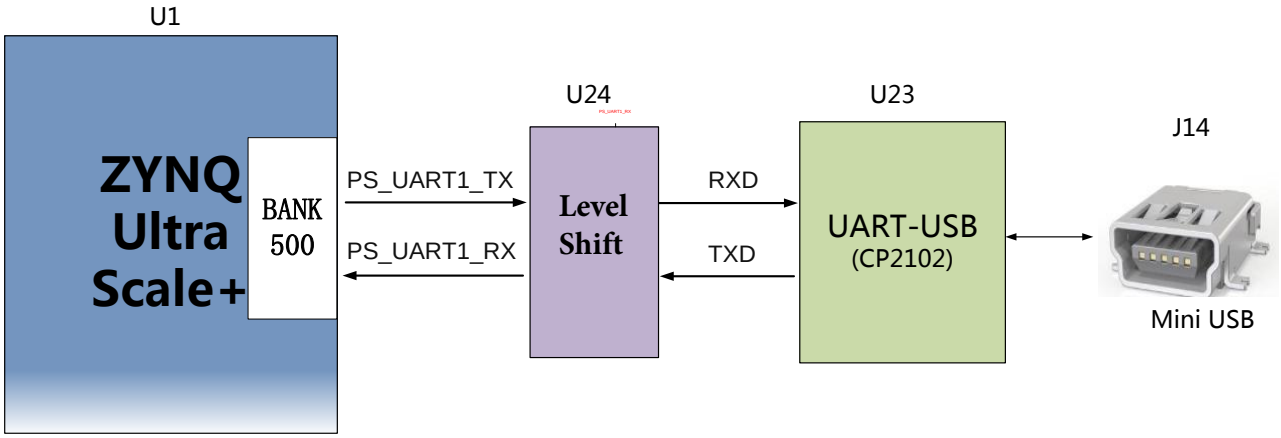


Figure 10-1 Schematic diagram of USB to serial port

ZYNQ pin assignment from USB to serial:

Signal name	Pin name	Pin number	Remarks
PS_UART1_TX	PS_MIO24	AB19	Uart data output
PS_UART1_RX	PS_MIO25	AB21	Uart data input

11. SD Cardslot

The EdgeBoard-Lite board includes a Micro SD card interface. The SDIO signal is connected to the IO signal of the PS BANK501 of ZU3EG. The schematic diagram of the SD card connector is shown in Figure 11-1.

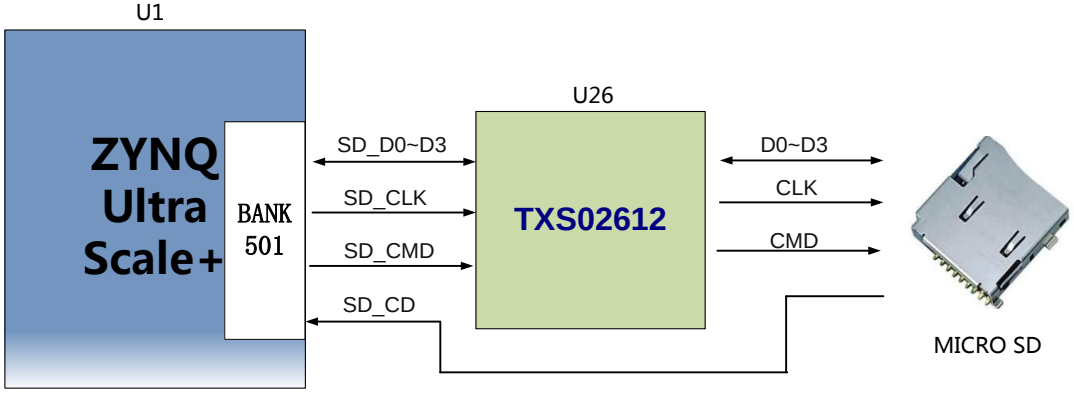


Figure 11-1 Schematic diagram of SD card connection

SD card slot pin assignment

Signal name	Pin name	Pin number	Remarks
SD_CLK	PS_MIO51	I21	SD clock signal
SD_CMD	PS_MIO50	M19	SD command signal
SD_D0	PS_MIO46	L20	SD data Data0
SD_D1	PS_MIO47	H21	SD data Data1
SD_D2	PS_MIO48	J21	SD data Data2
SD_D3	PS_MIO49	M18	SD data Data3
SD_CD	PS_MIO45	K20	SD card heartbeat

12. PCIE Interface

EdgeBoard-Lite is equipped with a PCIE x1 slot for connecting PCIE peripherals, and the PCIE communication speed is up to 5Gbps. The PCIE signal is directly connected to LANE0 of ZU3EG's BANK505 PS MGT transceiver. The schematic diagram of PCIE x 1 design is shown in Figure 12-1 below:

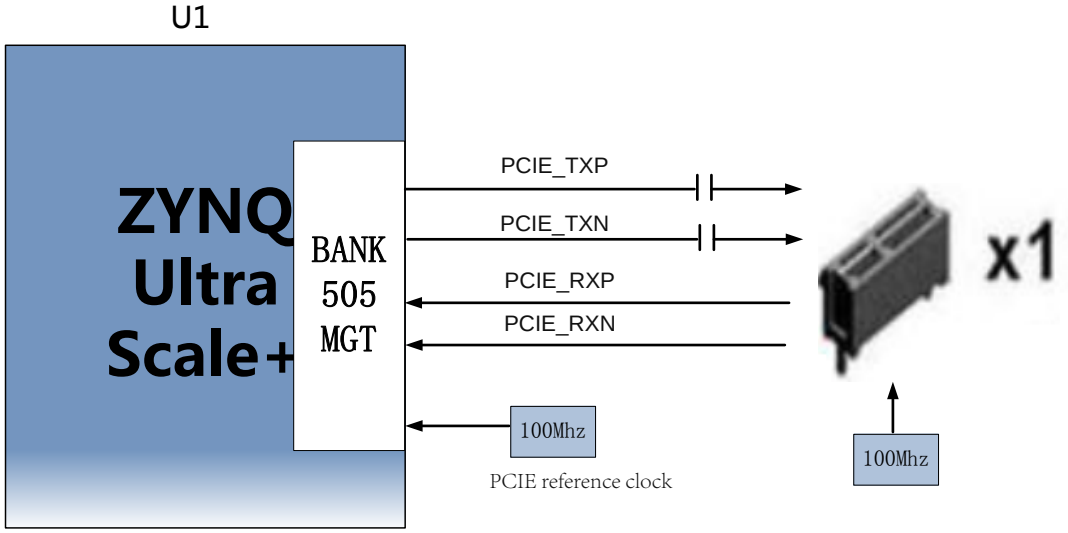


Figure 12-1 Schematic diagram of PCIE interface design

The ZYNQ pin assignment of the PCIE interface is as follows:

Signal name	Pin name	Pin number	Remarks
PCIE_TXP	PS_MGTTXP0_505	E25	PCIE data is being sent
PCIE_TXN	PS_MGTTXN0_505	E26	PCIE data transmission negative
PCIE_RXP	PS_MGTRXP0_505	F27	PCIE data receiving

PCIE_RXN	PS_MGTRXN0_505	F28	PCIE data reception negative
PCIE_REFCLK_P	PS_MGTREFCLK0P_505	F23	PCIE reference clock
PCIE_REFCLK_N	PS_MGTREFCLK0N_505	F24	PCIE reference clock negative

13. 44 Pin Extension

EdgeBoard-Lite reserves a 44-pin expansion port with a pitch of 2.0mm, including 3.3V power supply, RS485 bus, CAN bus and 36 IO ports. The CAN interface is connected to the MIO of the PS through the chip, 36 IO connections are connected to the IO of the ZYNQ chip BANK44, 26, the level standard is 3.3V. The schematic diagram of the expansion port design is shown in Figure 13-1 below:

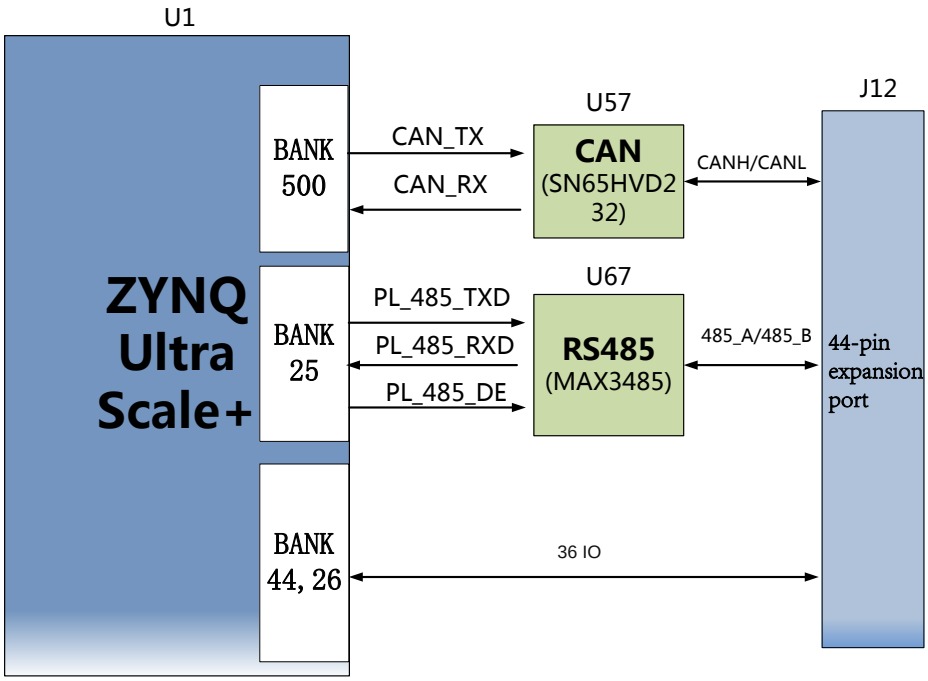
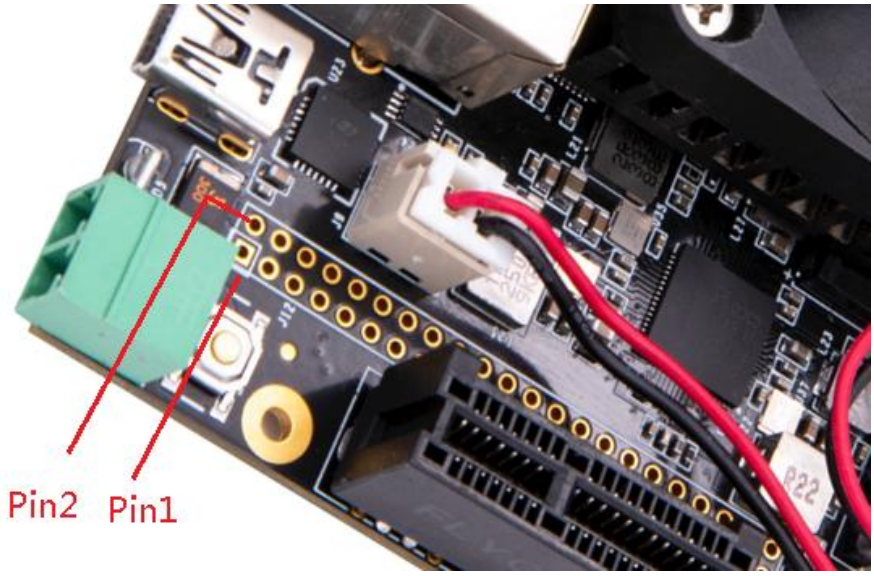


Figure 13-1 Schematic diagram of expansion port design



Indication diagram of expansion port PIN

The pin assignment of J12 expansion port ZYNQ is as follows:

J12 pin	Signal name	Pin number	J12 pin	Signal name	Pin number
1	+3.3V	-	2	+3.3V	-
3	GND	-	4	GND	-
5	485_A	-	6	485_B	-
7	CANH	-	8	CANL	-
9	IO_B14_1P	B14	10	IO_A14_1N	A14
11	IO_B15_2P	B15	12	IO_A15_2N	A15
13	IO_C14_3P	C14	14	IO_C13_3N	C13
15	IO_G13_4P	G13	16	IO_F13_4N	F13
17	IO_H14_5P	H14	18	IO_H13_5N	H13
19	IO_L14_6P	L14	20	IO_L13_6N	L13
21	IO_B13_7P	B13	22	IO_A13_7N	A13
23	IO_D15_8P	D15	24	IO_D14_8N	D14
25	IO_E14_9P	E14	26	IO_E13_9N	E13
27	IO_F15_10P	F15	28	IO_E15_10N	E15
29	IO_K14_11P	K14	30	IO_J14_11N	J14
31	IO_W10_12P	W10	32	IO_Y10_12N	Y10
33	IO_Y9_13P	Y9	34	IO_AA8_13N	AA8
35	IO_AB11_14P	AB11	36	IO_AC11_14N	AC11

37	IO_AD11_15P	AD11	38	IO_AD10_15N	AD10
39	IO_AE10_16P	AE10	40	IO_AF10_16N	AF10
41	IO_AF11_17P	AF11	42	IO_AG11_17N	AG11
43	IO_AG10_18P	AG10	44	IO_AH10_18N	AH10

The pin assignment of ZYNQ corresponding to RS485 is as follows:

Signal name	Pin name	Pin number	Remarks
PL_485_TXD	IO_L6P_25	F12	RS485 data transmission
PL_485_RXD	IO_L9N_25	B10	RS485 data reception
PL_485_DE	IO_L10N_25	A12	RS485 receiving direction selection

The pin assignment of ZYNQ corresponding to CAN is as follows:

Signal name	Pin name	Pin number	Remarks
CAN_TX	PS_MIO8	AF17	CAN data transmission
CAN_RX	PS_MIO9	AC16	CAN data reception

14. MIPI Interface

EdgeBoard-Lite has one MIPI interface, which is used to connect MIPI camera. The MIPI differential signal is connected to the HP IO of BANK64, the level standard is +1.2V; the MIPI control signal is connected to the BANK65, the level standard is +1.8V; the I2C control signal is connected to the BANK501, the level standard is + 1.8V. The schematic diagram of the MIPI port design is shown in Figure 14-1:

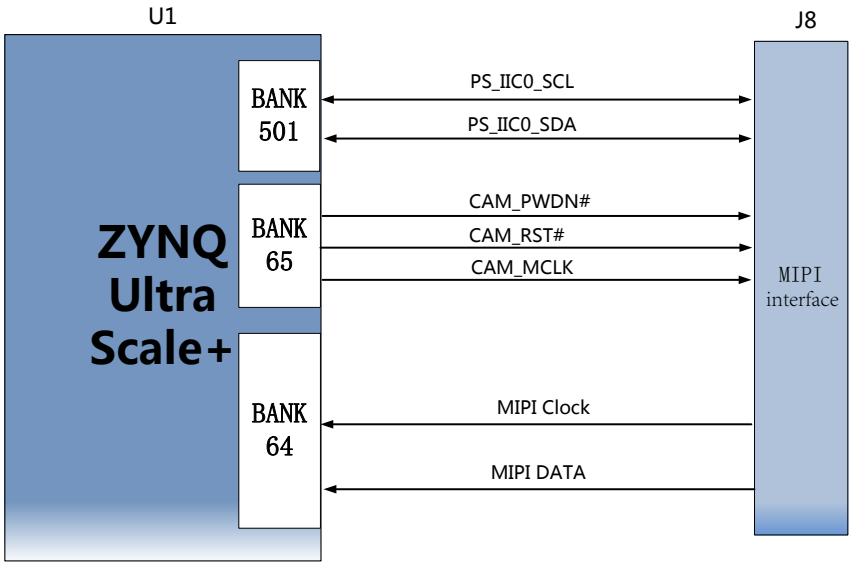


Figure 14-1 MIPI interface connection diagram

The MIPI communication pin assignment is as follows:

PIN	Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
1	MIPI_CSI_DATA3P	IO_L18P_64	AB1	MIPI data 3 signal P
2	MIPI_CSI_DATA3N	IO_L18N_64	AC1	MIPI data 3 signal N
3	GND	-	-	Ground
4	MIPI_CSI_DATA2P	IO_L17P_64	AB2	MIPI data 2 signal P
5	MIPI_CSI_DATA2N	IO_L17N_64	AC2	MIPI data 2 signal N
6	GND	-	-	Ground
7	MIPI_CSI_DATA1P	IO_L15P_64	AB4	MIPI data 1 signal P
8	MIPI_CSI_DATA1N	IO_L15N_64	AB3	MIPI data 1 signal N
9	GND	-	-	Ground
10	MIPI_CSI_DATA0P	IO_L14P_64	AC4	MIPI data 0 signal P
11	MIPI_CSI_DATA0N	IO_L14N_64	AC3	MIPI data 0 signal N
12	GND	-	-	Ground
13	MIPI_CSI_CLKP	IO_L13P_64	AD5	MIPI clock signal P
14	MIPI_CSI_CLKN	IO_L13N_64	AD4	MIPI clock signal N
15	GND	-	-	Ground
16	CAM_MCLK	IO_L13P_65	L7	Clock signal
17	GND	-	-	Ground
18	MIPI_IOVDD_1V8	-	-	+1.8V power supply
19	MIPI_IOVDD_1V3	-	-	+1.3V power supply
20	PS_IIC0_SCL	PS_MIO34	L17	I2C control clock
21	PS_IIC0_SDA	PS_MIO35	H17	I2C control data
22	CAM_PWDN#	IO_L1N_65	Y8	Power Down signal
23	CAM_RST#	IO_L2P_65	U9	RESET signal
24	MIPI_AVDD_3V3_2V8	-	-	+2.8V power supply
25	MIPI_AVDD_3V3_2V8	-	-	+2.8V power supply

15. BT1120 Interface

There is a 32PIN BT1120 connector on the EdgeBoard-Lite for video transmission and communication.
BT1120

The signal is connected to the IO of BANK24, the level standard is +3.3V, and the user can use it as normal IO. In addition, there are SPI interface and UART interface (level standard is +3.3V) on the interface, which is connected to the MIO of ZU3EG through level conversion. The schematic diagram of BT1120 interface design is shown in Figure 15-1 below:

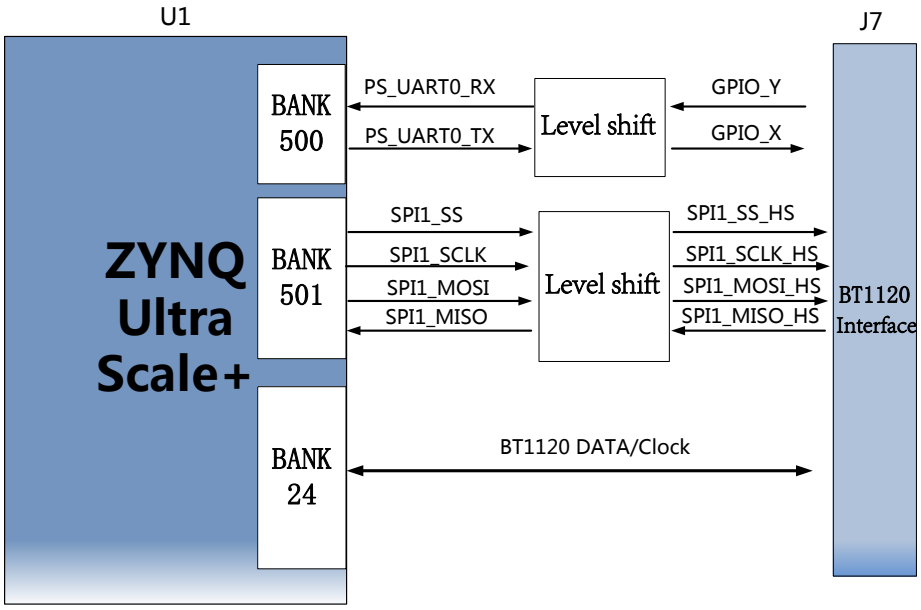


Figure 15-1 BT1120 interface connection diagram

The BT1120 communication pin assignment is as follows:

PIN	Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
1	BT1120_DATA0	IO_L9N_24	W13	BT1120 data 0
2	BT1120_DATA1	IO_L9P_24	W14	BT1120 data 1
3	BT1120_DATA2	IO_L8N_24	AB14	BT1120 data 2
4	BT1120_DATA3	IO_L8P_24	AB15	BT1120 data 3
5	BT1120_DATA4	IO_L7N_24	AB13	BT1120 data 4
6	BT1120_DATA5	IO_L7P_24	AA13	BT1120 data 5
7	BT1120_DATA6	IO_L6N_24	AC13	BT1120 data 6
8	BT1120_DATA7	IO_L6P_24	AC14	BT1120 data 7
9	BT1120_DATA8	IO_L5N_24	AD14	BT1120 data 8
10	BT1120_DATA9	IO_L4N_24	AF13	BT1120 data 9
11	BT1120_DATA10	IO_L4P_24	AE13	BT1120 data 10
12	BT1120_DATA11	IO_L3N_24	AH13	BT1120 data 11
13	BT1120_DATA12	IO_L3P_24	AG13	BT1120 data 12
14	BT1120_DATA13	IO_L2N_24	AH14	BT1120 data 13
15	BT1120_DATA14	IO_L2P_24	AG14	BT1120 data 14

16	BT1120_DATA15	IO_L1N_24	AE14	BT1120 data 15
17	GND	-	-	Ground
18	BT1120_CLK	IO_L5P_24	AD15	BT1120 clock
19	GND	-	-	Ground
20	GPIO_Z	IO_L1P_24	AE15	GPIO reserved
21	GPIO_Y	PS_MIO10_500	AD17	UART reception
22	GPIO_X	PS_MIO11_500	AE17	UART transmission
23	GND	-	-	Ground
24	SPI1_SCLK_HS	PS_MIO38_501	H18	SPI clock
25	SPI1_MOSI_HS	PS_MIO43_501	K19	SPI output
26	SPI1_MISO_HS	PS_MIO42_501	L18	SPI input
27	SPI1_CS_HS	PS_MIO41_501	J19	SPI Chip Select
28	GND	-	-	Ground
29	+12V	-	-	+12Vcc
30	+12V	-	-	+12Vcc
31	+12V	-	-	+12Vcc
32	+12V	-	-	+12Vcc

16. JTAG Debug Port

A 6-pin JTAG interface is reserved on the EdgeBoard-Lite board for downloading the ZYNQ UltraScale+ program or firmware to FLASH. The pin definition of JTAG is shown in the figure below

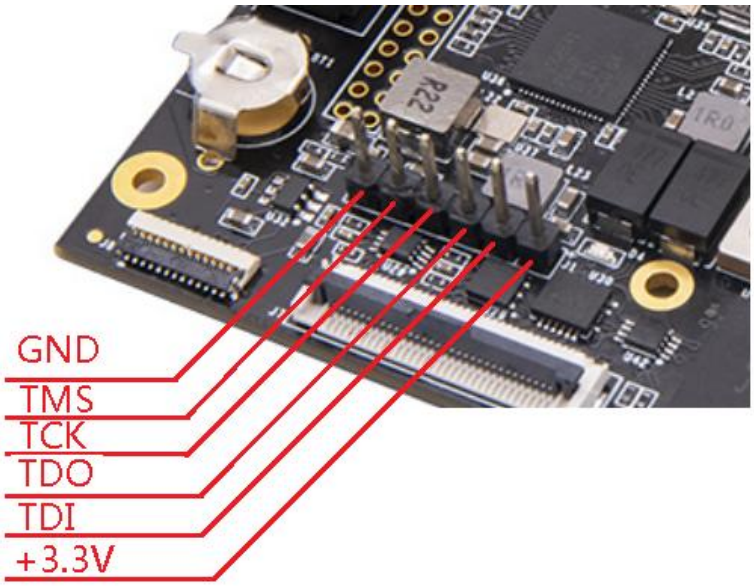


Figure 16-1 JTAG interface pin definition

17. Dip Switch Configuration

There is a 4-digit DIP switch on the board to configure the ZYNQ system startup mode. The EdgeBoard-Lite system supports 4 startup modes. The four startup modes are JTAG debug mode, QSPI FLASH, EMMC and SD2.0 card startup modes. The ZU3EG chip will detect the level of (PS_MODE0~3) after power-on to determine which startup mode. The user can select different start modes through the dial switch. The SW1 startup mode configuration is shown in Table 17-1 below.

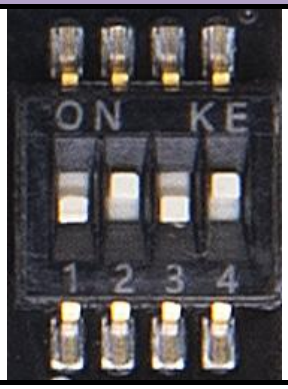
SW1	DIP position4，3，2，1）	MODE[3:0]	启动模式
	ON，ON，ON，ON	0000	PS JTAG
	ON，ON，OFF，ON	0010	QSPI FLASH
	ON，OFF，ON，OFF	0101	SD卡
	ON，OFF，OFF，ON	0110	EMMC

Table 17-1 SW1 startup mode configuration

18. LED lights

EdgeBoard-Lite has a two-color LED indicator (D5) on the edge of the board and three LEDs (D2, D3, D4) on the board. The red light of the two-color D5 LED is the power indicator light, and the green light is the user indicator light. The user indicator of D5 is connected to the IO of BANK25. The schematic diagram of LED lamp hardware connection is shown in Figure 18-1:

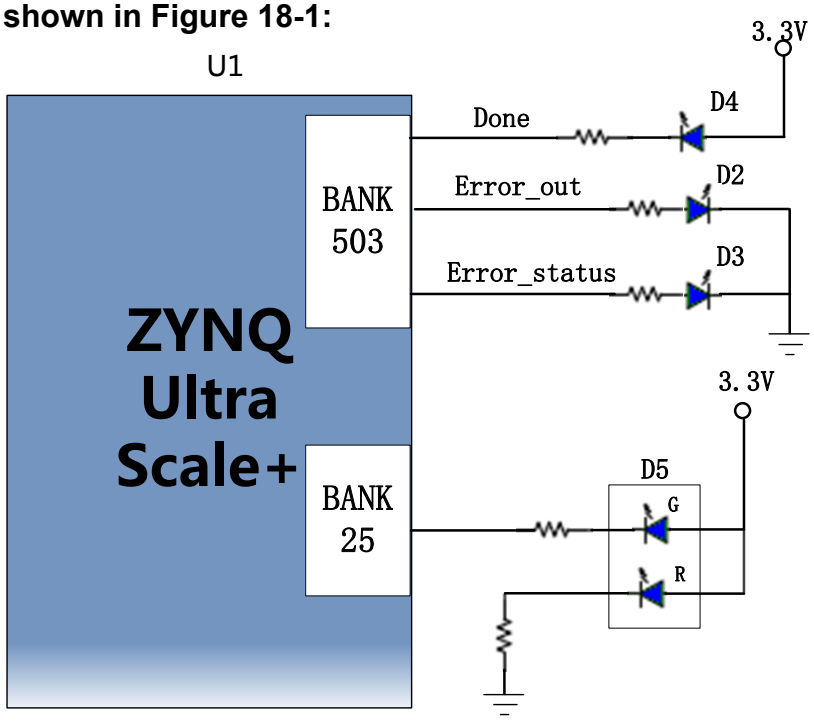


Figure 18-1 LED lamp hardware connection diagram

EEPROM pin assignment:

Signal name	Pin name	Pin number
PL_LED	IO_L10N_25	A10

19. System Clock

The RTC circuit, the PS system, and the PL logic part provide reference clocks on the board. The RTC clock is 32.768Khz, the PS system clock is 33.3333Mhz, and the PL terminal clock is 25Mhz. The schematic diagram of the clock circuit design is shown in Figure 19-1:

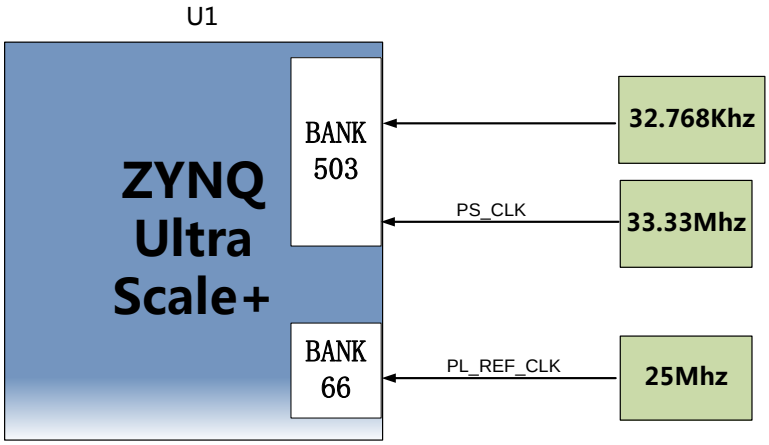


Figure 19-1 Clock source

Clock pin assignment:

Signal name	Pin name	Pin number
PL_REF_CLK	IO_L11P_66	D4

The level of PL_REF_CLK is +1.8V.

20. Fan Interface

The fan is powered by 12V, and the speed can be adjusted by the FAN_PWM signal. Fan pin assignment:

Signal name	Pin name	Pin number
FAN_PWM	IO_L10P_25	B11

21. Power Supply

EdgeBoard-Lite's power input voltage is DC12V, current 2A adapter. The direction of the power supply interface is shown in the following figure. Do not insert the positive and negative poles in reverse when using. Try to use the power adapter we provide.

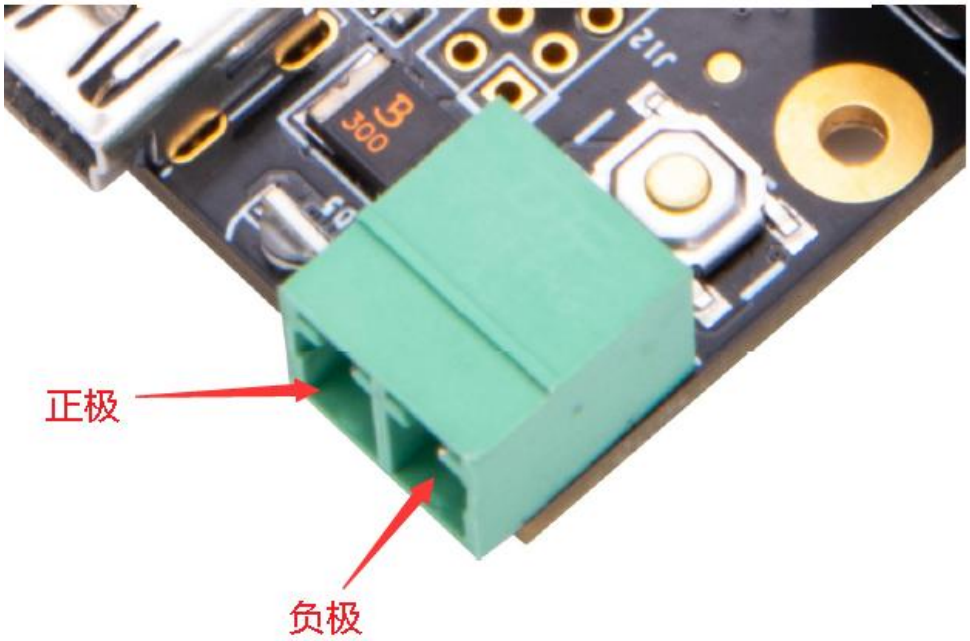


Figure 20-1 Power supply positive and negative indication

22. Structure Size Chart

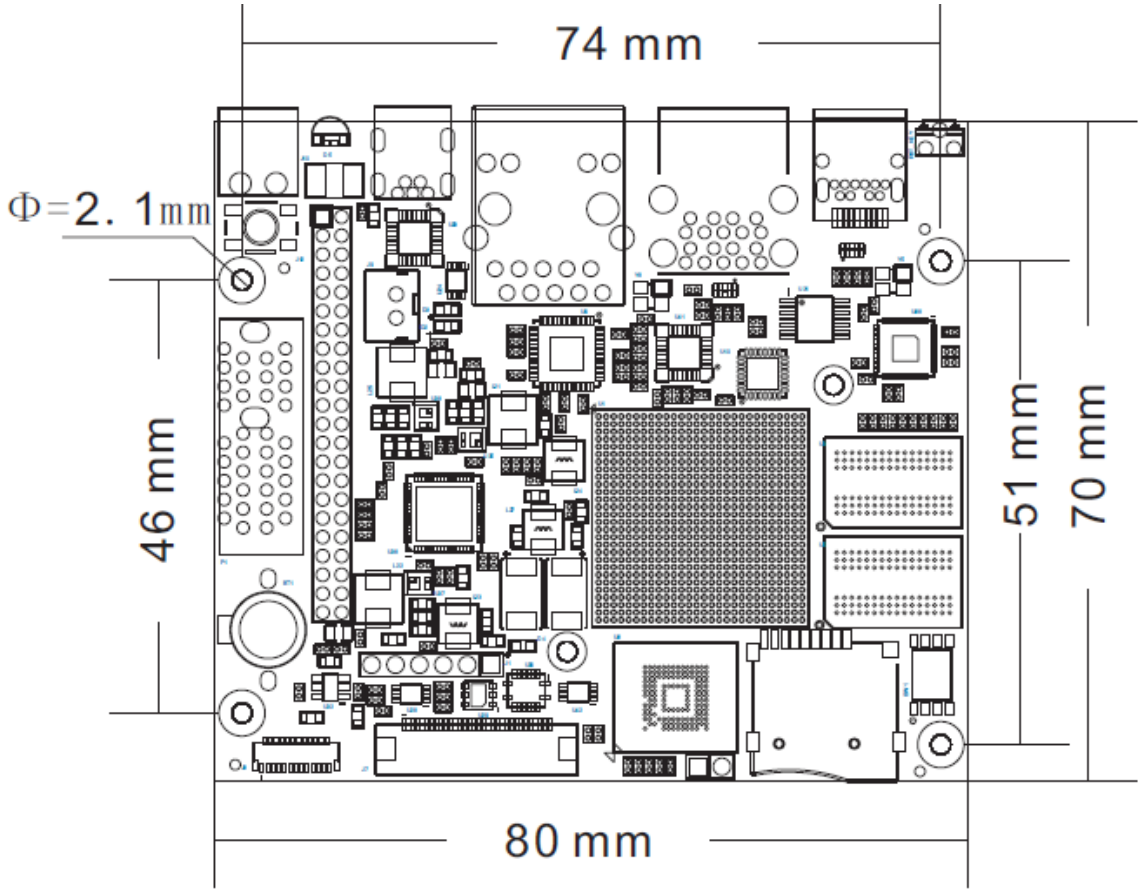


Figure 21-1 Top View