

A Report on
Two-Day Workshop on Virtual DSP Lab and
Reconfigurable Hardware

Jointly organized by,

e-Prayog Team, EE Dept., IIT Bombay and
Department of Electronics & Telecommunication
Engineering,
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On
4-5 February 2012

A Report

The Department of Electronics & Telecommunication Engineering, Sanjivani Rural Education Society's College of Engineering (SRES's COE), Kopargaon and e-Prayog Team of Wadhwani Electronics Lab from EE Dept. of IIT Bombay jointly organized a "Two-Day Workshop on Virtual DSP Lab and Reconfigurable Hardware" on February 4-5, 2012.

The said workshop was inaugurated in the Seminar hall of Training and Placement, at 10.00 am by Shri. Amit N. Kolhe, the trustee of SRES, Dr. D. N. Kyatanavar, Principal COE, Mrs. Madhumita P. Date, Project Manager- Virtual Labs (Electronics), IIT Bombay.



On the onset Prof. Mrs. A. M. Deshpande introduced the dignitaries on the dais and the team members of e-Prayog team, IIT Bombay, to the delegates from various engineering colleges, who had arrived to attend the workshop. Prof. B. S. Agarkar, Head of E&Tc Engg. Department along with other department heads felicitated the e-Prayog team members and welcome them all on behalf of Management, Principal and E&Tc Engg. Dept.



In this inaugural function, SRES's College of Engineering, Kopergaon is declared as one of the Nodal Centers of Virtual Labs (Electronics), IIT Bombay.



The inaugural function was aimed to introduce the e-Prayog and Virtual Labs Project to all the participants as well to other department faculties, which was effectively carried over by Mrs. Madhumita P. Date. In her presentation she put forth the need of the Virtual Labs, in terms of providing supporting material (which has been prepared by the team members of this project and made available on their website) to help teachers in explaining theory and help students in improving their understanding of basic and advanced concepts. In order to present what kind of supplementary material is prepared by Virtual Labs, she demonstrated examples from some labs, as how the audio-visual and remote triggered experimental set-up are to be accessed. She also appealed to all the participants to use it and make their students to use it and to give critical feed back on the same.



After inaugural function, the participants were divided into 2 groups for Virtual DSP and Reconfigurable hardware Lab Sessions. For both of the labs, total 4 sessions were conducted during these two days from morning 9.00 am to evening 6.00 pm. Total 42 participants from all over Maharashtra took part actively and were benefited.

Virtual DSP Lab Session

Total 20 participants attended Virtual DSP Lab Session. It was conducted by Mr. Samir Shelke, Mr. Narendra N. and Ms. Preeti Gopal under the guidance of Mrs. Madhumita Date.

First session started with introduction of Scilab, an open source software which was introduced by Narendra N. He introduced and elaborated various features of Scilab in comparison with MATLAB and gave away programming practice (with the help of Mr. Samir and Ms. Preeti) to the participants in it.



Amongst the highlights of the first day afternoon session was multitone generation in Scilab, followed by introduction to some of the basic operations in Image processing developed and presented by Ms. Preeti Gopal with the help of openCV library.



On the second day majority part in Virtual DSP session was conducted by Mr. Samir Shelke. The participants were given practice in 'C' programs like multitone waveform generation using 'C' as guided by Mr. Samir, Mr. Narendra and Ms. Preeti.

In the afternoon session, they conducted Generation of sine wave using DSK6713 Board, followed by detailed elaboration of remote triggering of DSP Board at IIT Bombay.

An exercise on design of chebyshev high pass filter was given to the participants for self evaluation.



Reconfigurable hardware Lab Session

Total 22 participants took part actively in Reconfigurable hardware Lab Session conducted by Mr. Debapritam Ghosh under guidance of Mrs. Madhumita Date. On first day Mr. D. Ghosh introduced the digital circuit design and the CPLD development kit (Helium board). He explained the participants the CPLD board i, building a project using Altera Quartus-II development environment, followed by downloading program using UrJTAG.



CPLDs and FPGAs- a Comparison

- CPLDs have macrocells containing the programmable hardware.
- CPLDs have programmable, non volatile interconnect.
- Non volatile hardware once configured.
- FPGAs have logic blocks (CLBs), each of lesser complexity than a macrocell, hence more in number.
- FPGAs have programmable, volatile interconnect.
- Volatile hardware configuration, hence external memory may be required.

In the afternoon session, participants were exposed to simulation of designs using Altera Quartus-II. Participants were also tested by the instructor by giving design challenges.

On the second day, during morning session, simulation of VHDL code using ghdl on Unix OS was introduced and another challenge in terms of writing VHDL/Verilog code with any digital system that will utilize around 63 macro cells of Helium board was given to the participants.

CPLD boards were used by each participant and had hands-on experience on it. In the highlights of afternoon session, both Mrs. Date Madam and Mr. Ghosh introduced to PIC 18Fxxx microcontroller kit, built in IIT Bombay. They explained programming of the same using USB. Another more interesting CPLD MAX-V series based Krypton board, developed in IIT Bombay, and was demonstrated by Mr. D. Ghosh.



Overall the workshop conducted by Mrs. Madhumita Date and her team proved to be very fruitful and encouraging.



Prof. Mrs. A. M. Deshpande
Coordinator,
Two-Day Workshop on Virtual DSP and
Reconfigurable Hardware.