ic555b.sqproj

Description

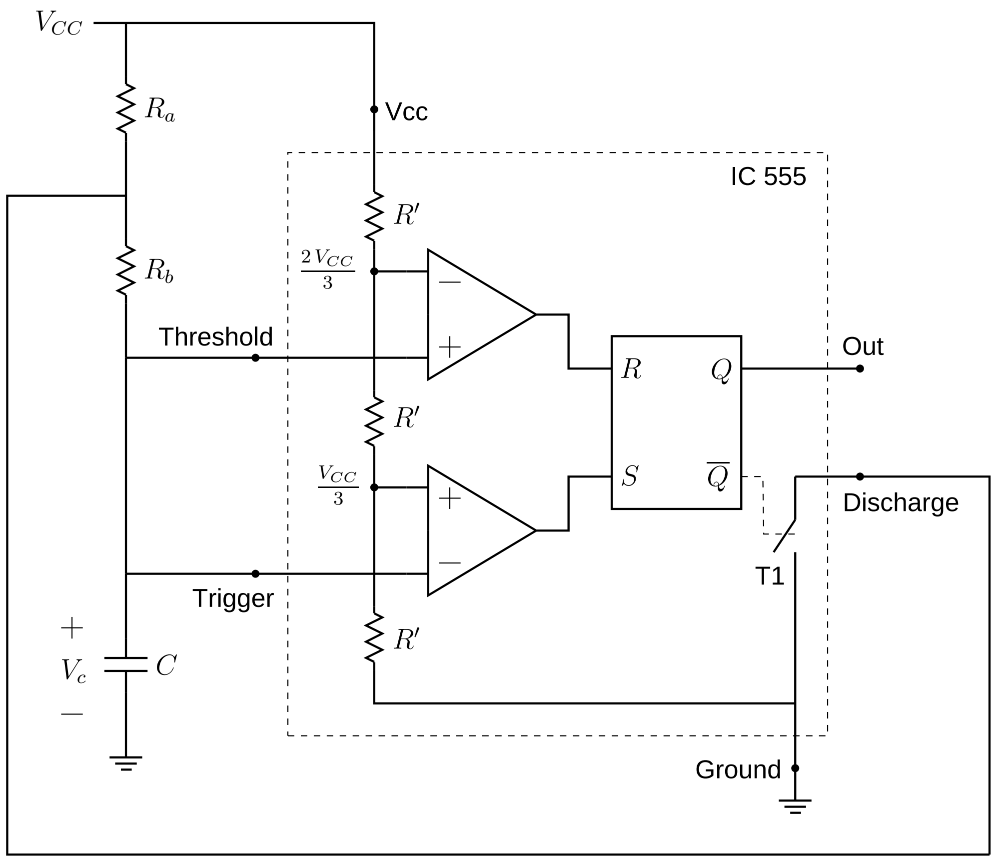

Figure 1: Astable operation of the 555 timer.

The purpose of the astable circuit shown in Fig. 1 is to produce oscillations whose frequency can be controlled by R_a, R_b, and C. The trigger and threshold inputs are tied together in this circuit, and we have $V_{\text{trigger}} = V_{\text{threshold}} = V_c$. The circuit operation can be understood by realizing that the following conditions hold:

$V_{CC}/3 < V_c(t) < 2\,V_{CC}/3$	$R=0, S=0$	flip-flop holds its state.
$V_c(t) < V_{CC}/3$	$R=0, S=1$	flip-flop is set ($Q=1$).
$V_c(t) > 2\,V_{CC}/3$	$R=1, S=0$	flip-flop is reset ($Q=0$).

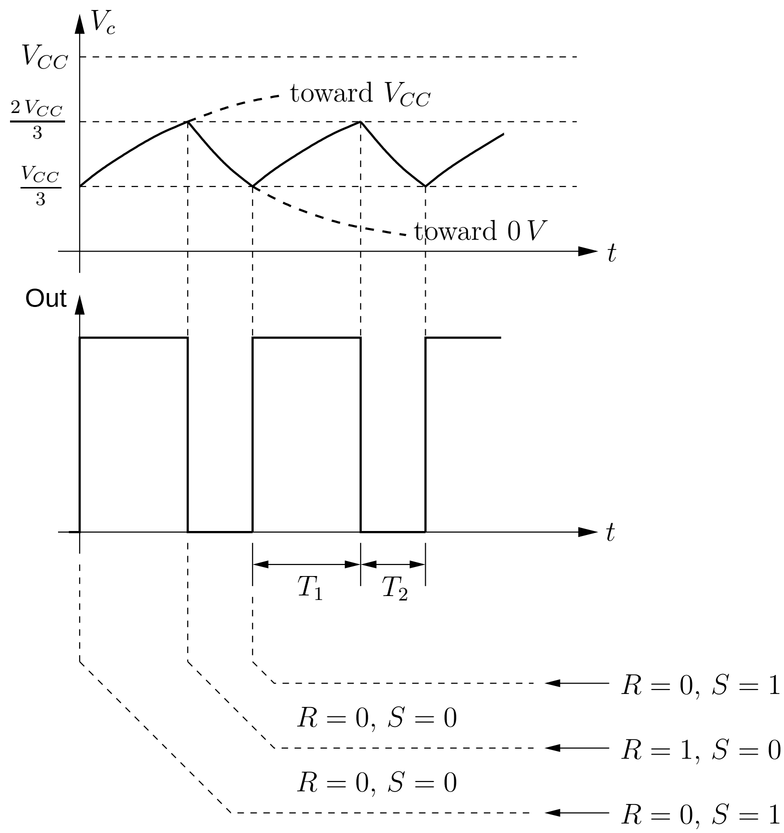

Figure 2: Waveforms for astable operation of the 555 timer.

Consider the interval marked T_1 in Fig. 2. During this time, $Q=1$, the switch T1 is open, and the capacitor charges toward V_{CC} through $(R_a + R_b)$. However, as soon as V_c reaches $2\,V_{CC}/3$, R becomes 1 (S is still 0), and the flip-flop gets reset to $Q=0$.

When Q becomes 0, $\overline{Q}$ becomes 1, and the switch T1 closes. The capacitor now starts discharging toward $0\,V$ through R_b. However, when V_c crosses $V_{CC}/3$, S becomes 1 (R is still 0), and the flip-flop gets set to $Q=1$, bringing us back to the T_1 phase. The output keeps oscillating between 0 and 1, as shown in Fig. 2.

The intervals T_1 and T_2 can be computed using the limits $V_{CC}/3$, S, $2\,V_{CC}/3$, S on $V_c(t)$ and the appropriate time constants ($\tau_1 = (R_a + R_b)\,C$ during the charging phase, and $\tau_2 = R_b C$ during the discharging phase). The result is,

$$T_1 = (R_a + R_b)\,C \ln 2\,, \tag{1}$$

$$T_2 = R_b\,C \ln 2\,. \tag{2}$$

Exercise Set

1. For $R_a = 0.5\,\text{k}\Omega$, $R_b = 0.5\,\text{k}\Omega$, and $C = 0.5\,\mu F$, calculate T_1 and T_2. Verify by simulation.

2. By simulation, obtain waveforms for V_c and Q. Compare with the expected waveforms shown in Fig. 2.

3. How will you make the output waveform nearly symmetric (i.e., $T_1 \approx T_2$)? Verify by simulation.