ee101_voltage_doubler.sqproj

Description

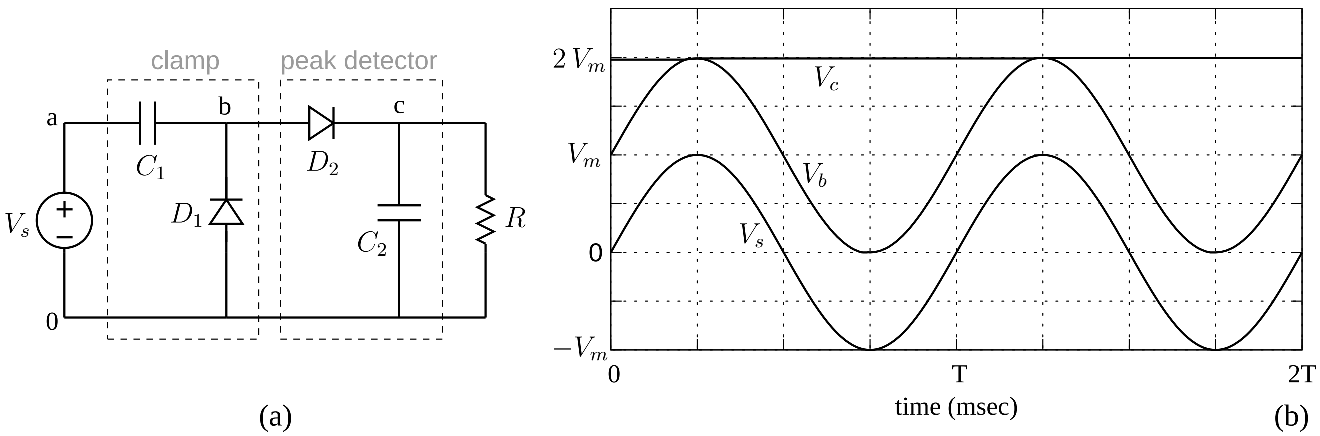

Figure 1: (a) Voltage doubler circuit, (b) Ideal waveforms with $V_{\text{on}} = 0\,V$ for the diodes, and $R \to \infty$.

Shown in Fig. 1 (a) is a voltage doubler circuit which produces a DC output voltage $V_o = 2\,V_m$ where V_m is the amplitude of the AC input voltage, $V_i(t) = V_m\,\sin\omega t$. The circuit operation can be understood if we make some simplifying assumptions: (a) V_{on} for the diodes is $0\,V$, (b) The load resistance is large, i.e., $R \to \infty$. With these assumptions, the waveforms shown in Fig. 1 (b) are obtained. The first part of the circuit serves to clamp $V_b(t)$ at $0\,V$ (as the lower limit). The second part detects the peak of this clamped voltage and holds it constant. If the resistance R is finite, it draws some current, causing a voltage drop (ripple) in V_c.

Exercise Set

1. Let $C_1 = C_2 = 1\,\mu F$, and for the voltage source, $V_m = 10\,V$ and $f = 1\,\text{kHz}$. Simulate the circuit with $V_{\text{on}} = 0\,V$ for the diodes and with a large value of R (say, $10\,\text{M}\Omega$), and verify that you get the theoretically expected waveforms shown in Fig. 1 (b).

2. What will happen to $V_c(t)$ if $V_{\text{on}} = 0.7\,V$ for the diodes? Verify with simulation.

3. Simulate the circuit with (a) $R = 100\,\text{k}\Omega$ and (b) $R = 10\,\text{k}\Omega$. Comment on your observations.

4. For $R = 10\,\mathrm{k}\Omega$, what will you do to reduce the ripple voltage at the output? Verify with simulation.