



[Design workflow management enhances SoC design quality and efficiency](#)

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Every semiconductor company and for that matter, every technology company constantly juggle a number of designs that are at different stages of development. To handle the numerous challenges, semiconductor companies in particular need to define a design workflow management system whose mechanisms adopt to a number of design and business models and can resolve the challenges of working on multiple designs from multiple locations.

Design collaboration (Figure 1) is the obvious but sometimes difficult given growing design complexity. Design teams and team members are located in different geographical regions and face complex design, data management and flow integration challenges. A tradeoff between schedule and quality is the major concern.

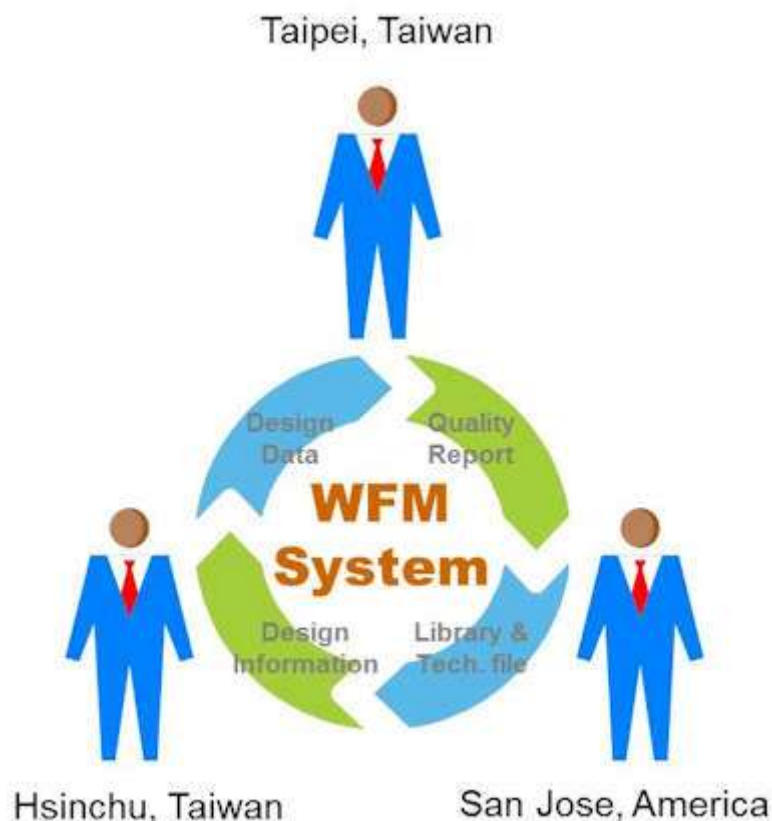


Figure 1: Design Collaboration

How do companies overcome these challenges? GUC has designed a workflow management system that may provide some insight into how to answer a number of these sticky questions.

On a strategic level, the GUC design workflow management system (WFM) is a ticket-driven design automation environment that consolidates design data version control management, technology & library management, flow/ticket packages, design task execution and design quality review into one integrated system. It automatically extracts the quality factors from EDA tool reports and evaluates the result through a series of pre-defined criteria for final design review. **Defining the workflow management system**

GUC's WFM system includes data management, library management, flow definition package, ticket execution environment, and quality control factor extraction, as shown in Figure 2.

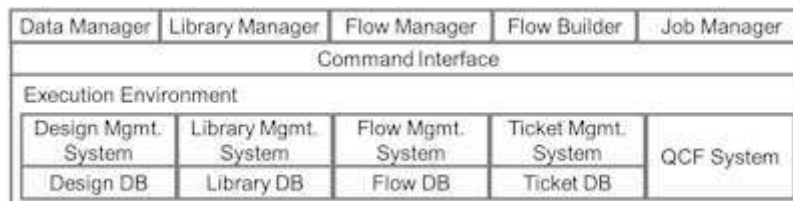


Figure 2: WFM System Architecture

The design team follows the procedures shown in Figure 3. At the project's start, the project leader checks the library and technology files into the library database, then defines the design name, job stages and version name in the data repository. At each stage, the project leader prepares the flow package with a ticket template. Any member of the project team can checkout the ticket file from the repository and execute the specific task requested by project leader. When completed, the team can review design quality on WFM GUI. If the quality meets the criteria, project members can check the results into the design database and continue to the next task.

When collaborating across different geographical regions, WFM automatically transfers design data to the other regions. A user checks the design data into the local WFM Design Database and WFM automatically sends and checks it into the other regions.

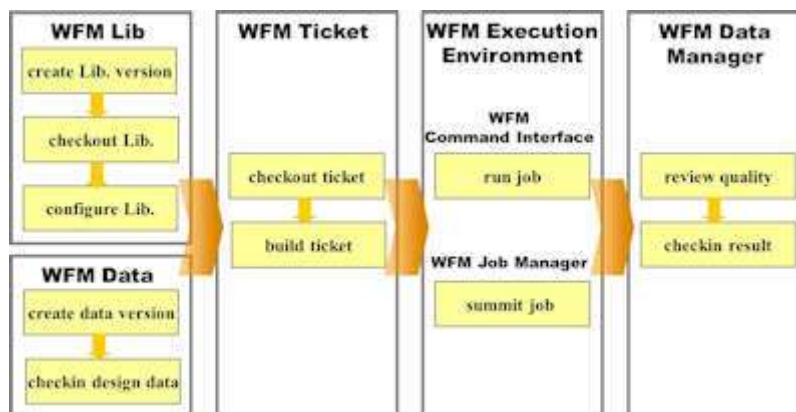


Figure 3: WFM Working Procedures

Flow definition package

To get consistent design quality across different projects, flow engineers can pre-implement the flow template (Figure 4). The main purpose of a WFM system is to let designers smoothly complete their jobs even when the designer is junior with limited experience. In the WFM system, there are collections of pre-developed flow definition packages. Each flow package represents a single execution step in the complete design flow. Each flow step could either be executed individually or combined with other flow steps to form a more complex flow. These flow packages are usually prepared by the flow engineers or senior design members and encapsulate valuable design know-how. A flow package contains parameterized tool scripts, job control mechanism and associated quality control factors.

Flow engineers need prepare four actions for each flow step, as shown in Figure 5. A “Pre-Check” action checks the inputted files for the job needs. Flow engineers also prepare EDA tool scripts for Job Execution action. A “Post-Check” action checks the EDA tool’s error and report. Then, a “QCF Extraction” action extracts QCF, Quality Control Factor. (Figure 6)

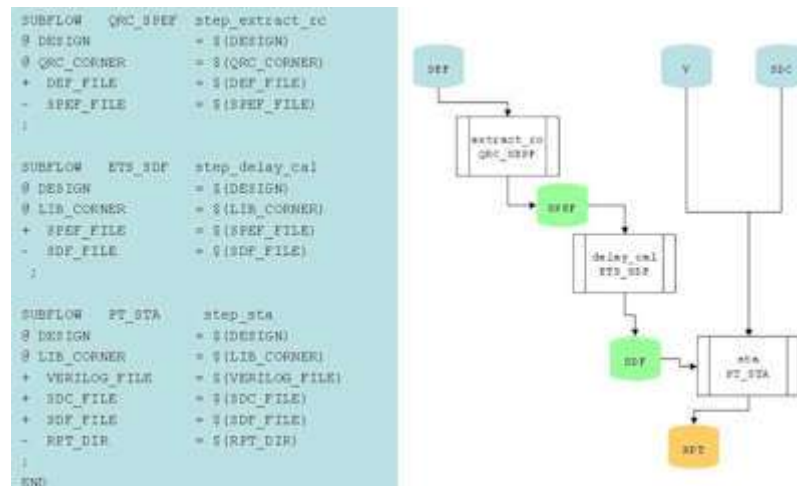


Figure 4: WFM Flow Definition Example

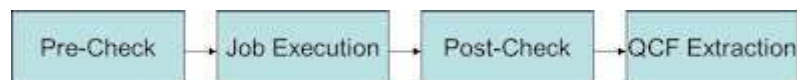


Figure 5: Actions of Flow Step

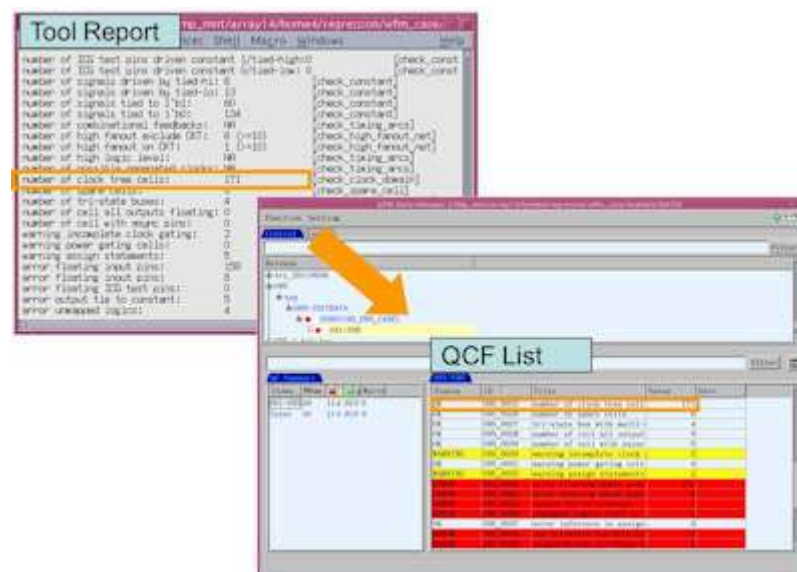


Figure 6: QCF Extraction

Technology and library management

At GUC, for example, the project leader prepares technology and library files for the project team. This step maintains a centralized database of all design libraries and technology files. Each project has its own library configuration file that is created by the project leader and shared by all team members. A library configuration file describes the design's IP libraries. Designers only need to specify the library configuration file in the system and no longer have to prepare library setting for tools by their own.

WFM Library Manager provides a convenient environment and the project leader can use it to review and modify library's configuration easily. (Figure 7)

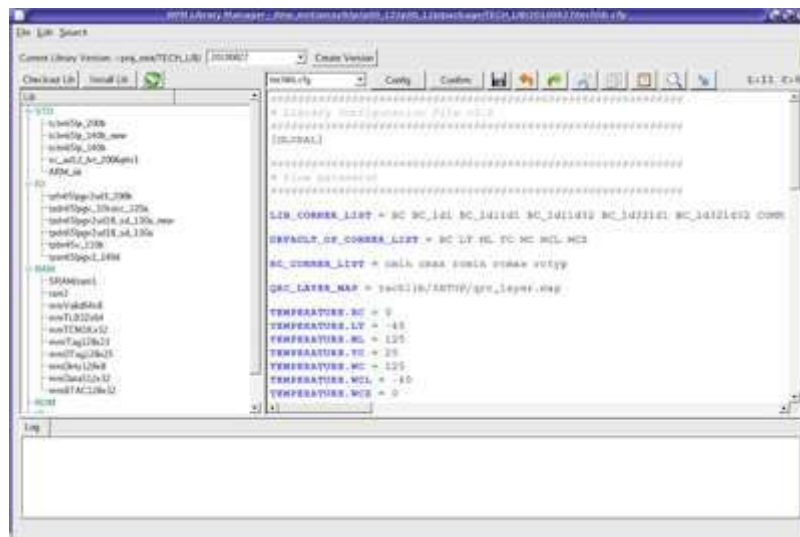


Figure 7: WFM Library Manager

Design data management

Before executing their jobs, project team members need to arrange their design data in a unified design data directory structure provided by WFM, as shown in Figure 8. It is a four layer hierarchical structure that reflects the design and job progress. The first layer is the design stage layer, such as trial, stable and final. The second layer is the design name layer. Designers can partition their design on this layer. The 3rd layer is the job stage layer. The 4th layer identifies a job stage's version. Figure 9 shows these job stages.

Users can easily explore the design data and trace the design history with a built-in version control mechanism. An important feature of WFM Data Management is that it can advise users the correct input data they need for each design stage. When integrated with the ticket execution mechanism, WFM can automatically pick up the correct data. This reduces the chance of making mistakes by using the wrong data.

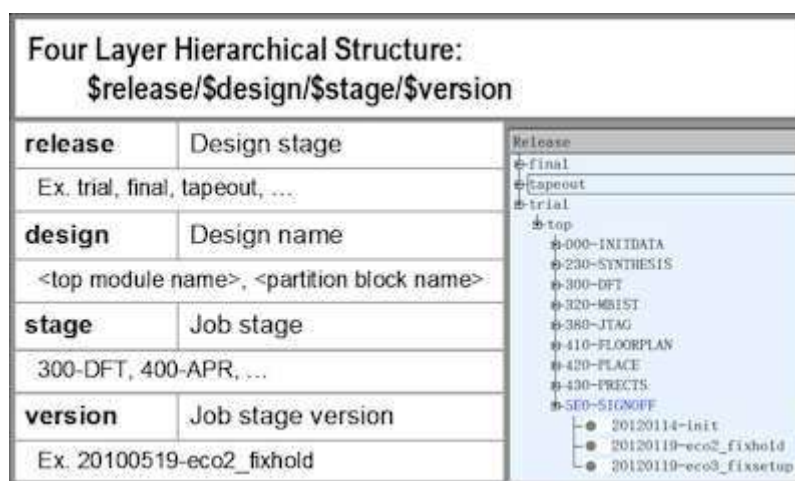


Figure 8: Directory Structure of WFM Design Data

000-INITDATA	400-APR	500-TIMING
100-CIRCUIT	410-FLOORPLAN	510-POSTSIM
200-FUNCTION	420-PLACE	590-SIGNOFF
210-RTL	430-PRECTS	600-POWER
230-SYNTHESIS	440-CTS	700-TAPEOUT
240-LEC	450-POSTCTS	800-TESTING
241-CLP	460-ROUTE	900-PACKAGE
250-PRESTA	470-POSTROUTE	
260-PRESIM	495-ASSEMBLE	
300-DFT_INIT		
310-MBIST		
320-MACROPOWERDOWN		
330-MACROBYPASS		
340-SCAN		
350-ATPG		
360-LOGICBIST		
370-JTAG		

Figure 9: WFM Job Stage

Members of the project team can use WFM Data Manager to maintain design data and the project leader can easily review the project progress on the GUI. An example is shown in Figure 10.

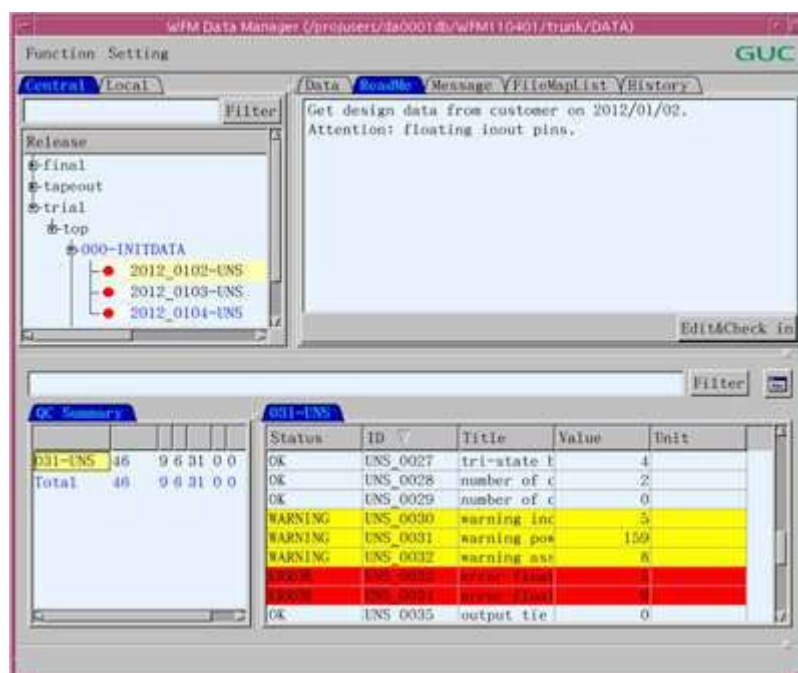


Figure 10: WFM Data Manager

Ticket execution environment

After preparing library files and design data, members of the project team can take tickets for design steps, such as Synthesis, LEC, CTS, or STA from a Ticket Data Base. The ticket file is a task description file (See Figure 11) that contains the following information:

- Where is the input and output data
- What to do with predefined flow
- Associated flow parameters to execute the task

The WFM system reads the above information and creates an EDA tool execution environment. It actually generates a make file based execution environment that automatically handles job dependency. WFM will record the job running environment and setting, so designers can easily track their jobs result and source data. WFM system can link with a Sun Grid Engine for job queuing control, but it can be easily ported to any other job queue system like LSF. Users can use WFM Job Manager to execute and monitor design jobs. WFM Job Manager is a GUI that visualizes the job dependency, control job execution and monitor job status (Figure 12).


```

[HEADER]
TICKET_ID      = T5E0_MMMC_FLAT_TIMING
TICKET_TITLE   = "MMMC RC-to-STA Timing Signoff"
TICKET_USER    =
TICKET_FLOW    = 5E0-MMMC_FLAT_TIMING
#####Please modify below setting#####
TICKET_LIB     = CLN65LP_MMMC_SIGNOFF_CASE1/techlib.cfg
TICKET_DESIGN  = MMMC_SIGNOFF/PS_TOP
TICKET_DBSRC   = 590-SIGNOFF/2012_0428_SIGNOFF_CASE1
TICKET_DBDEST  = 590-SIGNOFF/2012_0428_SIGNOFF_CASE1
TOP_MODULE     = PS_TOP

[PARAMETER]
#####
## set User specify OCV_MAX, OCV_MIN value
## If STA_USER_SPECIFY_OCV=true, STA_USER_OCV_MAX,
STA_USER_OCV_MIN are valid.
## If STA_USER_SPECIFY_OCV=false, STA_USER_OCV_MAX,
STA_USER_OCV_MIN are invalid.
## Format: STA_USER_OCV_MAX = [user_specify_value]
##       STA_USER_OCV_MIN = [user_specify_value]
#####
#@WFM EXPAND TIMING_ANALYSIS BEGIN
#@WFM KEY Constraint_mode Timing_environment RC_CORNER
Operation_condition
STA_USER_OCV_MAX_SETUP_PMrtonly_PMstandby_cmax_TC = 1.0
STA_USER_OCV_MIN_SETUP_PMrtonly_PMstandby_cmax_TC = 0.92
STA_USER_OCV_MAX_HOLD_PMrtonly_PMstandby_cmax_TC = 1.0
STA_USER_OCV_MIN_HOLD_PMrtonly_PMstandby_cmax_TC = 0.92

```

Figure 11: WFM Ticket File Example

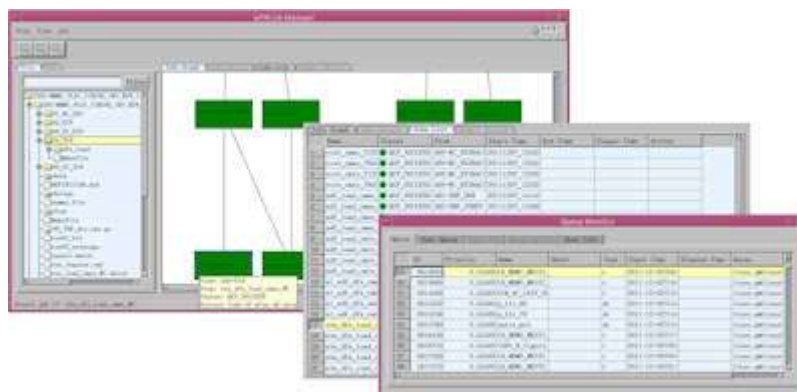


Figure 12: WFM Ticket Execution and Job Manager

Quality control factor

At each design stage, designers have to look for several quality checking items in the tool report. WFM provides a quality control mechanism that systematically monitors the design quality. After executing each step, WFM automatically extracts quality control factors (QCF) from EDA tool reports and log files. The QCFs are defined in WFM flow definition package and includes such items as the number of floating pin, the number of slack violation path, and other similar details.

WFM also provides graphic user interfaces. The WFM Data Manager can analyze design quality, summarize the quality control factors .and then highlight the job stage version with a circle mark. If the tool result needs to be debugged, WFM will highlight the job stage version with a red circle mark. If there is something else that needs to be check, the job stage will be marked with a yellow circle. This way, users can quickly review the design quality (Figure 13). WFM automatically transfers design data to other geographic regions, so the project leader can easily review the quality of job stage versions implemented by the other regions' engineers.



Summary

To meet aggressive design schedules while ensuring the design quality, companies should have a flow and data management system. The ideal system integrates unified design data and library management, reusable flow script package, EDA tool execution environment and quality control factor extraction. The consistent working model helps cross-region engineers smoothly collaborate to increase the design team's overall productivity. Ultimately, the system helps designers avoid mistakes caused by applying wrong data or settings.

One GUC project developed through it was a 40nm GPS chip. It contains about 7 million equivalent logic gates. For multi mode multi corner timing analysis, there were 5 function modes, 4 timing environments, 5 RC corners, 3 setup-time and 13 hold-time library signoff corners. In the past, designers had to prepare many scripts for RC extraction, delay calculation, STA, and SI jobs, and they also had to arrange the dependency relation between the job's data.

The WFM system automatically associated design data and constraint files for each MMMC job and built their dependency graph (see Figure 14). Thus, designers could easily execute these jobs from the WFM GUI. The project adopted WFM system to handle the timing signoff jobs and completed them on schedule. It was a successful experience. In the first year, there is only 20% of GUC's projects adopted this system. Now, almost all projects adopt WFM. To date, GUC has taped out more than 70 designs that were run through the WFM system. The devices targeted a number of manufacturing processes ranging from 28nm to 90 nm. The systematic working model improved both project quality and schedule control.

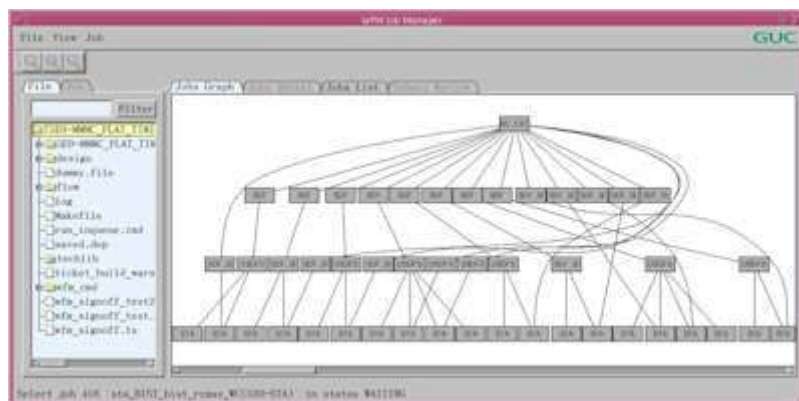


Figure 14: MMC Timing Signoff Job Dependency Graph

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