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Implementation of Multi-Channel Time-to-Digital Converter using FPGA

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Abstract

- This project deals with the design and implementation of a Multi-channel Time-to-Digital Converter (TDC) to measure time intervals with a picosecond level resolution.
- The hybrid counter designed for measuring the time interval uses a combination of a coarse counter and a fine counter technique .
- The coarse counter provides a longer measuring range whereas the fine counter provides the precision required in the concerned conditions. Thus, this design is efficient and reliable. Fpga is used to implement the above design.
- Using a HDL, FPGAs can be designed to meet the needs of the developer. This is beneficial to the project since it provides: high parallel processing capabilities, high reconfiguration, flexibility less development time.
- The embedded system developed for this research is planned to be integrated with the TIFR's GRAPES-3 experiment. As a result, it's built to handle enormous amounts of data efficiently during communication and processing. Finally, the suggested FPGA-based TDC system is combined with a UART module to allow for smooth data transmission to and from the end user.

Introduction

Background

- The earth's atmosphere is blasted on a daily basis by cosmic rays, and these deviate on colliding with neutrons in the atmosphere. This produces large air showers, which are a spray of particles.
- As a result, when the ray reaches ground level, the air spray created by a single ray covers a broad region. The detection and observation of these air showers is carried out using huge muon detectors installed at ground level.
- The study of cosmic rays in different regions of the Galaxy can be aided by the detection of diffuse Galactic gamma ray flux. The abundance and spectrum shape of relativistic particles in the Milky Way are encoded in the energy and angular distributions of photons.

Introduction

Background

The GRAPES-3 experiment in Ooty, India, began as a cooperation between Mumbai's Tata Institute of Fundamental Research and Osaka City University in Japan.



Introduction

Background

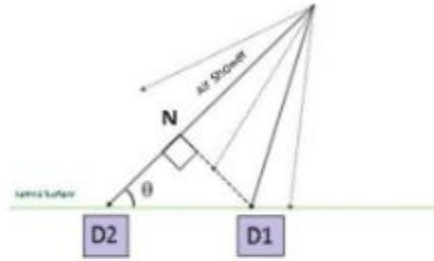


Figure 1.1: Detection of Air Showers

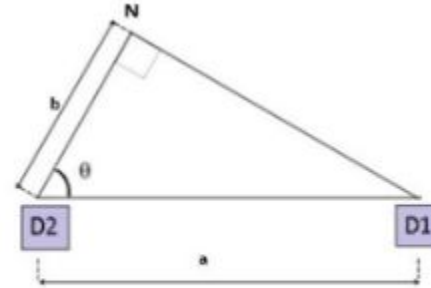


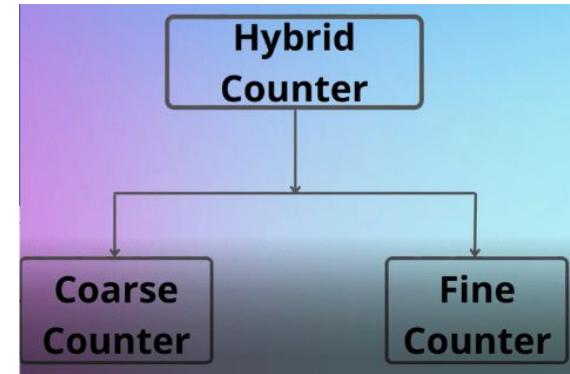
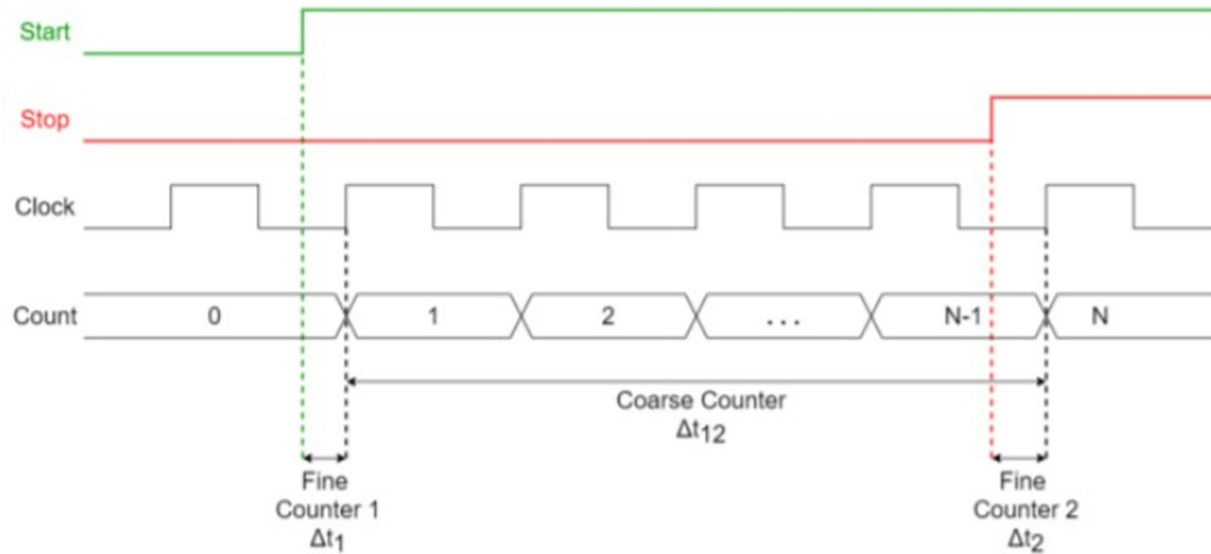
Figure 1.2: Calculating the Angle of Incidence of Cosmic Ray Air Shower

$$\theta = \cos^{-1} \frac{b}{a} = \cos^{-1} \frac{v \cdot \Delta t}{a}$$

v = velocity of the ray (known)

Δt = time measured by TDC

TDC-Nutt Interpolation Method



Requirements

- Phase shifted clock

This clocks are created Using internal MMCM module.

- MMCM

The MMCM Module takes an input clock named CLKIN1, and generates several output clocks, each of which can be configured to have a different frequency that is dependent on the input clock frequency.

Cascading MMCM

- Why cascading?

To improve the precision of TDC.

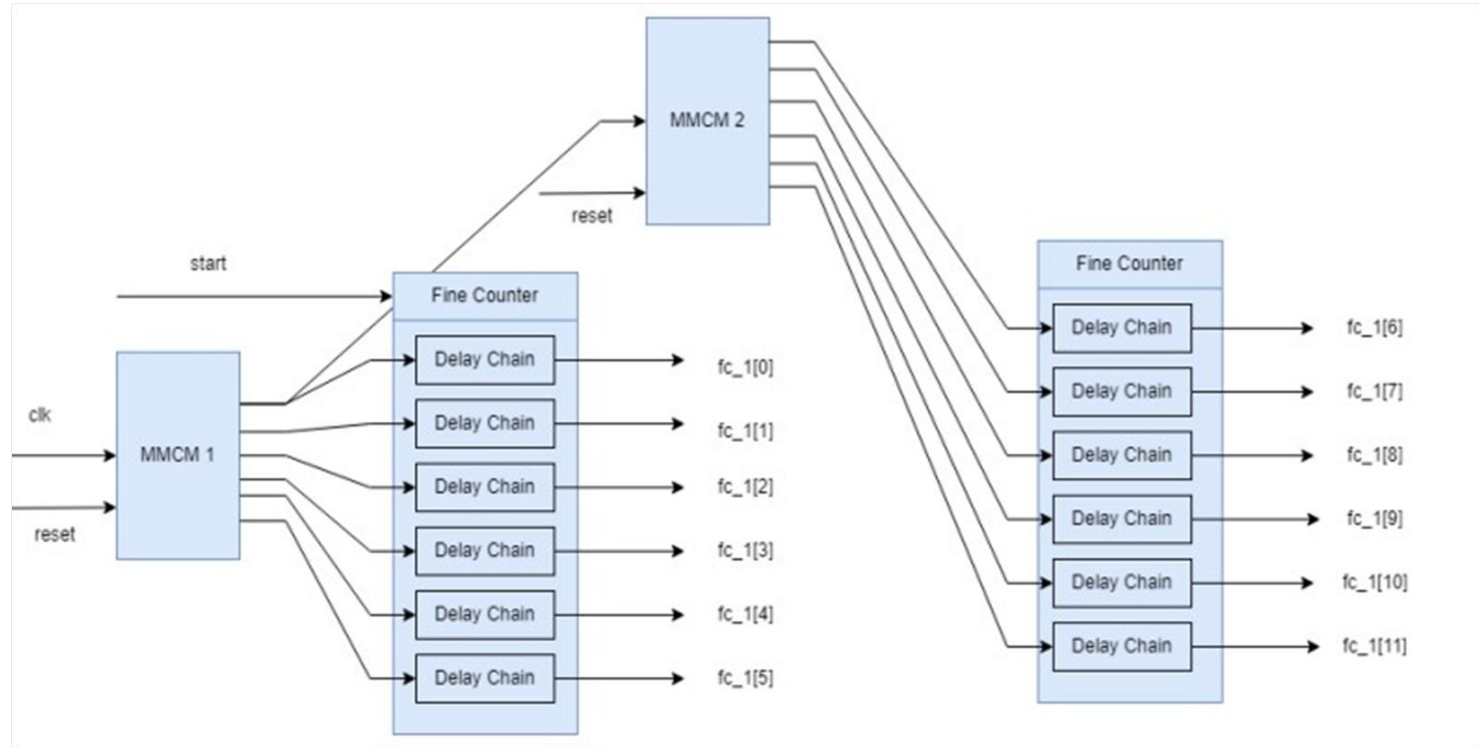
- How?

Generate 6 op from first MMCM & next 6 from the second MMCM, the input for first MMCM is given as primary input(100MHz) and the for the second MMCM the input is given as one of the clock from the first MMCM

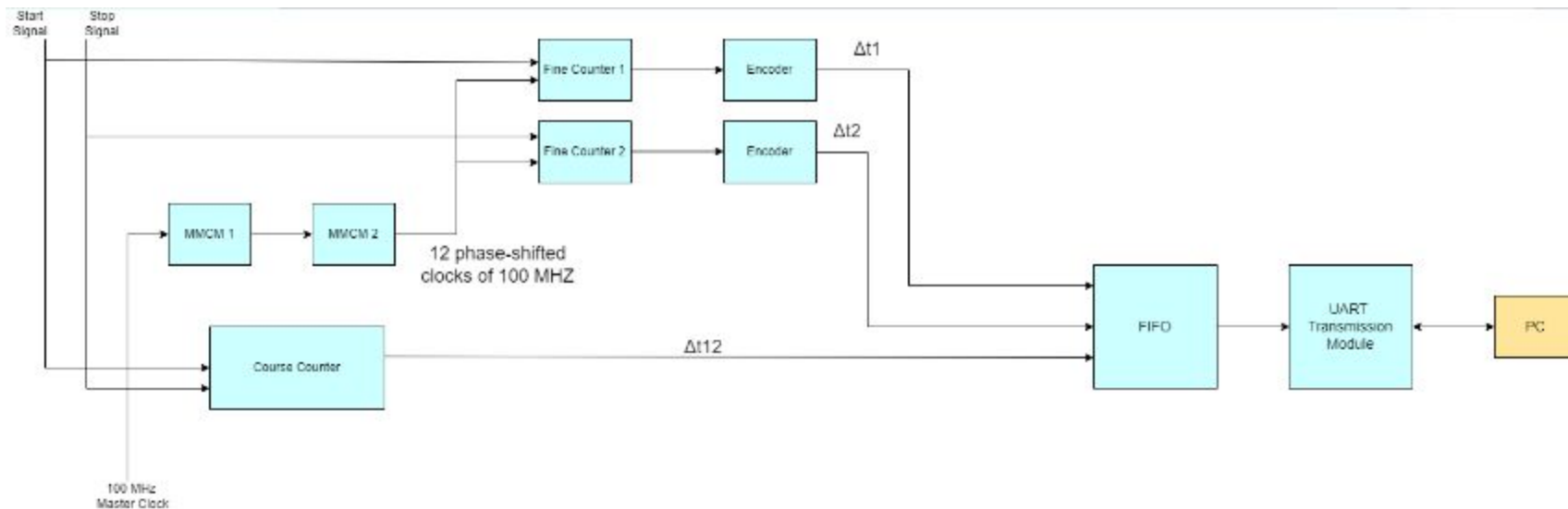
- Phase Difference

We are generating 100 MHz clocks with 30° phase shift

Cascading MMCM

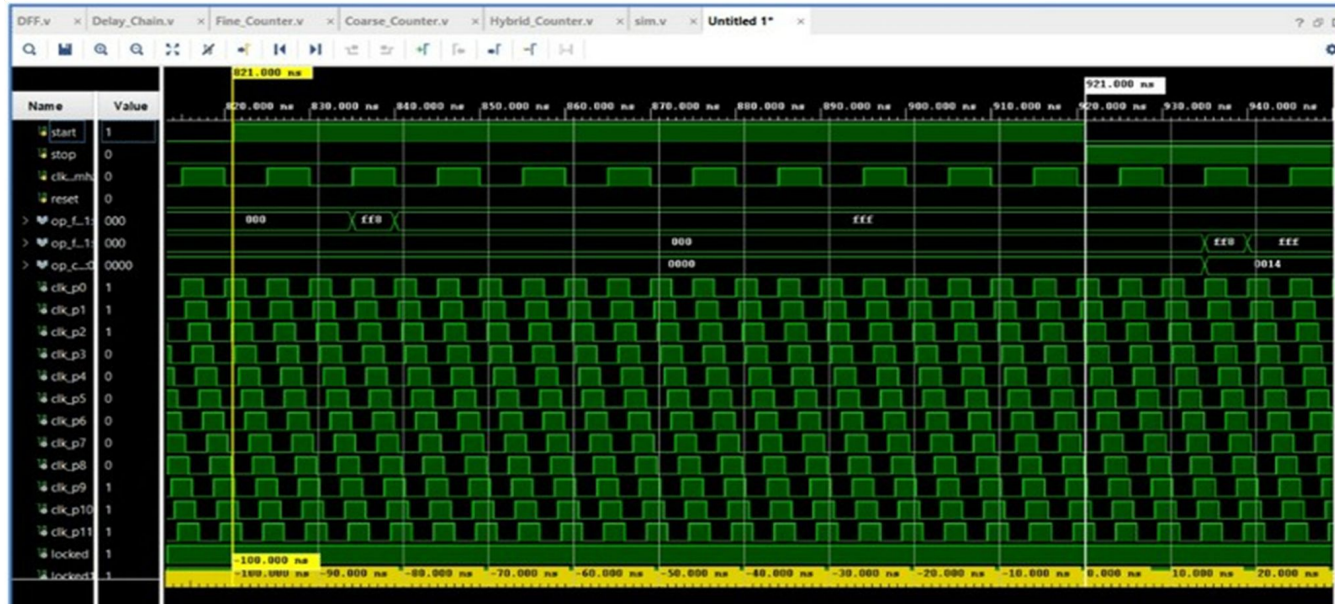


Block Diagram of TDC



12-Bit Phase Shift

- We have implemented 12-bit phase shift, with 30° phase shift.



Go About

- 12 bit output of 100 MHz
- Used 2 delays in the delay chain and a latch all the 12 bit outputs at first clock output

Simulation Flow

- Start / Stop

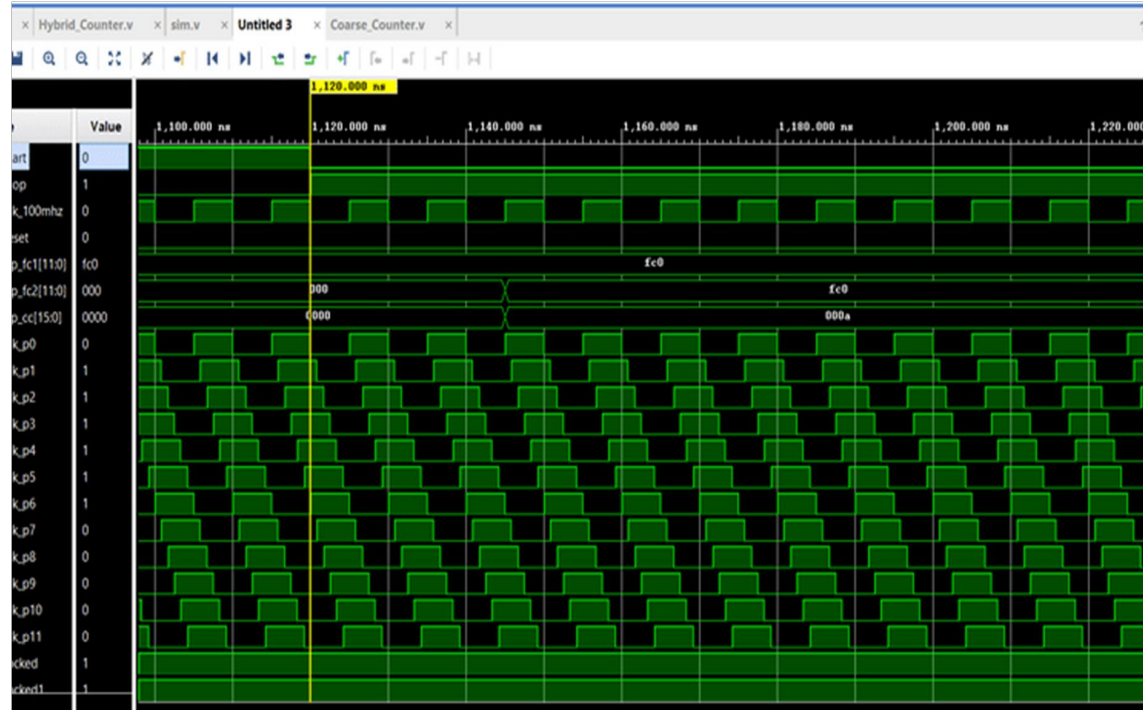
Start signal is given at 1020ns
and stop is at 1120ns

- Fine Counter

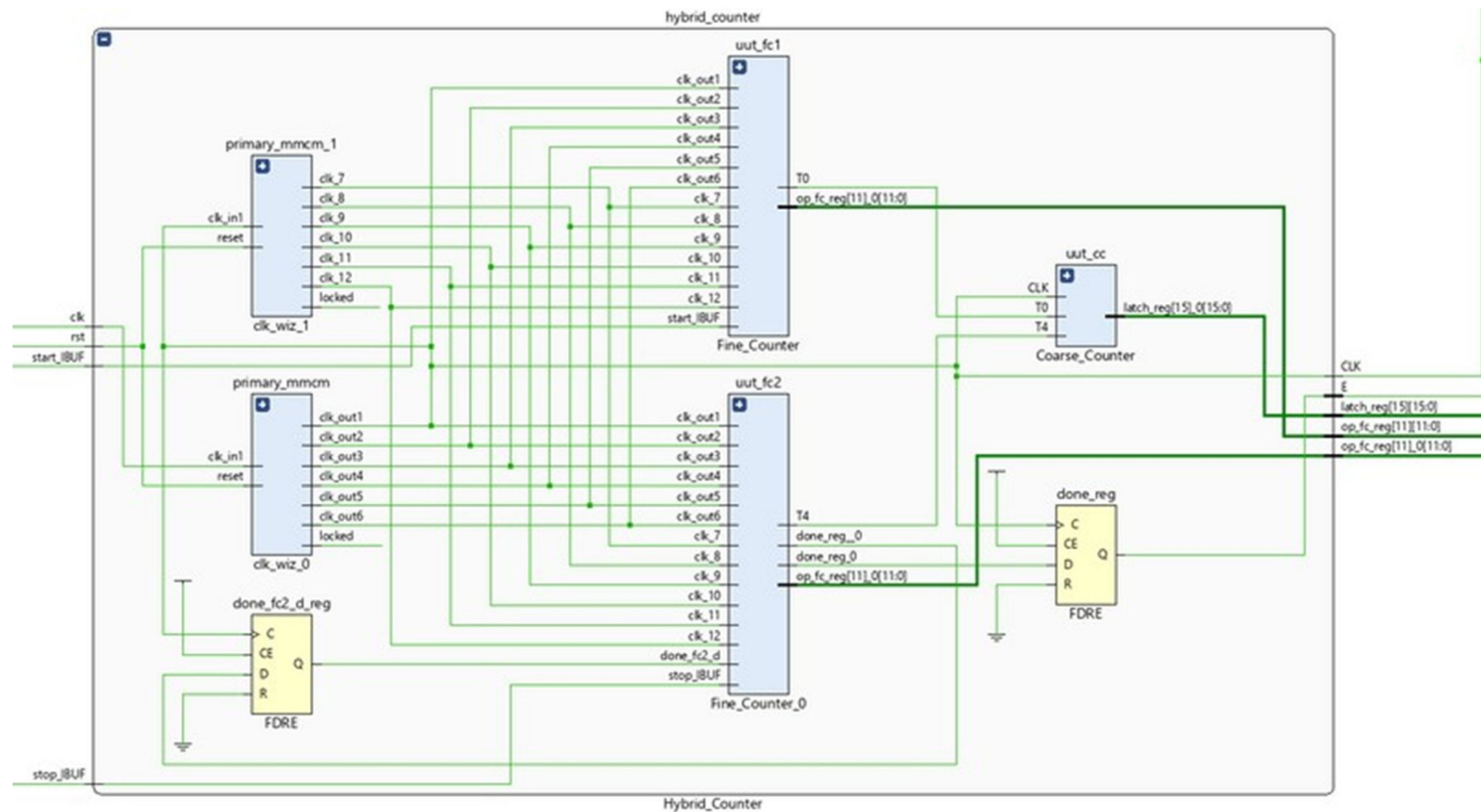
There are two fine counters with
fc0 as output.

- Coarse Counter

The coarse counter values are
latched and we get the output
after the stop signal goes high.
The output is 000a.



Schematic Diagram



Conclusion

- The examination of various methodologies and equipment used to implement coarse counters, fine counters, and time-to-digital converters is described in this research.
- The benefits of TDCs based on FPGAs are underlined and described. Thus this paper covers all the details regarding the cascaded MMCM setup and the successful simulation hybrid counter.
- Our goal of achieving the 12 phase hybrid counter simulation is achieved. The experiment can be further extended to design a customized hybrid counter to achieve a better precision.

ACKNOWLEDGMENT

- We would like to express our gratitude to our project supervisor Mr. Irfan Mirza (TIFR) and Dr. Raghunandan Shukla who have guided us throughout this project.
- We also wish to acknowledge the help provided by the TIFR team and the technical staff at the Department of Computer Engineering, Fr. C. Rodrigues Institute of Technology.

References

- <https://www.prowesscorp.com/what-is-fpga/>
- B. Hariharan, S. Ahmad, M. Chakraborty, A. Chandra, S. R. Dugad, S. K. Gupta, Y. Hayashi, H. Kojima, S. S. R. Inbanathan, P. Jagadeesan, and et al., "Energy sensitivity of the grapes-3 eas array for primary cosmic ray protons," *Experimental Astronomy*, vol. 50, p. 185{198, Sep 2020.
- <https://www.elprocus.com/fpga-architecture-and-applications/>
- 2011 IEEE Nuclear Science Symposium Conference Record NP2.S-147A Multichannel High-Resolution «5 ps RMS between two channels) Time-to-Digital Converter (TDC) Implemented in a Field Programmable Gate Array (FPGA) by Eugen Bayer, Peter Zipf and Michael Traxler
- <https://www.ni.com/documentation/en/labview-comms/5.0/fpga-targets/configurable-logic-blocks/>
- Low resource FPGA-based Time to Digital Converter by Alessandro Balla, Matteo Beretta, Paolo Ciambone, Maurizio Gatta, Francesco Gonnella, Lorenzo Iafolla, Matteo Mascolo, Roberto Messi, Dario Moricciani, Domenico Riondino
- <https://www.ourpcb.com/fpga-vs-microcontroller.html>
- A Multi-Channel, I/Os Resolution, FPGA-Based TDC with 300MS/s Throughput for Open-Source PET Applications by Harmen Menninga, Claudio Favi, Matthew W. Fishburn Student Member, IEEE, and Edoardo Charbon Sr. Member, IEEE
- <https://www.eetimes.com/all-about-fpgas/#>
- Pico-TDC: a novel FPGA-based TDC with 2.2ps RMS timing resolution T. Sui, Z. Zhao, S. Xie, Q. Huang*, J. Xu*, and Q. Peng*
- <https://digilent.com/blog/fpga-configurable-logic-block/>
- <https://digilent.com/reference/programmable-logic/nexys-a7/reference-manual?redirect=1>
- https://www.xilinx.com/content/dam/xilinx/support/documentation/ip_documentation/mmcm_module.pdf

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