Implementation of Multi-Channel Time-to-Digital Converter using FPGA

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***Abstract*—The cosmic rays consisting of high energy particles travel from the cosmos, and creates a shower of particles called air showers, mainly consisting of leptons and gamma rays. The detection of these showers is conducted by placing large muon detectors at ground level. The energy and angular distributions of the photons encode information about the density and spectral shape of relativistic particles in the entire Milky Way.The GRAPES-3 experiment at Ooty, India is involved in the study of these cosmic rays. The experiment is designed to detect and study cosmic rays with an array of air shower detectors and a large area muon detector.The TDC is a necessary step for learning more about cosmic rays in different regions of the galaxy.The angular distributions of the photons are used to discover information about the density and spectral shape of relativistic particles in the entire Milky Way. Thus, this project plays a small, but vital role in understanding various aspects of the universe from the tiny spec called Earth.The aim of our project is to design and implement a multi-channel time-to-digital converter (TDC) using a Field Programmable Gate Array (FPGA). The designed hybrid counter will enable the precise measurement of time intervals between two signals (start and stop) with an accuracy of sub-nanoseconds.**

***Index Terms*—TDC, FPGA, Course Counter, Fine Counter, MMCM, Hybrid Counter**

I. Introduction

A. Background

The earth's atmosphere is blasted on a daily basis by cosmic rays, which are high-energy particles that travel from the sun or further out in the universe. When a primary energetic particle enters the Earth's atmosphere, it collides with nuclei and molecules, producing secondary particles that share the energy of the original primary particle. The secondary particles continue to propagate, decay, and form new particles. This produces large air showers, which are a spray of particles. Leptons (muons, electrons, neutrinos) and gamma rays make up the majority of these showers. [1] As a result, when the ray reaches ground level, the air spray created by a single ray covers a broad region.

The study of cosmic rays in different regions of the Galaxy can be aided by the detection of diffuse Galactic gamma ray flux. The abundance and spectrum shape of relativistic particles in the Milky Way are encoded in the energy and angular distributions of photons. The GRAPES-3 experiment in Ooty, India, began as a cooperation between Mumbai's Tata Institute of Fundamental Research and Osaka City University in Japan. It is presently a collaboration between numerous Indian and Japanese institutes. An array of air shower detectors and a large area muon detector are used in the experiment to detect and analyse cosmic rays. Currently, approximately 400 scintillators spanning a total area of 25,000 m² are recording observations that identify charged particles in large air showers caused by high-energy cosmic ray interaction in the atmosphere. The GRAPES-3 experiment will investigate the following topics:

- In the galaxy and beyond, the origin, acceleration, and spread of $>$1014 eV cosmic rays.
- Existence of "Knee" in the cosmic ray energy spectrum.
- Production and/or acceleration of the universe's highest energy ($approx 1020eV$) cosmic rays.
- Multi-TeV -ray astronomy from neutron stars and other compact objects.
- The Sun is the nearest astrophysical object, acting as an accelerator of energetic particles and having an impact on Earth.

The angle of incidence of cosmic rays is crucial in determining the distance to the rays' source. The wavefront of rays originating from a faraway source reaches the Earth's surface with a very high radius curvature. The angle of incidence of the beams may be computed using trigonometry because this wavefront is a straight line. The graphic that can be used to determine the angle of incidence θ is as follows:

$\theta = \cos^{-1} \frac{b}{a} = \cos^{-1} v.\Delta t / a$
v = the ray's velocity (known)
Δt = time measured by TDC

B. Motivation

In a variety of high-energy physical experiments, such as examining subatomic fine structure in fixed target studies and collision experiments, precise time interval measurements are frequently required. It is employed in this case as part of a wider experiment to observe and investigate diffuse galactic ray flux. The TDC is a prerequisite for understanding more about cosmic rays in various parts of the cosmos. The photons' angular distributions are utilised to learn about the density and spectral shape of relativistic particles throughout the Milky Way. As a result, this initiative plays a minor but critical role in gaining a better understanding of the universe from the tiny spot named Earth. This influenced our decision to work on this project.

C. Aim and Objective

This project will use a Field Programmable Gate Array to develop and implement a multi-channel time-to-digital converter (TDC) (FPGA). With sub-nanosecond precision, the developed Hybrid Counter will be able to measure time intervals between two signals (start and stop). The UART protocol is used to efficiently communicate readings from the FPGA to the end user.

D. Report Outline

The goal of the project is to measure the time intervals between detection of rays at adjacent light sensors precisely and accurately. This project deals with the design and implementation of a multi-channel time-to-digital converter (TDC) to measure and transmit these time intervals. The hybrid counter designed for measuring the time interval uses a combination of the coarse counter and the fine counter technique. The coarse counter provides a longer measuring range whereas the fine counter provides the precision required in the concerned conditions.Thus, this combined design is efficient and suitable for attaining a TDC with pico-second level resolution.

II. Literature Survey

A. Low resource FPGA-based Time to Digital Converter

Authors: Alessandro Balla, Matteo Beretta, Paolo Ciambrone, Maurizio Gatta, Francesco Gonnella, Lorenzo Iafolla, Matteo Mascolo, Roberto Messi, Dario Moricciani, Domenico Riondino

They devised and implemented a 32-channel TDC with a precision of 255 ps and low non-linearity effects on a Xilinx Virtex-5 FPGA in this article. Due to the need for a specialised data collecting system and interface, the system was constructed on the FPGA. The Nutt interpolation method and 4xOver-sampling technology were employed in the TDC's architecture. Integral Non-Linearity (INL) is the divergence of the input-output characteristic from the ideal straight line, whereas Differential Non-Linearity (DNL) is the deviation of a single quantization step from the ideal value of 1 Last Significant Bit (LSB). This work was examined in order to learn more about differential and integral non-linearity, as well as their testing and outcomes. [1]

B. Pico-TDC: a novel FPGA-based TDC with 2.2ps RMS timing resolution

Authors: T. Sui[1], Z. Zhao[2], S. Xie[1], Q. Huang[2], J. Xu[1], Q. Peng[3]

[1] Huazhong University of Science and Technology, Wuhan, China

[2] Shanghai Jiaotong University, Shanghai, China

[3] Lawrence Berkeley National Laboratory, Berkeley, USA

Their goal was to create a low-cost, high-performance TDC that could match the demands of the next generation sub-10ps TOF- PET camera. They provided a new way for constructing TDCs on FPGA termed Pico-TDC method in the study. The Pico-TDC approach is unique in that it uses single FPGA registers as low-precision TDCs and then combines many of those low-precision TDCs to create a high-precision TDC. This research was looked at to see what other measures may be taken to improve the TDC's performance. [2]

C. 264 Channel TDC Platform Applying 65 Channel High Precision (7.2 psRMS) FPGA Based TDCs

Authors: Cahit Ugur[1], Grzegorz Korcyl[2], Jan Michel[3], Manuel Penschuk[3] and Michael Traxler[1]

[1] GSI Helmholtz Centre for Heavy Ion Research, Darmstadt, Germany

[2] Jagiellonian University, Krakow, Poland

[3] Goethe-University, Frankfurt, Germany

The architecture of a 65-channel TDC built on a single FPGA is thoroughly addressed in this work, as well as test results illustrating some of the quality measurements. For time measurements, the TDC uses the interpolation approach, and for precision, it employs the Wave Union Launcher method. On all channels, the TDC has a maximum precision of 7.2 ps RMS and a $<$ 14 ps RMS. To get around the minimum pulse width restriction, a semi-asynchronous pulse stretcher is used, which has been confirmed to allow for a pulse width measurement of $<$500 ps. This work describes the Semi-asynchronous stretcher, which was effective for limiting the minimum pulse width. [3]

D. A Multichannel High-Resolution (less than 5 ps RMS between two channels) Time-to-Digital Converter (TDC) Implemented in a Field Programmable Gate Array (FPGA)

Authors: Eugen Bayer[1], Peter Zipf [1] and Michael Traxler[2] [1] University of Kassel, Germany[2] GSI Helmholtz Centre for Heavy Ion Research, Darmstadt, Germany

This study provides a new concept for time interpolation that uses dedicated carry-chains and can do two time measurements in a single carry-chain per hit. Multiple ($>$2) measurements can be done in a single chain per hit, resulting in a temporal resolution of $approx2$ ps RMS between two channels in this architecture. This work was examined in order to examine some advanced interpolation approaches for the tapped delay line method in greater depth. These strategies are used to improve a TDC channel's single channel resolution using

the TDL method. An incoming start signal begins numerous interpolations in all procedures, resulting in N measurements that are averaged and recorded. [4]

E. Time-to-digital-converter based on multiple-tapped-delay-line

Authors: Dariusz Chaberski[1] [1] Nicolaus Copernicus University, Poland

The idea, operation, analysis, design, and test results of a time-to-digital converter (TDC) based on multiple-tapped-delay-lines are described in this article (MTDL). Multiple TDLs with low equivalent resolution (323 ps on average) were used to achieve a measurement equivalent resolution of approximately 5:8 ps. For each hit, the aim of measurement is to combine all tapped-delay-line results into a single high-precision time-stamp. This study included a detailed mathematical analysis that was required to complete this process. [5]

F. A Coarse-Fine Time-to-Digital Converter

Authors: Ya-Qian Chen[1], Li-Ya Meng[1] and Xiao-Gang Lin[1] [1] Key Laboratory of Optoelectronic Technology and System, P.R. China

A high-precision TDC based on a three-level conversion technique is proposed in this study. A TDC with excellent resolution and a large dynamic range is required as integrated circuit technology advances. It's not enough to meet just one goal. The Coarse-Fine TDC suggested in this study contained three steps, similar to the nutt interpolation method, in terms of precision and dynamic range. This study was researched in order to gain a better understanding of these three stages. [6]

G. New Design-methodology of High-performance TDC on a Low Cost FPGA Targets

Authors: Foudil Dadouche, Timothé Turko, Wilfried Uhring, Imane Malass, Norbert Dumas, Jean-Pierre Le Normand

This project seeks to propose a Time-to-Digital Converter (TDC) design technique for low-cost Field-Programmable Gate Array (FPGA) targets. To begin, the paper shows how to take use of the presence of carry chains in the FPGA's elementary logic parts to improve TDC resolution. After that, it explains how to use the Chip Planner tool to place the system's partitions in user-defined physical zones. This allows TDC divisions to be placed in such a way that routing pathways are restricted. As a result, the user has effective control over the propagation delay over the connection network.The paper concludes with a case study demonstrating the design and construction of a high resolution TDC dedicated to a time correlated single photon counting system using the technique described. The INL, DNL, and mean Jitter values (22 ps rms, 13 ps rms, and 26 ps rms, respectively) found utilising a low-cost FPGA target Cyclone family are all highly promising and suited for a wide range of rapid applications. [7]

H. Low-Cost FPGA TDC With High Resolution and Density

Authors: Jiajun Zheng, Ping Cao, Di Jiang, Qi An

For years, time-to-digital converters (TDCs) in field programmable gate arrays (FPGAs) have been developed and have achieved exceptional performance. If TDC is implemented in an FPGA, a tradeoff between performance and cost must be addressed in an application with a large number of channels. Massive channels with a high event rate present significant obstacles for real-time transmission of huge data rates. As a result, developing time digitizers that can handle a high data rate while maintaining a satisfactory resolution and cost is critical. A TDC prototype with sandwich structure developed in a low-cost FPGA is shown in this research. It has 320 time measurement channels (ten TDC daughter cards) and can be used as a digitizer in compressed baryonic matter time-of-flight experiments to evaluate super module detectors. [8]

I. A fully fledged TDC implemented in field-programmable-gate-arrays

Authors: Jinhong Wang, Shubin Liu, Qi Shen, Hao Li, Qi An

The goal of this work is to construct a fully functional FPGA-based TDC in XILINX XC4VFX60 FPGAs with self-testing, temperature variation correction, and trigger-matching capabilities. Self-testing is done using statistical methods, and the resolution of the delay chain is determined at its temperature and supplied voltage. The resolution varies with the temperature of the environment, thus a self-test from 30 to 60 degrees Celsius was used to compensate. The RMS of time measurement after compensation and INL calibration is less than 30 ps per channel of the total six, with a resolution of roughly 50 ps. Trigger-matching is done with content addressable memory and two programmable parameters: trigger-latency and matching window. [9]

J. Several Key Issues on Implementing Delay Line Based TDCs Using FPGAs

Authors: Jinyuan Wu (Fenni National Accelerator Laboratory, Batavia, IL, USA)

This work covers the development of the Wave Union TDC, a revolutionary FPGA TDC scheme that uses multiple measurements to improve time measurement precision, as well as various other subjects in FPGA delay line based TDCs. First, FPGA-specific concerns such as delay line selection in different FPGA generations and encoding logic are studied. Following that, common concerns for both FPGA and ASIC TDCs are explored, including coarse time counter implementation techniques, bin-by-bin calibration, and noise issues caused by single ended signals. The document describes several resource/power-saving design methods for various processing phases. [10]

III. Proposed System

A. Problem statement

Using a Field Programmable Gate Array (FPGA) device, create a multi-channel time-to-digital converter (TDC). With

the TDC as planned, we will be able to measure time delays between any two signals (start and stop) with sub-nanosecond accuracy. For data transfer, the TDC needs be connected to a UART module.

B. Scope

The goal of our project is to create a ”Multi-channel Time to Digital Converter (TDC) integrated with UART communication.” As a result, our project’s scope is limited to the development of coarse and fine counters, as well as their integration with UART communication. The Coarse Counter will be used to measure longer time intervals (steps of 10 nanoseconds), while the Fine Counter will be used to monitor shorter time intervals (steps of 476 picoseconds). This technology can be employed anywhere precision timing measurement and massive data transmission are required.

C. Experimental Setup

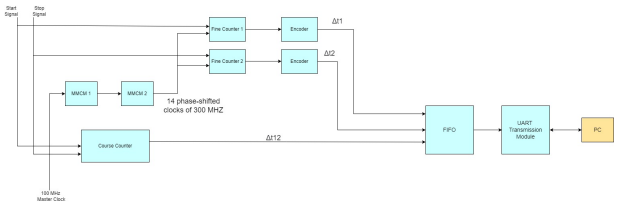

Fig. 1. Block Diagram

The start and stop pulses are sent from the observatory to the FPGA. Start and clock pulse are fed into fine counter module 1, while stop and clock pulse are fed into fine counter module 2. The time intervals $\Delta t1$ and $\Delta t2$ are output by the fine counter. This is the number of picoseconds between the start and stop pulse edges and the next positive edge of the clock. The coarse counter module receives the start, stop, and clock pulses as inputs. This returns the Δtc time interval, which is the period of 10 nanoseconds between start and stop pulses. This final output is transmitted to the User/PC by using the UART module. The final count is calculated as follows :

$\Delta T = \Delta tc + \Delta t1 - \Delta t2$

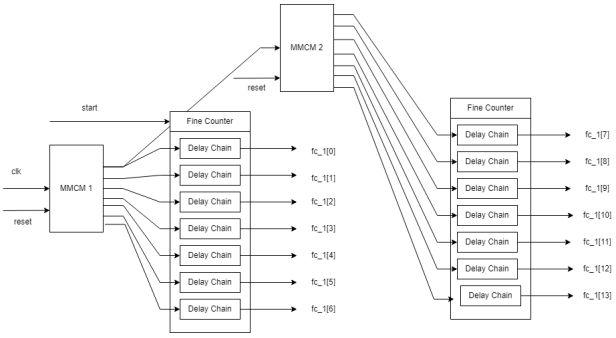

Fig. 2. MMCM Module

MMCM generates multiple clocks with defined phase and frequency relationships to a given input clock. It accepts up to two input clocks and up to seven output clocks per clock network. So therefore, we have included two MMCM to get 14 phase shifted clocks.

	Output Clock	Frequency (MHz)	Phase (Degree)	Duty Cycle (%)
MMCM 1	clk_out1	300.000	0.000	50.000
	clk_out2	300.000	25.000	50.000
	clk_out3	300.000	50.000	50.000
	clk_out4	300.000	75.000	50.000
	clk_out5	300.000	100.000	50.000
	clk_out6	300.000	125.000	50.000
	clk_out7	300.000	150.000	50.000
MMCM 2	clk_out8	300.000	175.000	50.000
	clk_out9	300.000	200.000	50.000
	clk_out10	300.000	225.000	50.000
	clk_out11	300.000	250.000	50.000
	clk_out12	300.000	275.000	50.000
	clk_out13	300.000	300.000	50.000
	clk_out14	300.000	325.000	50.000

Fig. 3. Output clock of 2 MMCM

In this system, the fine counter is implemented with the help of two Mixed-Mode Clock Manager (MMCM) module of the FPGA. The clock of 100 MHz is given as input to first MMCM which gives seven equally phase shifted 300 MHz clocks as output.Then the first output clock (clkout1) of first MMCM is given input to the second MMCM which in-turn generates 7 output clocks of 300 MHz. So total of 14, 300MHz clocks are generated using 2 MMCM modules.These fourteen phase shifted 300 MHz clock latch the start and stop signal to 14 bit thermometer code. The 14 bit value obtained from this is used to calculate the fine measurement. Figure 3 shows the clocks generated by the MMCM module for use in the fine counter. Since the time period of the 300 MHz clock is 3333.33 ps, the resolution of the fine counter is 3333.33 ps ÷ 14 = 238.09 ps.

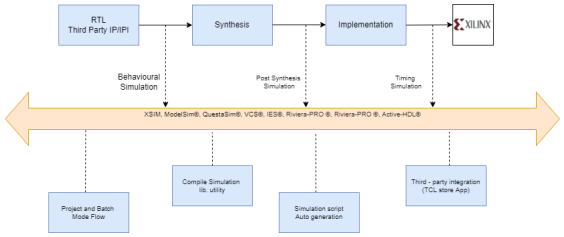

Fig. 4. Simulation Flow

D. Proposed System

Our proposed system is a hybrid counter that measures time using the Nutt interpolation approach. An FPGA board will be used to create the circuit (Nexys A7 FPGA). Finally, the UART protocol will be used to communicate in this system.

The nutt interpolation method is used to create the hybrid counter. The key benefit is that it can use the coarse counter to measure long ranges and the fine counter to achieve resolution finer than the clock cycle period.

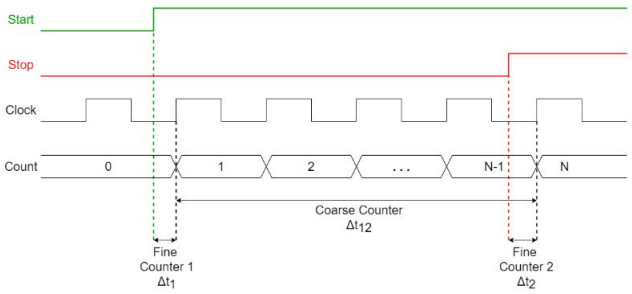

Fig. 5. Timing Diagram

The time interval T to be measured is divided into three intervals as shown in Figure 5. One interval t12 (which may be quite long) is measured in real time by the coarse counter; the remaining two short intervals, Δt1 and Δt2 (at the beginning and at the end of the interval T), are measured by a high resolution TDC, that is, the fine counter. The fine counter measures the time between the positive edge of the STOP/START pulse and the next positive edge of the clock.

1) Course Counter: The coarse measurement in this project was done with a 100 MHz clock. As a result, the coarse counter measures time in 10ns increments. Because the fine counter cannot measure lengthy timing intervals, this is a key component. The coarse counter is a simple counter that counts the FPGA clock to measure time intervals.

2) Fine Counter: The fine counter is used to calculate time intervals in the picosecond range. Because the internal clock frequency of the FPGA is 100 MHz, direct counting at a picosecond interval is impossible. The fine counter is

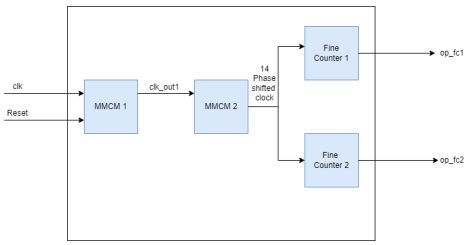

Fig. 6. Fine Counter

implemented in this system using the FPGA's Mixed-Mode Clock Manager (MMCM) module. A clock of 100 MHz is fed into the first MMCM, which outputs seven equally phase shifted 300 MHz clocks, and clk out1, the first output clock of MMCM 1, is fed into MMCM 2, which outputs seven equally phase shifted 300 MHz clocks. As a result, a total of fourteen 300MHz clocks with equivalent phase shifts are formed. The start and stop signals are latches to 14 bit thermometer code by these fourteen phase shifted 300 MHz clocks. The fine measurement is calculated using the 14 bit value acquired from this.

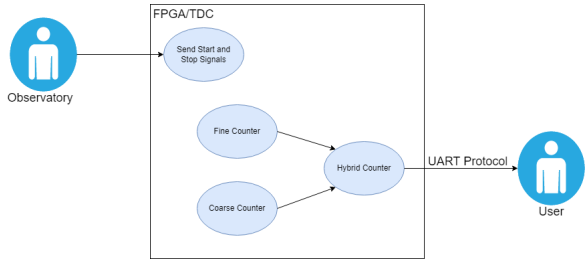

Fig. 7. Use Case Diagram

IV. Design

Diagram 5 Depicts how the system interacts with the external environment. In this diagram, there are two actors, the astronomical observatory and the user. The end user here may be another receiving end of the same observatory.The observatory detects the light rays using optical sensors and passes the start and stop pulses to the TDC system. The TDC system is fabricated on the FPGA and uses a hybrid counter which is a combination of the coarse and fine counter to measure and output the final time interval. This result is read by the end user.

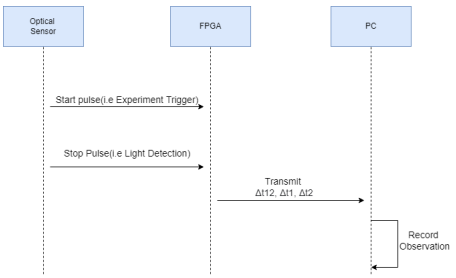

Fig. 8. Sequence Diagram

Diagram 8 shows the Sequence Diagram with object interactions arranged in time sequence. It is used represent the the sequence of messages exchanged between the objects needed to carry out the functionality of the scenario.The start of the experiment triggers the start pulse and the detection of light by the optical sensors creates the stop pulse. These two serve as input to the FPGA where the TDC counts the time interval between the two. The FPGA divides the time interval into 3 parts and generates 3 counts (Δtc, Δt1 and Δt2). The values are repeatedly generated and stored accordingly.

V. Results And Discussions

Here, figure 9 shows schematic diagram of the 14 bit counter and figure 10 shows the timing diagram of 14 bit counter. clk100 MHz is the master clock input provided, and the fc[13:0] is the fine counter total. clkout0 to clkout13 are the 14 phase shifted clocks of 300 MHz frequency.These phase shifted clock are provided through the MMMCM module of the Vivado Design Suite. We are using 2 MMCM to get an output of14 bit

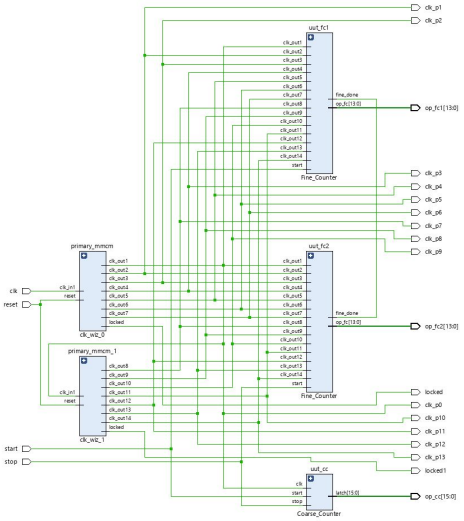

Fig. 9. Schematic Diagram of Hybrid Counter

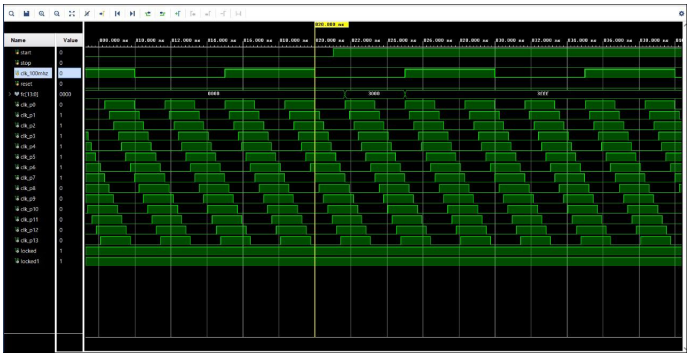

Fig. 10. Timing Diagram of Fine Counter

VI. Conclusion

The examination of various methodologies and equipment used to implement coarse counters, fine counters, and time-to-digital converters is described in this research. The benefits of TDCs based on FPGAs are underlined and described.

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