Implementaion of TDC using FPGA

Group No: 22

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Project Guides:

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Abstract

- This project deals with the design and implementation of a Multi-channel Time-to-Digital Converter (TDC) to measure time intervals with a picosecond level resolution.
- The hybrid counter designed for measuring the time interval uses a combination of a coarse counter and a fine counter technique .
- The coarse counter provides a longer measuring range whereas the fine counter provides the precision required in the concerned conditions. Thus, this design is efficient and reliable. Fpga is used to implement the above design.
- Using a HDL, FPGAs can be designed to meet the needs of the developer. This is beneficial to the project since it provides: high parallel processing capabilities, high reconfiguration, flexibility less development time.
- The embedded system developed for this research is planned to be integrated with the TIFR's GRAPES-3 experiment. As a result, it's built to handle enormous amounts of data efficiently during communication and processing. Finally, the suggested FPGA-based TDC system is combined with a UART module to allow for smooth data transmission to and from the end user.

Introduction

Background

- The earth’s atmosphere is blasted on a daily basis by cosmic rays, and these deviate on colliding with neutrons in the atmosphere. This produces large air showers, which are a spray of particles.
- As a result, when the ray reaches ground level, the air spray created by a single ray covers a broad region. The detection and observation of these air showers is carried out using huge muon detectors installed at ground level.
- The study of cosmic rays in different regions of the Galaxy can be aided by the detection of diffuse Galactic gamma ray flux. The abundance and spectrum shape of relativistic particles in the Milky Way are encoded in the energy and angular distributions of photons.

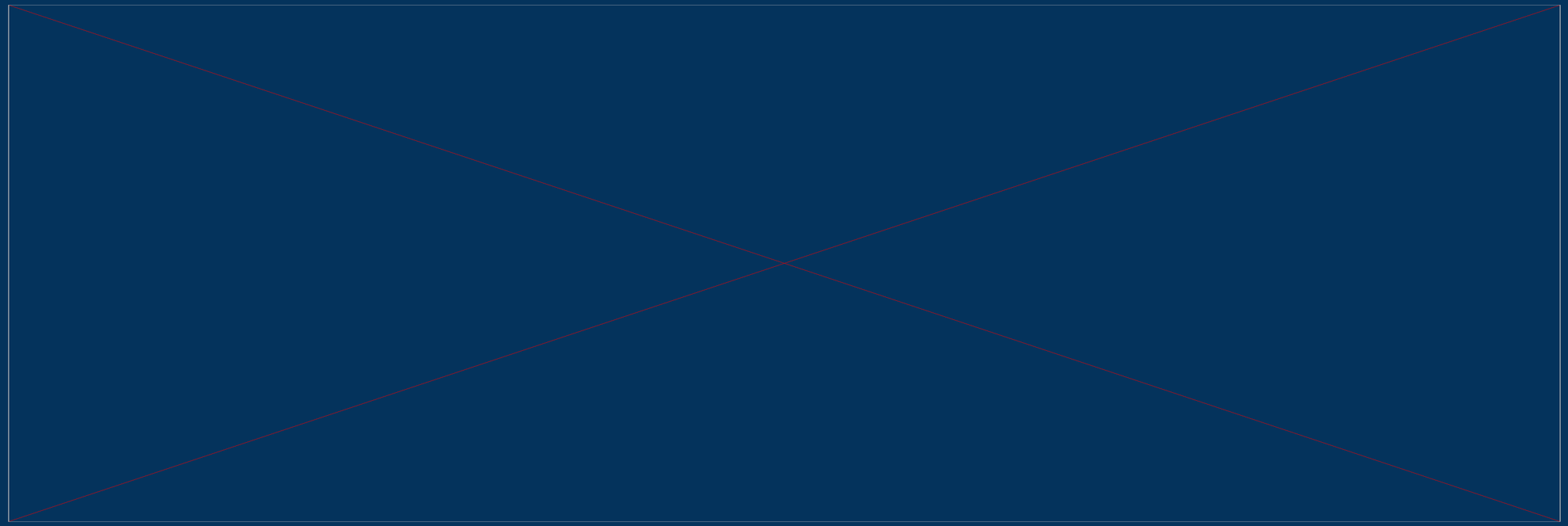
Introduction

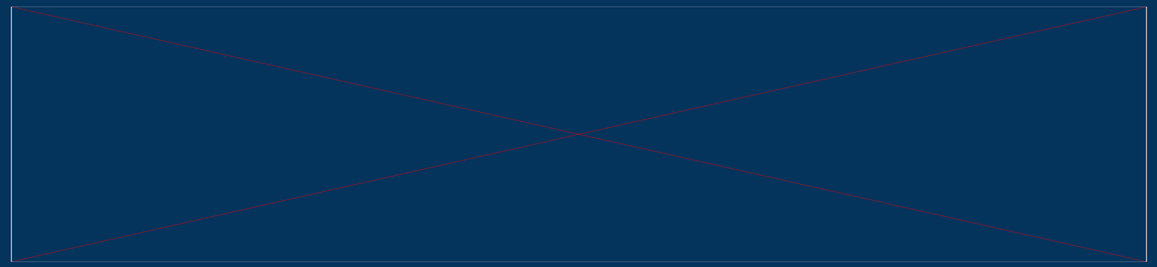
Background

The GRAPES-3 experiment in Ooty, India, began as a cooperation between Mumbai's Tata Institute of Fundamental Research and Osaka City University in Japan.

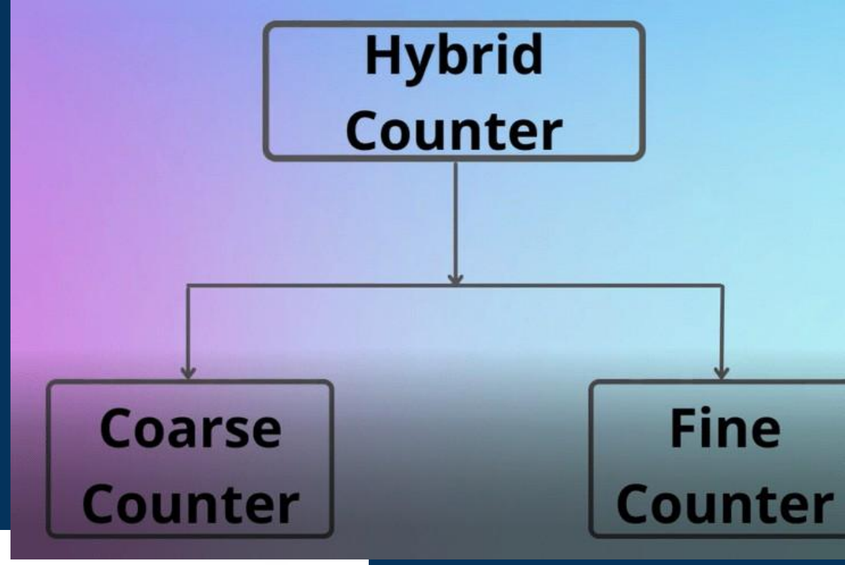
Introduction

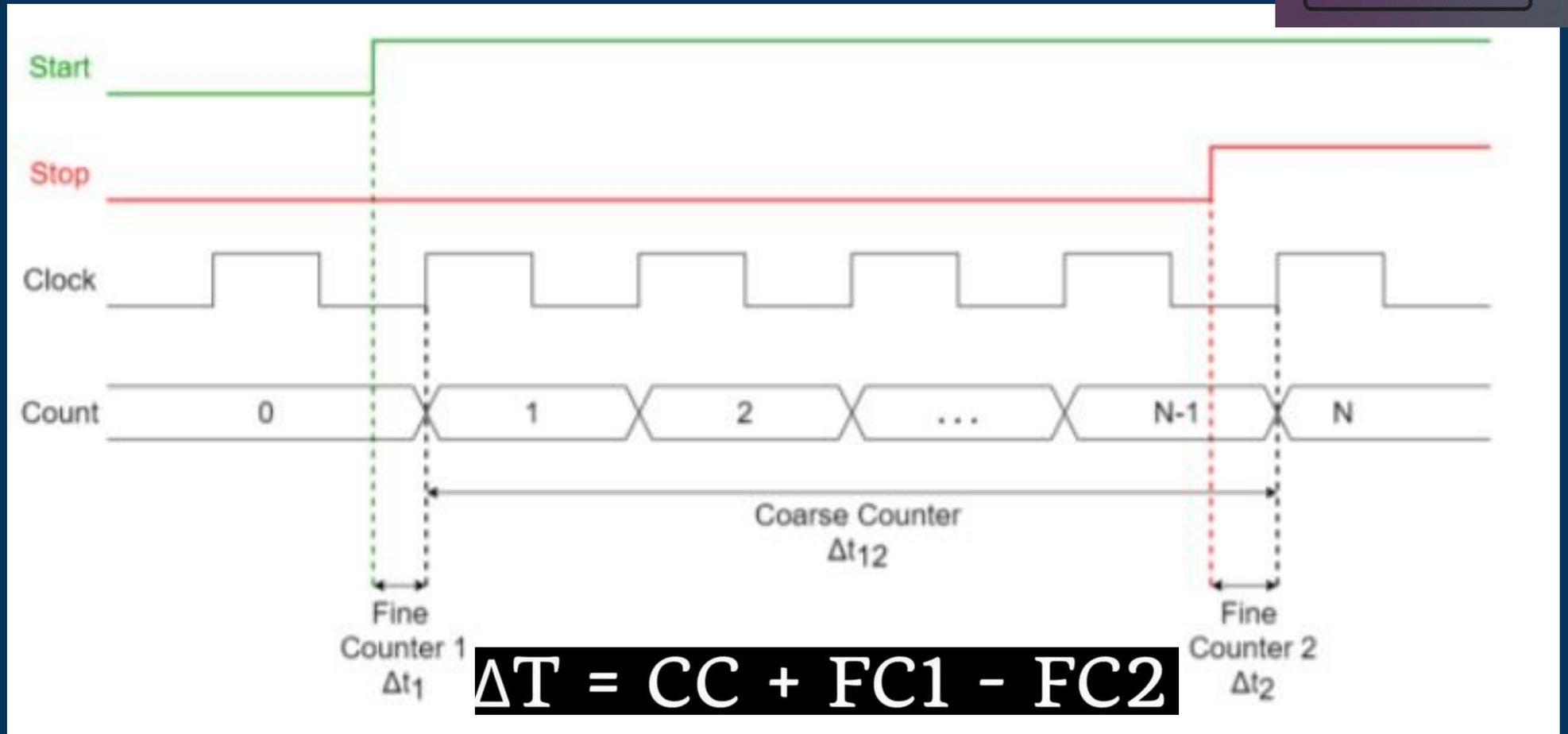
Background





TDC - Nutt Interpolation Method





$$\Delta T = CC + FC1 - FC2$$

PREVIOUSLY DONE

TDC using 6 phase shifted fine counter

- 60 degree phase shift 200
- MHz o/p frequency 833ps
- resolution

TDC using 12 phase shifted fine counter

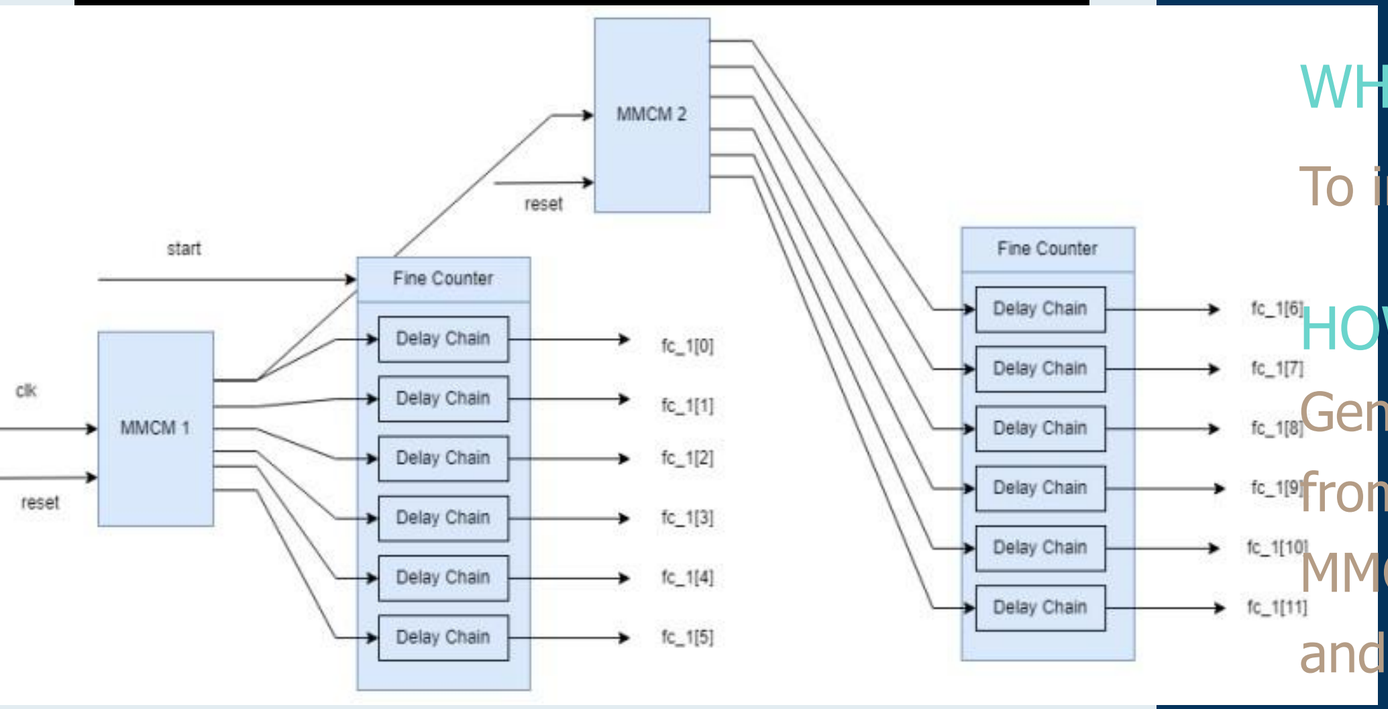
- 6, 60 degree phase shift
- 200 MHz o/p frequency
- 417ps resolution
- using posedge and neg edge of the clock

Phase shifted clock

THIS CLOCKS ARE CREATED USING INTERNAL MMCM MODULE.

MMCM

THE MMCM MODULE TAKES AN INPUT CLOCK NAMED CLKIN1 , AND GENERATES SEVERAL OUTPUT CLOCKS, EACH OF WHICH CAN BE CONFIGURED TO HAVE A DIFFERENT FREQUENCY THAT IS DEPENDENT ON THE INPUT CLOCK FREQUENCY.



Cascading MMCM

WHY CASCADING?

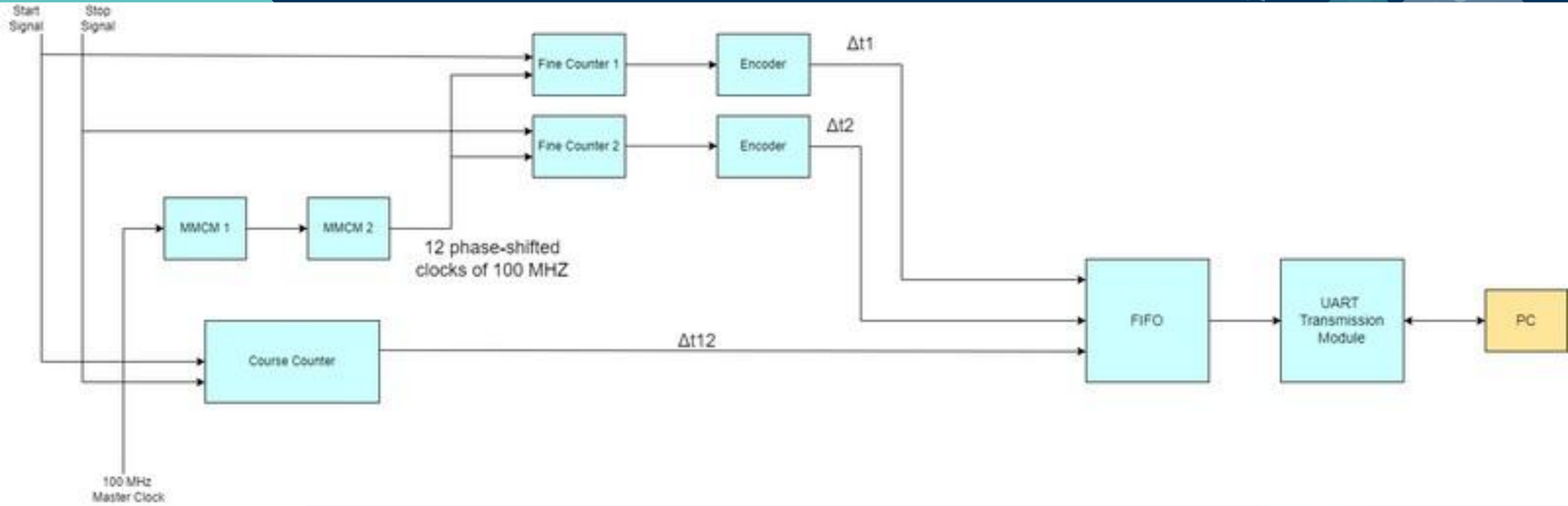
To improve the precision of TDC.

HOW?

Generate 6 op from first MMCM & next 6 from the second MMCM, the input for first MMCM is given as primary input(100MHz) and the for the second MMCM the input is given as one of the clock from the first MMCM

PHASE DIFFERENCE

We are generating 100 MHz clocks with 30° phase shift

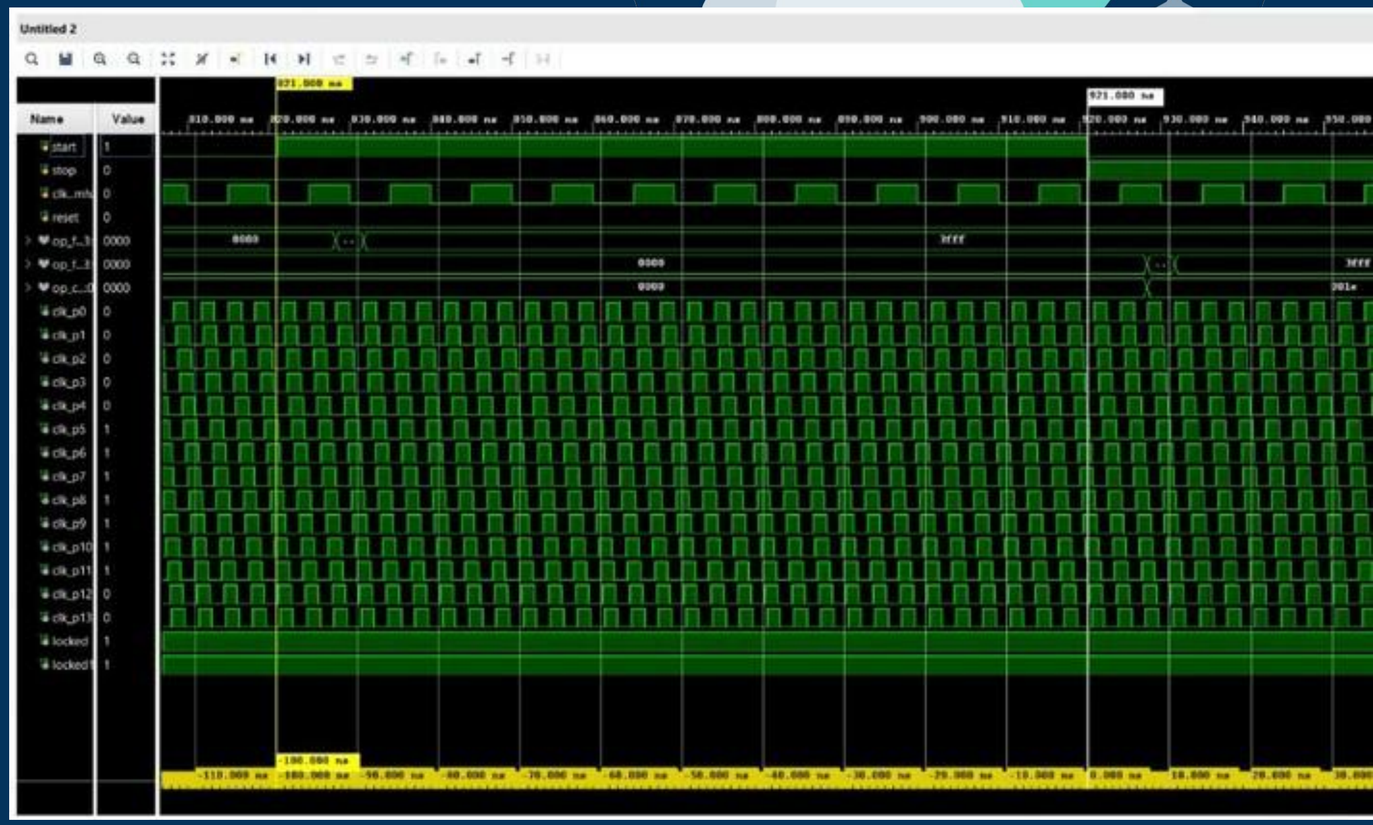


Block Diagram of TDC

14-PHASE SHIFT

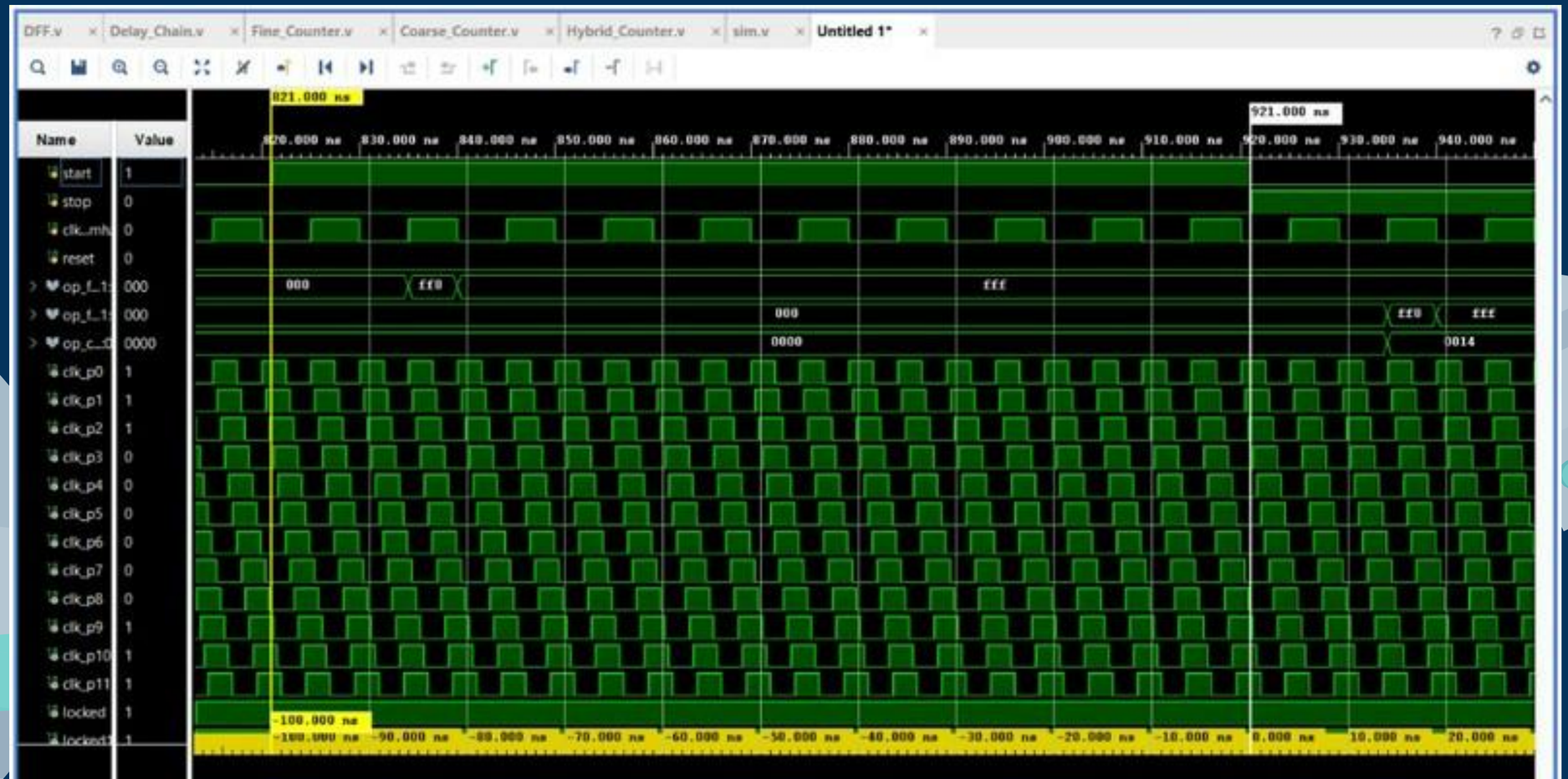
At first we tried to do the 14 phase TDC, but we counldn't get through the timing error

We had cascaded two MMCM with phase difference of 25°, with 300MHz frequency.



12-bit phase shift

WE THEN IMPLEMENTED 12 - BIT PHASE SHIFT SIMULTANEOUSLY, WITH 30° PHASE SHIFT.

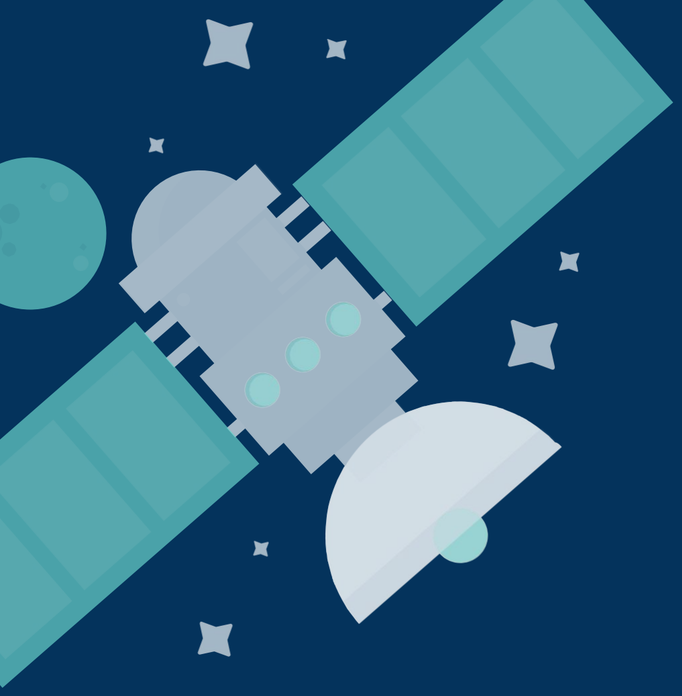


Go About

12 bit output of 200 MHz

Used 2 delays in the delay chain and a latch all the 12 bit outputs at first clock output

Expected timing error has occured



RECTIFICATION

FIRST

changed the output clock frequency to 150 MHz

SECOND

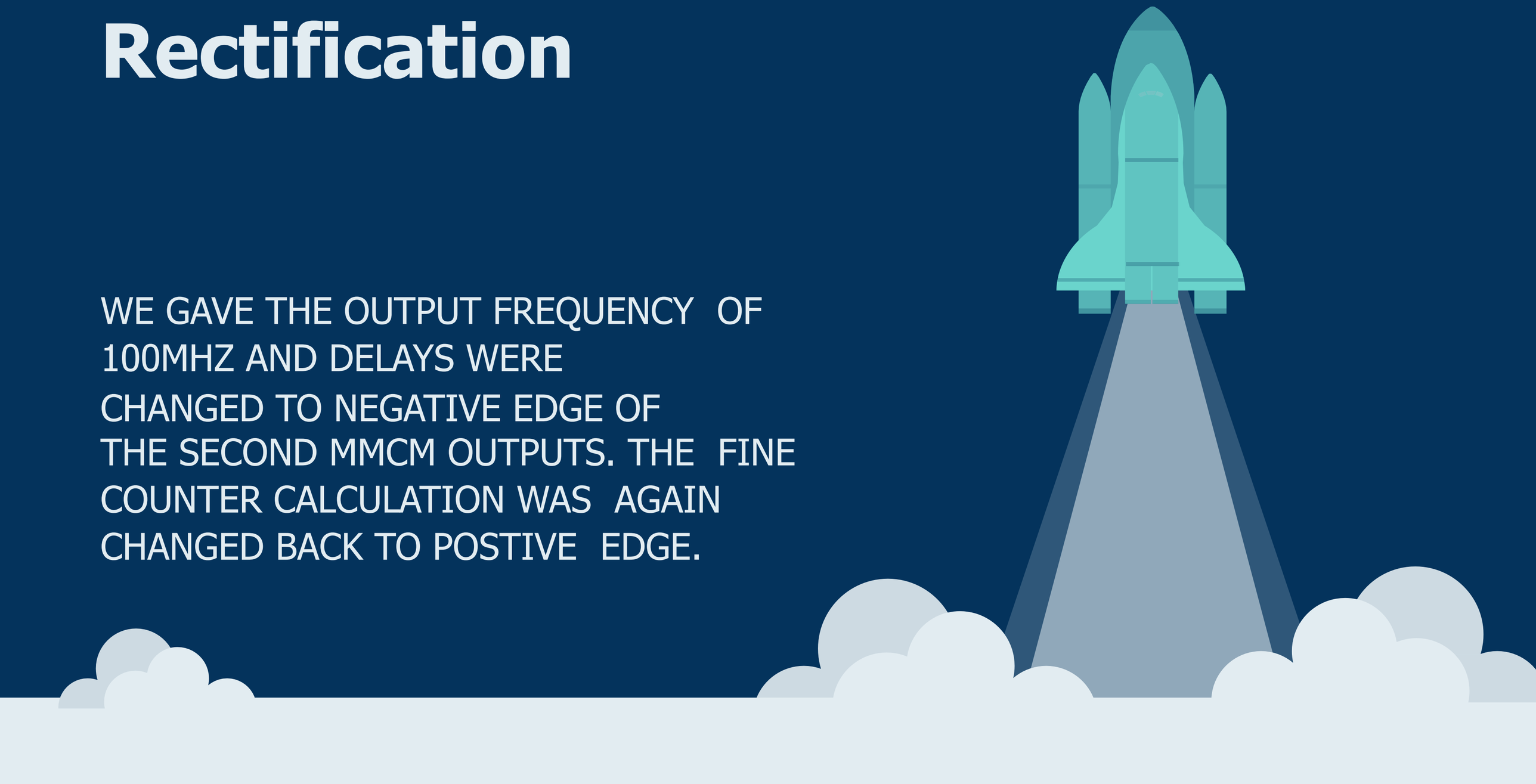
changed the delays from positive edge to negative edge

THIRD

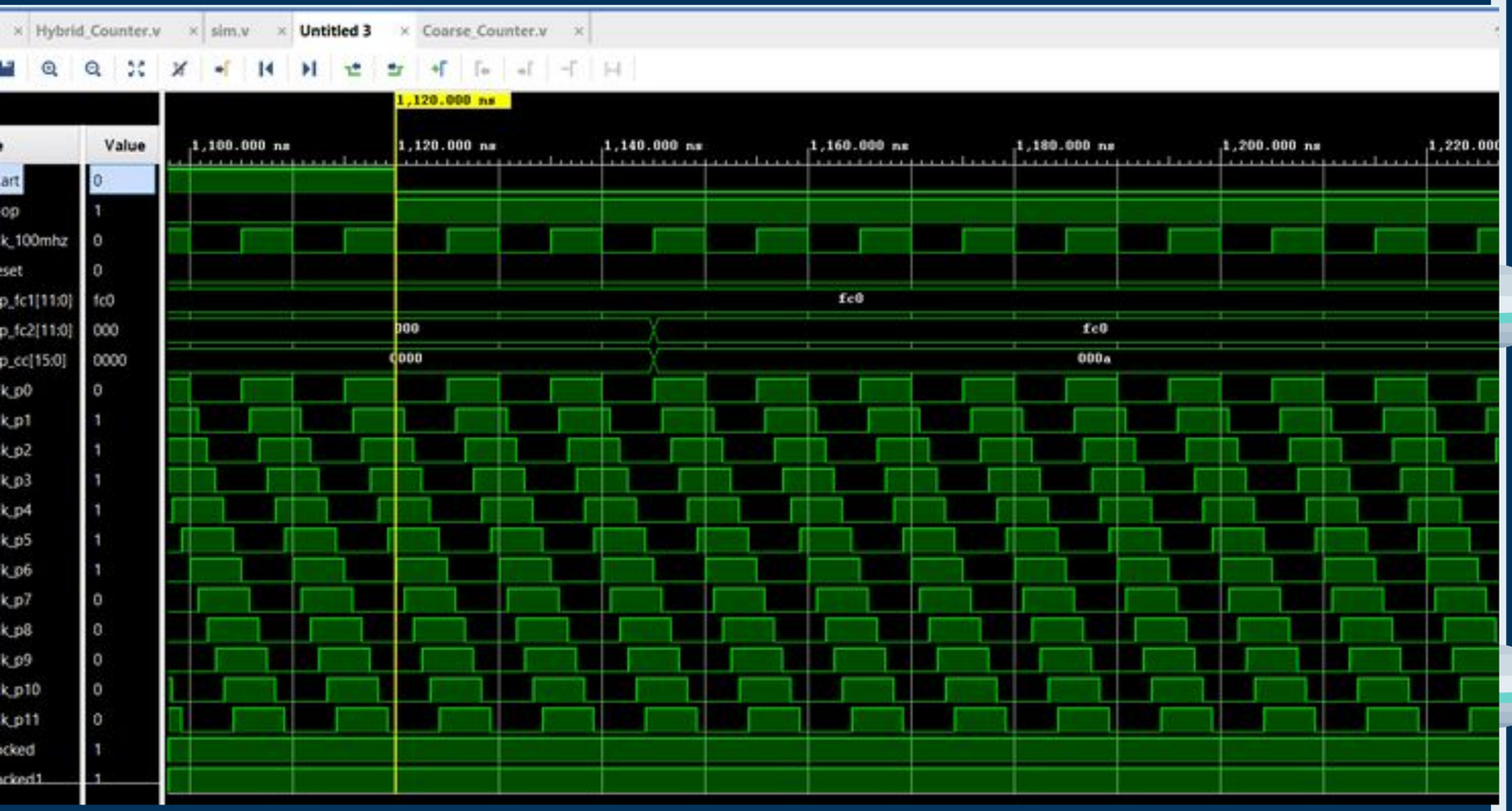
changed the fine counter calculation from positive edge to negative edge

Rectification

WE GAVE THE OUTPUT FREQUENCY OF 100MHZ AND DELAYS WERE CHANGED TO NEGATIVE EDGE OF THE SECOND MMCM OUTPUTS. THE FINE COUNTER CALCULATION WAS AGAIN CHANGED BACK TO POSTIVE EDGE.



Simulation Flow



The input clock is 100 MHz

START / STOP

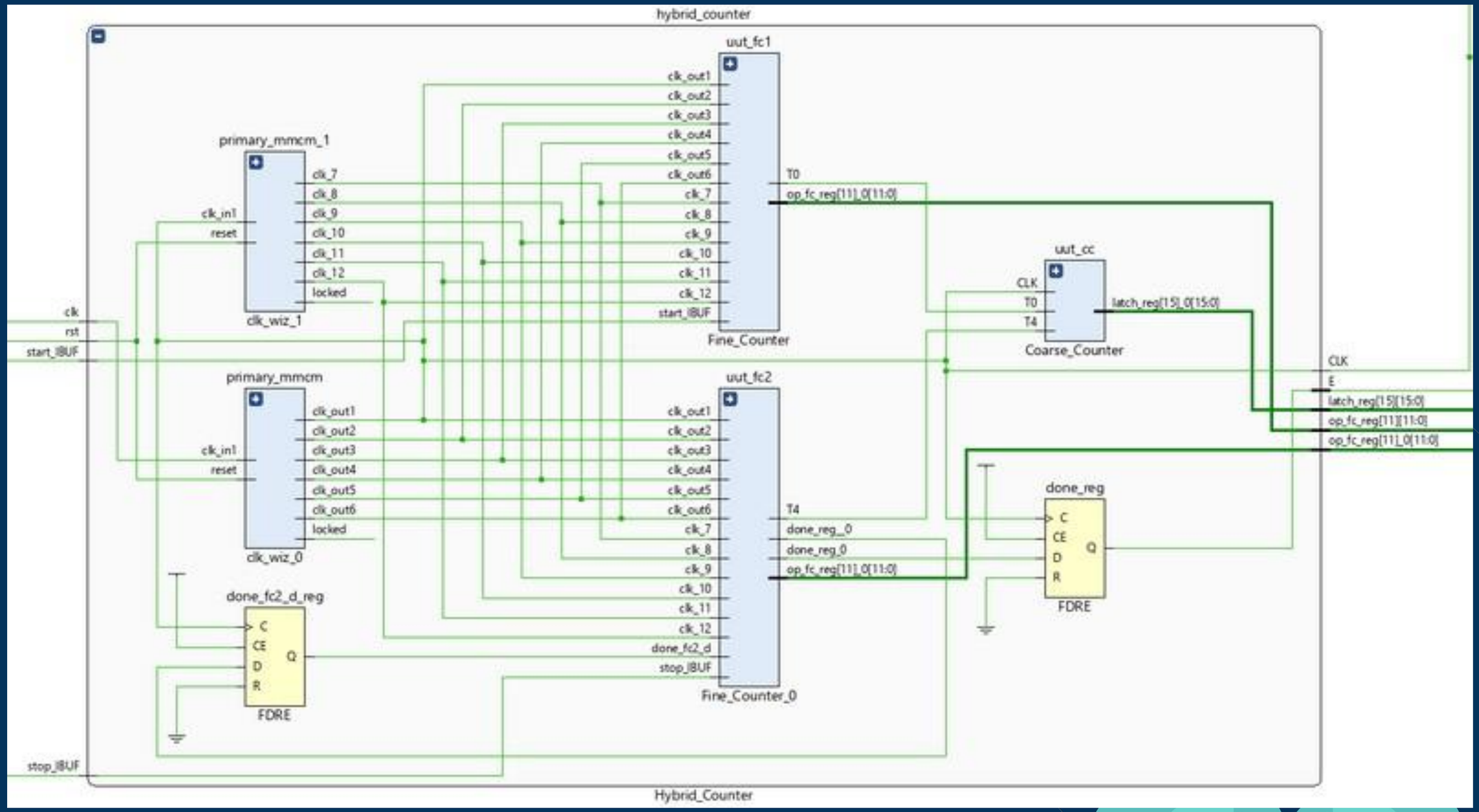
Start signal is given at 1020ns and stop is at 1120ns

FINE COUNTER

There are two fine counters with fc0 as output.

COARSE COUNTER

The coarse counter values are latched and we get the output after the stop signal goes high. The output is 000a


hybrid_counter
uut_fc1
clk_out1
clk_out2
clk_out3
clk_out4
clk_out5
clk_out6
clk_7
clk_8
clk_9
clk_10
clk_11
clk_12
start_IBUF
T0
op_fc_reg[11]_0[11:0]
Fine_Counter
primary_mmcm_1
clk_in1
reset
clk_7
clk_8
clk_9
clk_10
clk_11
clk_12
locked
clk_wiz_1
uut_cc
CLK
T0
T4
latch_reg[15]_0[15:0]
Coarse_Counter
clk
rst
start_IBUF
CLK
E
latch_reg[15][15:0]
op_fc_reg[11][11:0]
op_fc_reg[11]_0[11:0]
primary_mmcm
clk_in1
reset
clk_out1
clk_out2
clk_out3
clk_out4
clk_out5
clk_out6
locked
clk_wiz_0
uut_fc2
clk_out1
clk_out2
clk_out3
clk_out4
clk_out5
clk_out6
clk_7
clk_8
clk_9
clk_10
clk_11
clk_12
done_fc2_d
stop_IBUF
T4
done_reg__0
done_reg_0
op_fc_reg[11]_0[11:0]
Fine_Counter_0
done_reg
C
CE
D
R
Q
FDRE
done_fc2_d_reg
C
CE
D
R
Q
FDRE
stop_IBUF
Hybrid_Counter

TESTING EQUIPMENT/REQUIREMENT

TEKTRONICS GENERATOR (AFG 3252 C)

Two analog channels (ch1 & ch2), ch1(3.3 V) generates start pulse and ch2(3.3 V) generates stop pulse.[FPGA works on 3.3 V]

FPGA(NEXY' S A7)

The 2 signals are connected to FPGA board on which bit and ltx files have been programmed

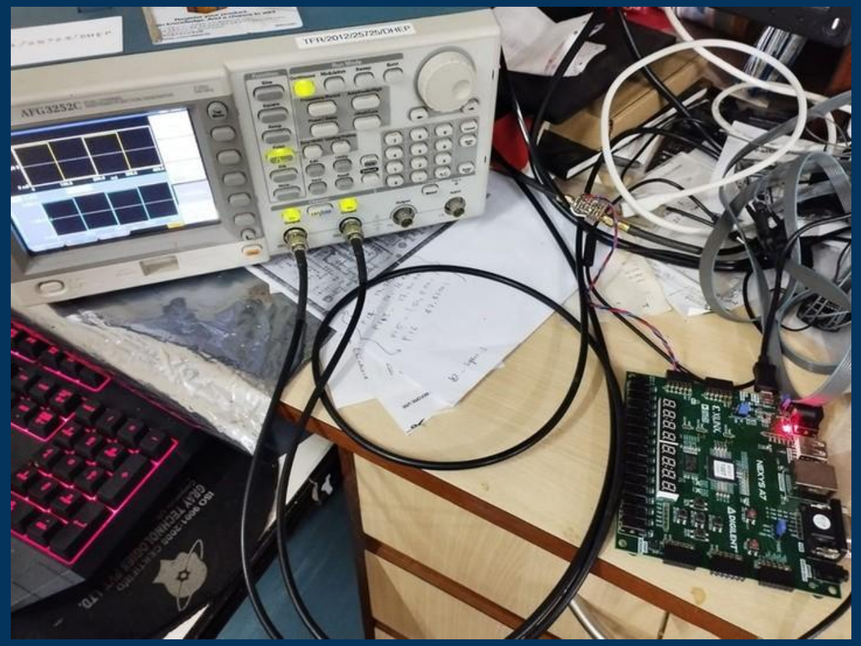
TIME DELAY

Time delays can between the start and stop can be changed digitally from 10ns to 10 ms on the function generator

DATA AQUISATION

Once FPGA files have been programmed TCL script has to be run to acquire data from FPGA via VIO and store it into a file.

Data Aquisation



EACH FILE CONTAINS 500 DATA READINGS OF AA(FIX BYTE), EVENT VALUE, COURSE COUNTER , AND FINE COUNTERS VALUE.

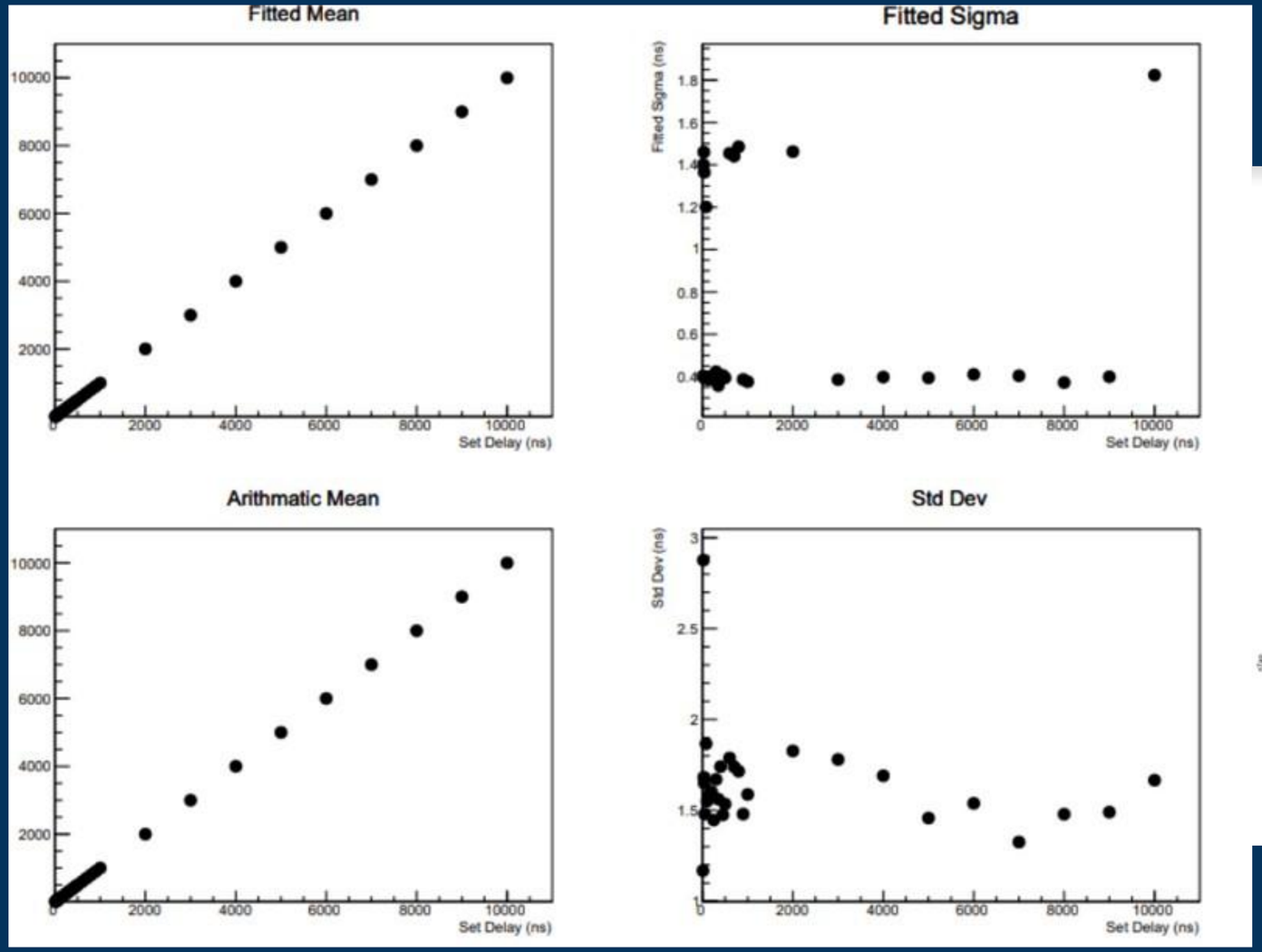
THESE FILES ARE GENERATED FOR EVERY DELAY. THE DATA IS ACQUIRED ON 2 HZ AND

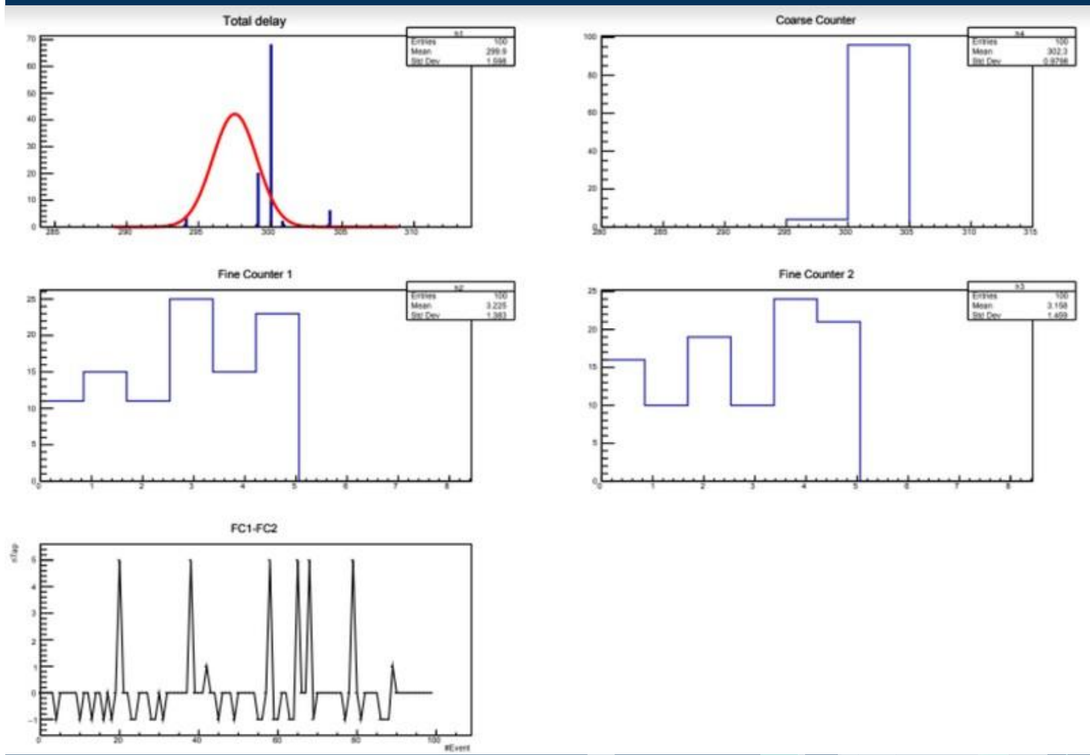
5 HZ.

These data files were analyzed through python script using pyROOT package of ROOT framework

Tests

6 phase shifted TDC

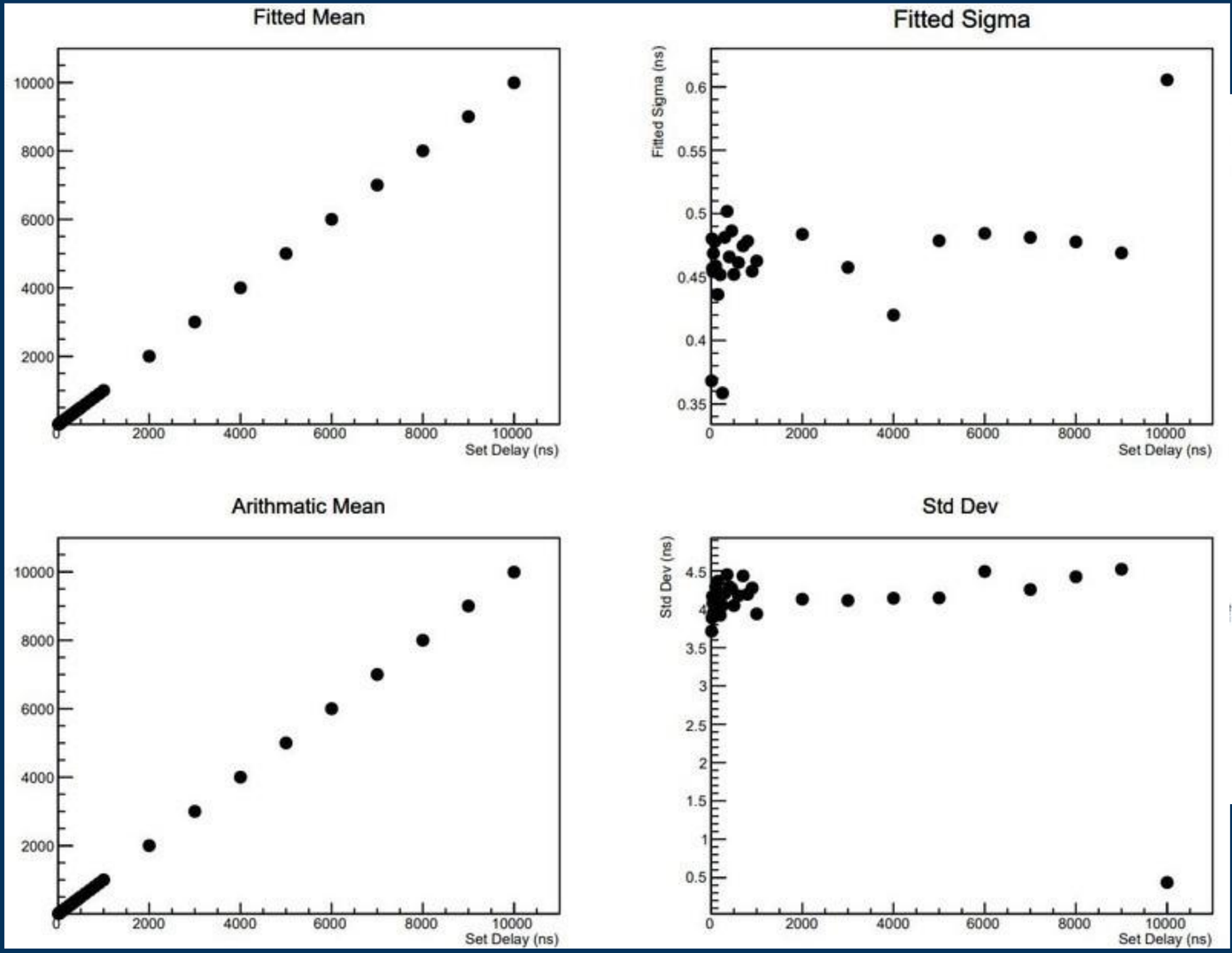


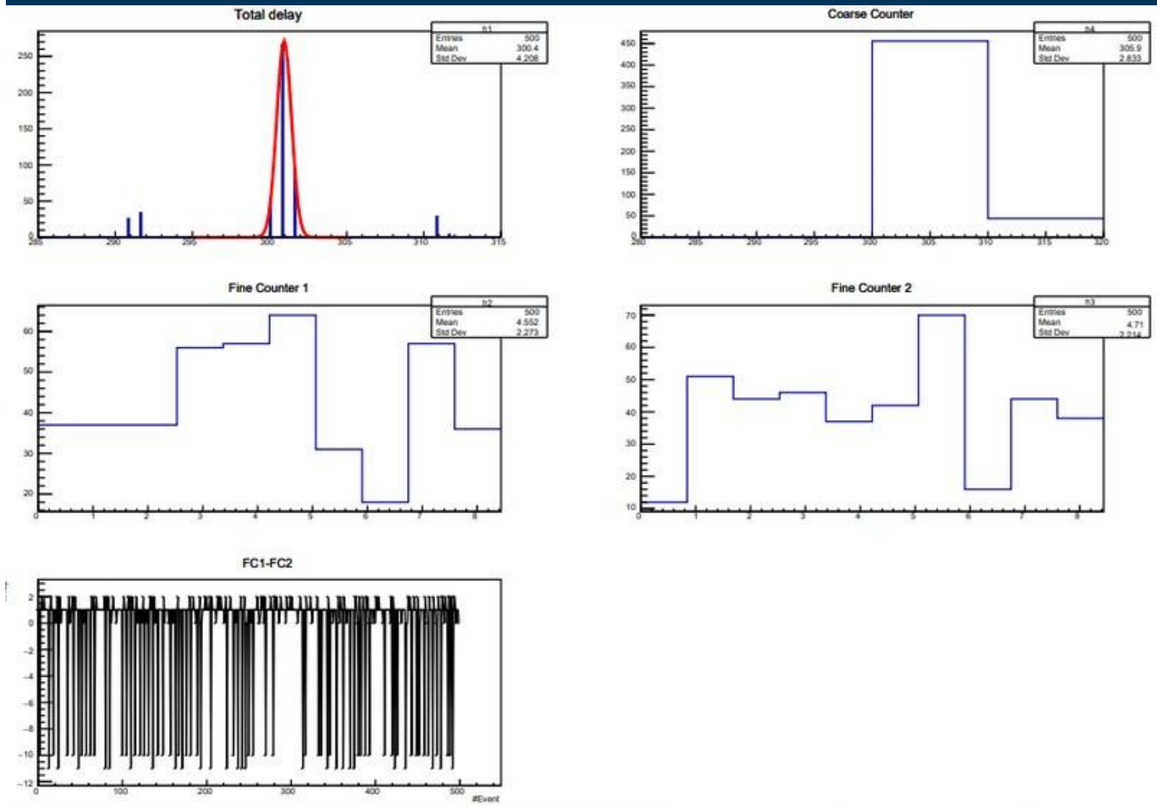


Eg. 300ns Delay

Tests

12 phase shifted TDC





Eg. 300 Delay

Conclusion

- Seniors followed with an approach of going ahead with one MMCM for 6ph clocks and achieved 833ps resolution with a reasonable **sigma fitting of (2.5ns to 3.5ns over the entire delay range of 10ns to 10microseconds).**
- The ultimate idea was to use multiple MMCMs and improvise upon both parameters(sigma variation and fitting). We took this challenge as a project for this year.
- The sigma fitting in our case was **0.4ns to 0.45ns (much much better with previous case)** over the entire range of 10ns to 10000ns. However the **standard deviation found was slightly higher (4ns-4.5ns) .**

Future Scope

Standard deviation which was high, requires investigation and can be improvised by suitably modifying constraints clock domains of data collection inside of FPGA.

We can still improve the 12-bit TDC by using manual placement.

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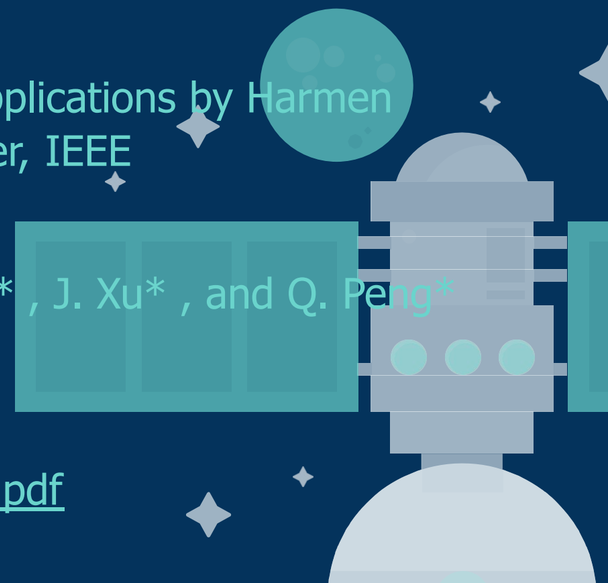


thank you