Assignment on Cache Memory

CO LAB: CS-201

May 14, 2018

The objective of this assignment is to design a Cache Simulator with the following characteristics:

- Cache Size: 1024, 2048, 4096, 8192, 16384 bytes
- Block size: 16 bytes
- Mapping Function:
  - Direct Mapped
  - 2-way set associative
- Replacement Policy:
  - LRU- Require updating the time-stamp of a block every time it is accessed.
  - FIFO- Require updating the time-stamp of a block when it is loaded into cache the first time.

The simulator should keep track of cache misses for each combination of size, associativity, and replacement policy. Considering a sequence of hexadecimal addresses, simulator executes a read from the cache to 1) check if it is contained in the cache. 2) If not, the number of misses are incremented and the cache is updated using the replacement policies. You are provided with a large file of address traces in order to test the scalability of your program.

• Requirements

- Simulator should be written in C/C++. Make sure that your program compile and run correctly. The simulator should output results in a table which contain the miss ratio for each combination of size and mapping function for each replacement policy. Output the tables in the following format:

LRU
FIFO LRU FIFO
Mapping/size 1024 2048 4096 . . . 1024 2048
Direct
2-Way

– Write a one page report summarizing the results for the provided test file. Explain the miss rates (why they are better for different configurations).
– Marks will be awarded based on the uniqueness of your implementation.
– Finally, find the size and mapping function of your laptops cache: L1-D, L1-I, L2 and L3 cache,
write the same in your report.