St. Francis Institute of Technology

Class: SE-ITA/ITB Semester: IV A.Y. 2023-2024

Subject: Microprocessor Programming Lab

Experiment – 2: Study of Logic Gates

1. **Aim:** To realize standard and universal logic gates:
   i. To verify the truth tables for basic and universal logic gates.
   ii. To design and implement half adder and full adder circuit.

2. **Prerequisite:** Basic working of logic gates.

3. **Requirements:**
   i. Breadboard, Power supply of 5V, connecting wires, LED, resistor
   ii. ICs – NAND-7400, NOT-7404, EXOR-7486, AND-7408, OR-7432, NOR-7402
   iii. Open source software tool: LogiSim

4. **Pre-Experiment Exercise:**

   A. Basic Gates

   a. AND Gate: An AND gate is a multiple input single output gate. For a 2-input AND gate as shown in Fig. 1(a) below, the output Q is true if both the inputs are true.

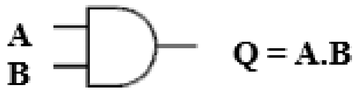

Fig.1(a). AND Gate

   b. OR Gate: An OR gate is a multiple input single output gate. For a 2-input OR gate as shown in Fig. 1(b) below, the output Q is true if any one or both the inputs are true.

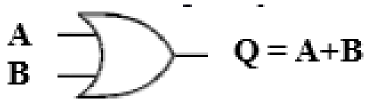

Fig. 1(b). OR Gate

   c. NOT Gate (Inverter): A NOT gate is a single input single output gate as shown in Fig. 1(c) below. The output Q is inverse of the input A.

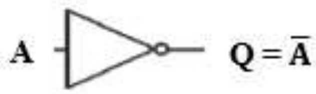

Fig.1(c). NOT Gate

   B. Universal Gates

   a. NAND Gate (NAND = Not AND): This is an AND gate with the output inverted. A NAND gate is a multiple input single output gate. For a 2-input NAND as shown in Fig. 2(a) below, the output Q is true if one or both the inputs are false.

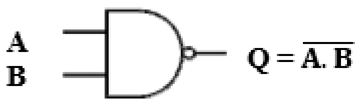

Fig. 2(a). NAND Gate

   b. NOR Gate (NOR = Not OR): This is an OR gate with the output inverted. A NOR gate is a multiple input single output gate. For a 2-input NOR gate as shown in Fig. 2(b) below, the output Q is true only if both the inputs are false. If any one of the input or both the inputs are true, the output Q is false.

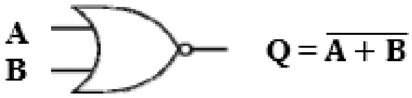

Fig. 2(b). NOR Gate

C. **Derived Logic Gates**

a. **EX-OR (Exclusive-OR) gate:** This is an OR gate but Excluding the case when both the inputs are true. An EX-OR gate is two input single output gate. For a 2-input EX-OR gate as shown in Fig. 3(a) below, the output Q is true when one of the inputs is true and the other is false i.e. the inputs are DIFFERENT. If both the inputs are false or true, then the output Q is false.

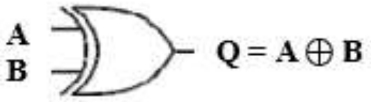

Fig. 3(a). EX-OR Gate

b. **EX-NOR (Exclusive-NOR) gate:** This is EX-OR gate with inverted output. An EX-NOR gate is two input single output gate. For a 20-input EX-NOR gate as shown in Fig. 3(b) below, the output Q is true when both the inputs are true or both are false i.e. both the inputs are SAME.

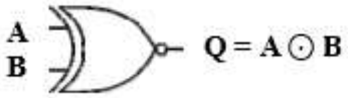

Fig. 3(b). EX-NOR Gate

D. **Adder Circuits**

a. **Half Adder:** There are two inputs and two outputs in a Half Adder. Inputs are named as A and B, and the outputs are named as Sum (S) and Carry (C). The sum is XOR of the input A and B. Carry is AND of the input A and B. With the help of half adder, one can design a circuit that can perform simple addition with the help of logic gates.

b. **Full Adder:** The full adder is a little more difficult to implement than a half adder. The main difference between a half adder and a full adder is that the full adder has three inputs and two outputs. The two inputs are A and B, and the third input is a carry input CIN. The output carry is designated as COUT, and the normal output is designated as S.

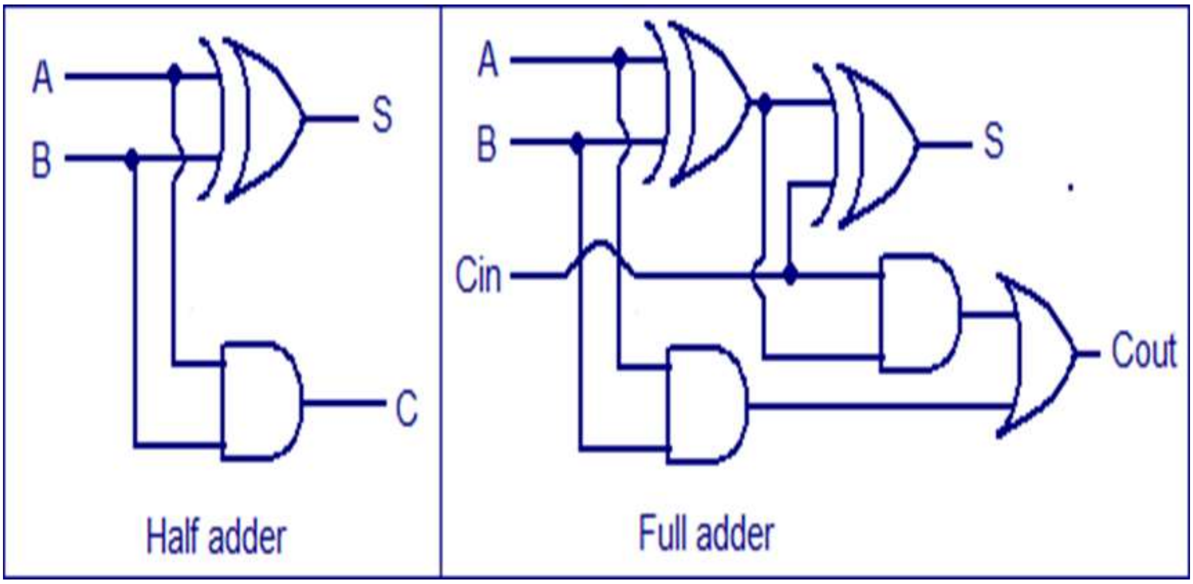

Fig. 4(a). Half Adder

Fig. 4(b). Full Adder

5. **Laboratory Exercise**

   A. Using Hardware

   a. Place the IC on the breadboard. Connect Positive and Negative terminal of Power supply to V_{CC} and GROUND of the IC.

   b. Use connectors for inputs and connect an LED via a resistor to the output of the IC.

   c. Apply various combinations of inputs according to the truth table and observe the output using LED.

   B. To design and implement half adder and full adder circuit.

   a. Place the gates on the canvas panel of LogiSim. Add the wires and connect it to the gates (input and output).

   b. Add the inputs. Save, Run and Observe the output.

6. **Post-Experiments Exercise:**

   A. Results/Calculations/Observations

   i. Draw the respective truth tables for all the logic gates and universal gates.

   ii. Draw the truth tables for half adder and full adder.

   B. Questions

   i. Why are NAND and NOR gates called as universal gates? Explain with an example for each.

   ii. Realize the following Boolean equation using gates: $Y = ABC + B\bar{C}D + \bar{A}BC$

   C. Conclusion

   Draw conclusion based on the experiment performed. Also mention few applications based on above experiment.

   D. References

   Mention two book references and two web references.

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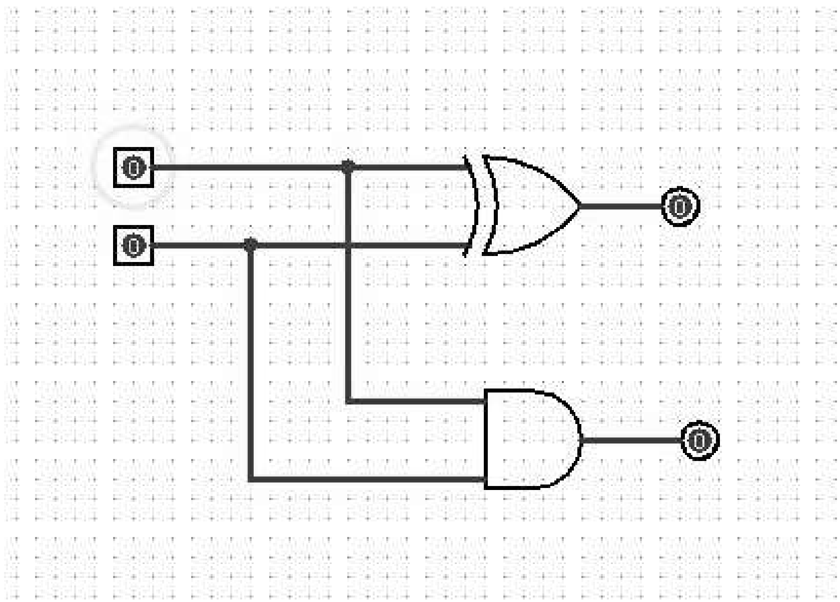
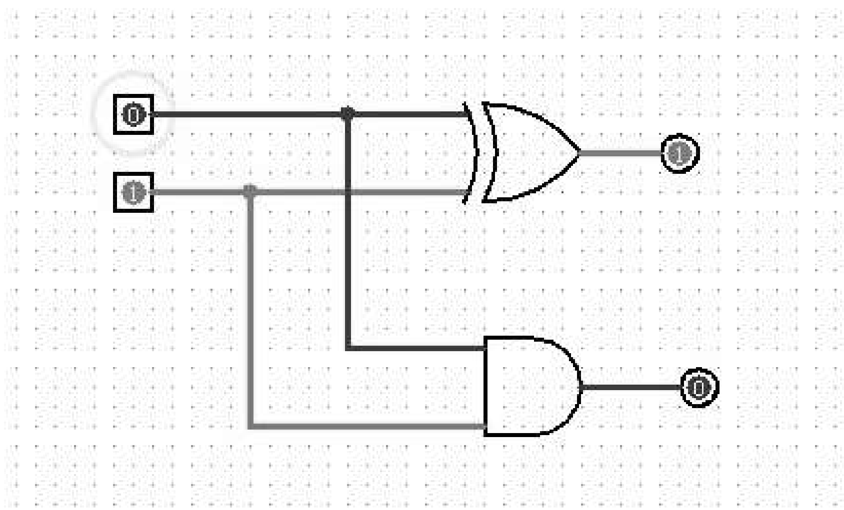
HALF- ADDER

Half Adder take 2 Input A and B and gives two output Sum(S) and Carry(C)

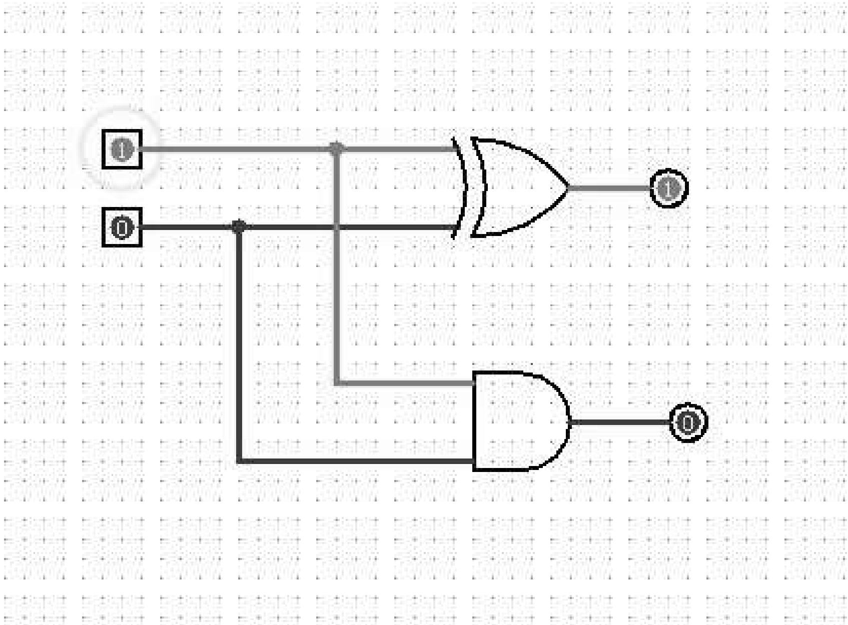
1.When A is 0 and B is 0, Sum(S) is 0 and Carry(C) is 0



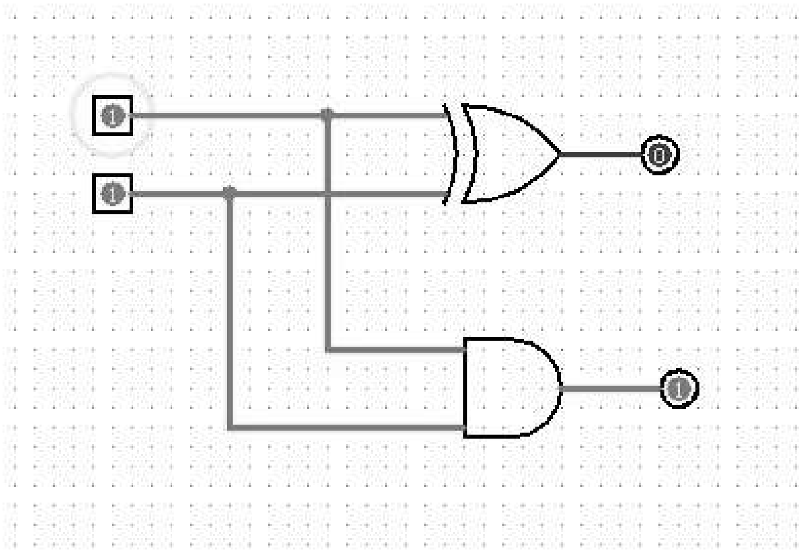
2.When A is 0 and B is 1, Sum(S) is 1 and Carry(C) is 0



3.When A is 1 and B is 0, Sum(S) is 1 and Carry(C) is 0

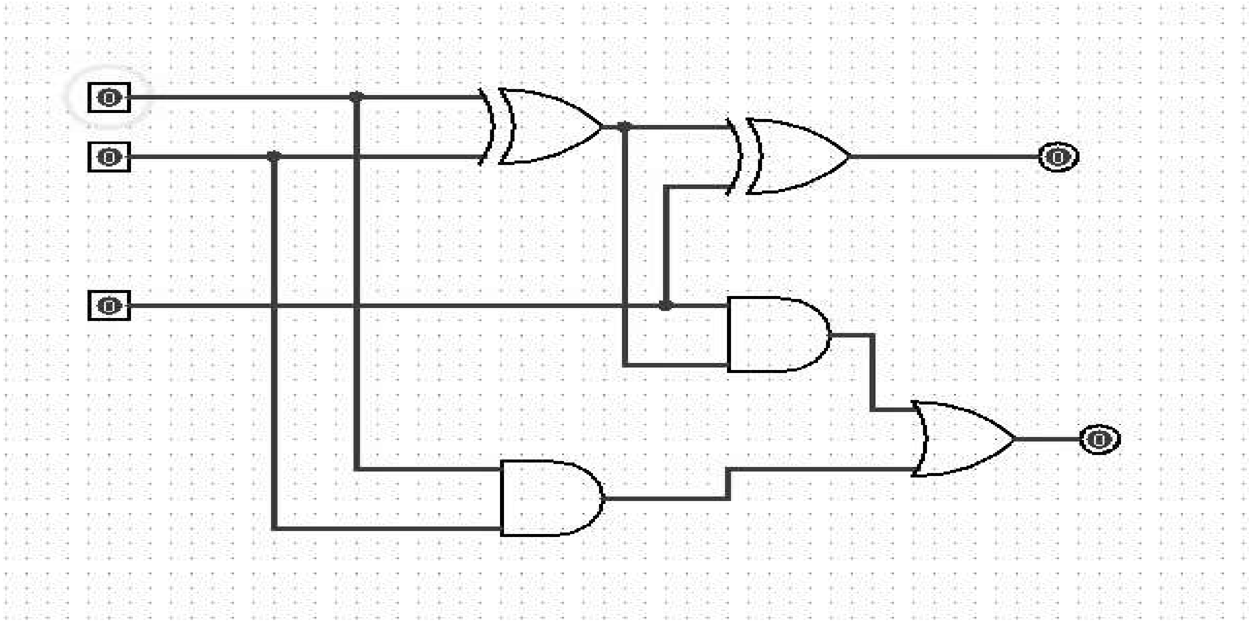


4.When A is 1 and B is 1, Sum(S) is 0 and Carry(C) is 1

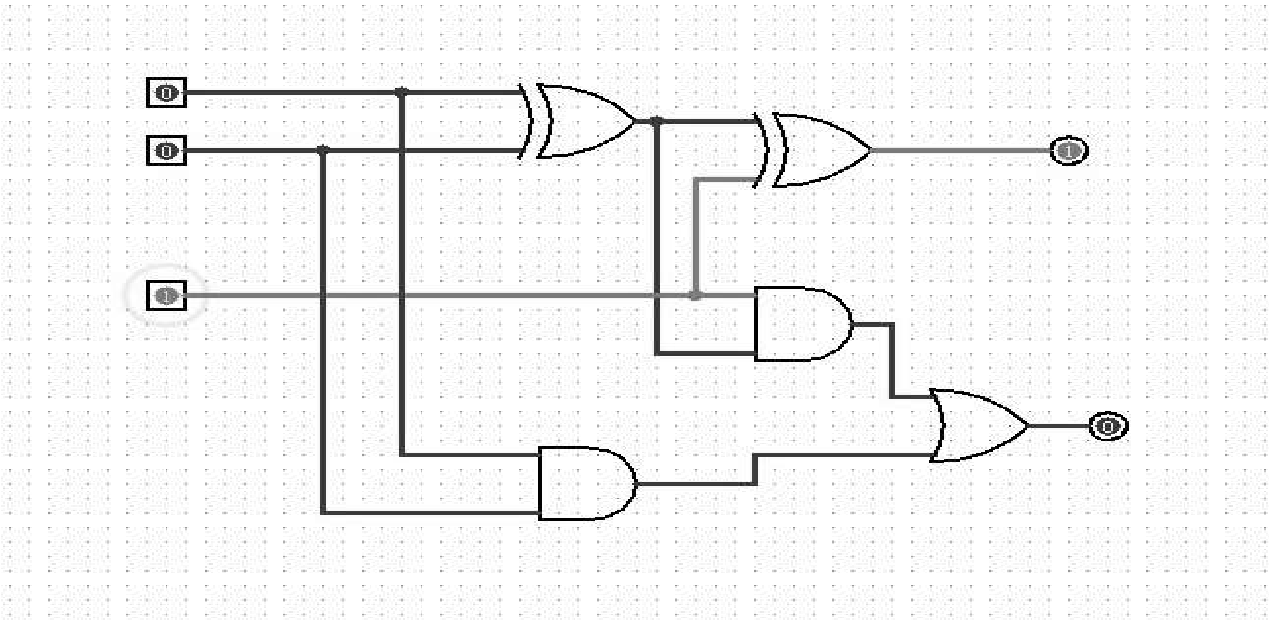


FULL - ADDER

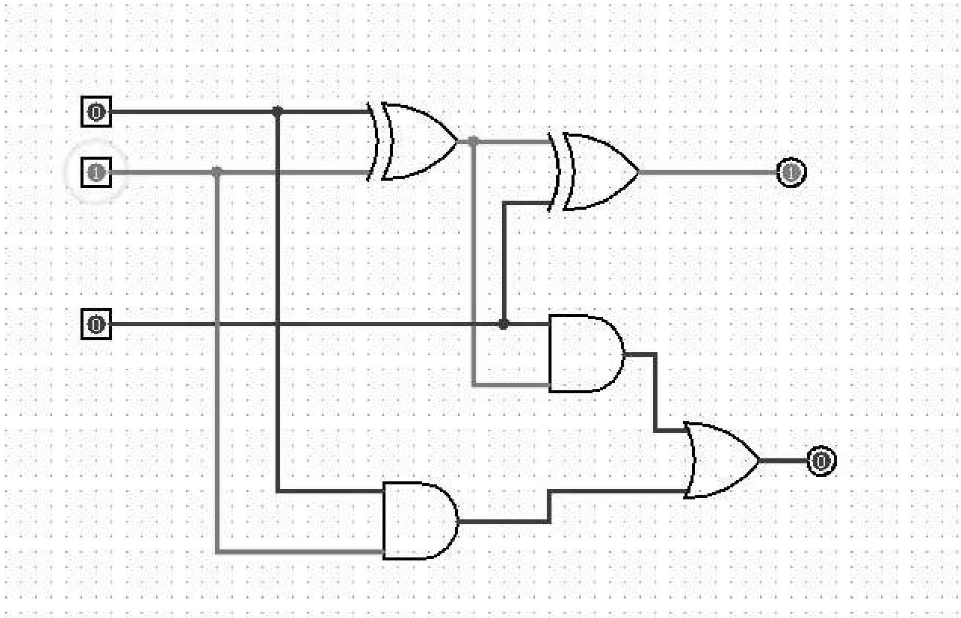
1. When A is 0, B is 0 and Cin is 0 , Sum (S) is 0 and Carry out (Cout) is 0



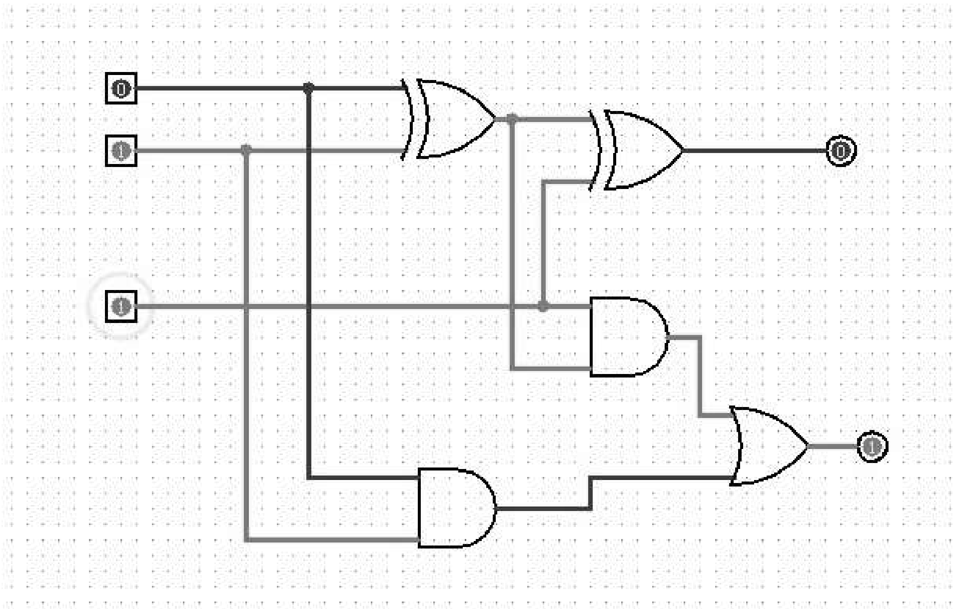
2. When A is 0, B is 0 and Cin is 1 , Sum (S) is 1 and Carry out (Cout) is 0.



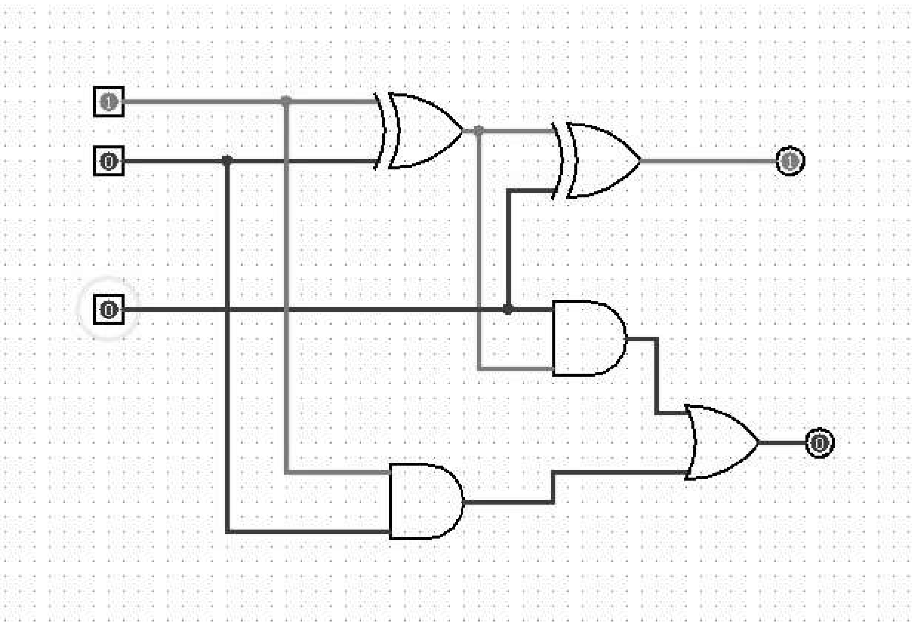
3. When A is 0, B is 1 and Cin is 0 , Sum (S) is 1 and Carry out (Cout) is 0.



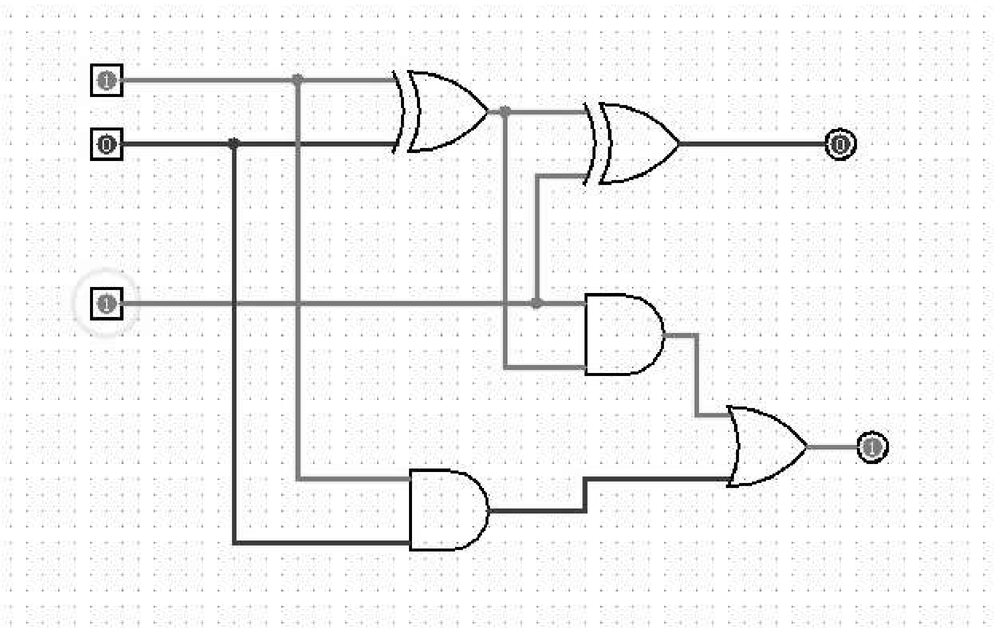
4. When A is 0, B is 1 and Cin is 1 , Sum (S) is 0 and Carry out (Cout) is 1.



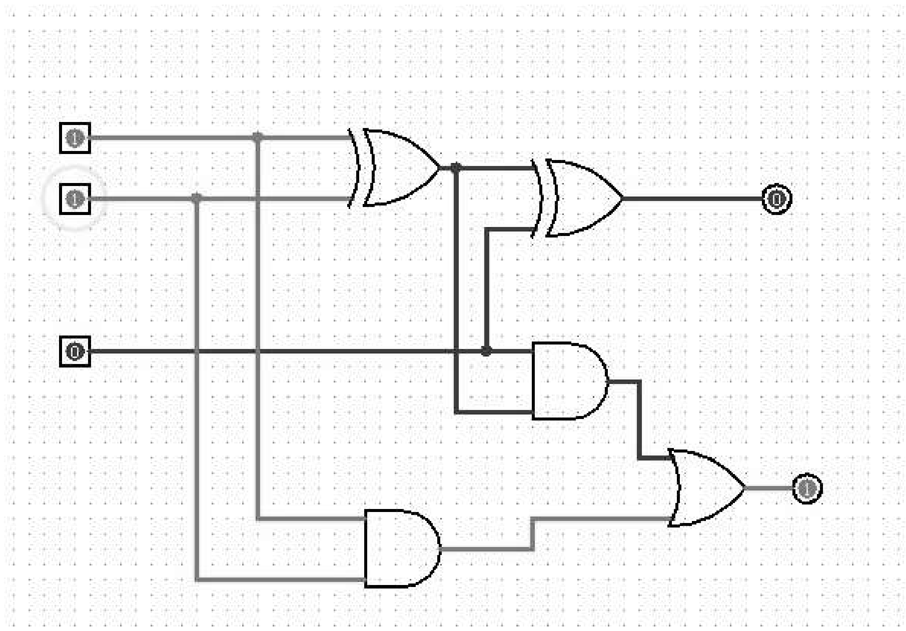
5. When A is 1, B is 0 and Cin is 0 , Sum (S) is 1 and Carry out (Cout) is 0.



6. When A is 1, B is 0 and Cin is 1 , Sum (S) is 0 and Carry out (Cout) is 1.



7. When A is 1, B is 1 and Cin is 0 , Sum (S) is 0 and Carry out (Cout) is 1.



8. When A is 1, B is 1 and Cin is 1 , Sum (S) is 1 and Carry out (Cout) is 1.