



MANIPAL INSTITUTE OF TECHNOLOGY

Assignment II (Part A)

A assignment report submitted in fulfillment of the requirement for the completion of the assignment 2 (part A) of digital VLSI design, a subject of

**MASTER OF TECHNOLOGY
In
MICROELECTRONICS**

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6T SRAM

1 a. Design a six-transistor CMOS SRAM cell and perform its simulation.

(i) Do the transistor sizing and calculate the cell ratio. Check the design for various modes of operation

a. Standby mode,

b. Write Mode for both logic 0 and 1

c. Read mode for both logic 0 and 1

(ii) Draw the stick diagram and layout of the cell. Perform the post-layout simulation and check whether both the results are relatively equal or not. If so, highlight the cause and possible remedies.

(iii) Calculate the various power dissipations during read and write mode.

(iv) Calculate the static noise margin (SNM) of your cell using the "butterfly curve."

(v) Perform the process corner analysis and discuss the effects of transistor sizing in the cell qualitatively.

(vi) Finally, Generate a GDS II file for your design.

After all the analysis, can you develop the design specification of your proposed SRAM cell?

INTRODUCTION:

A 6T SRAM cell is a widely used memory cell configuration in digital integrated circuits, offering high-speed performance and robust data stability. The "6T" designation refers to the six transistors that make up each cell: four for the core latch that stores a bit of data and two additional access transistors for reading and writing data. This structure provides a balance between area efficiency and data stability, making the 6T SRAM cell ideal for cache memory in processors, where speed and reliability are critical.

The basic operation of a 6T SRAM cell leverages the bistable nature of cross-coupled inverters to hold a stable logic state '0' and '1' without the need for refreshing, unlike dynamic RAM cells. When data is written, the access transistors enable the bit lines to set the state of the cell. During a read operation, these same transistors allow the stored state to be sensed on the bit lines, aided by pre-charged sense amplifiers. The design of a 6T SRAM cell allows it to retain its data as long as power is supplied, making it "static" in nature.

While the 6T SRAM cell is efficient in terms of read/write performance, it faces challenges with area and power consumption as technology scales down. Transistor dimensions must be carefully managed to ensure reliable performance, and leakage currents need to be minimized for power efficiency. As a result, ongoing research in SRAM technology aims to enhance the performance, stability, and density of 6T SRAM cells for modern applications in low-power and high-performance computing.

LITERATURE SURVEY:

In the first paper named "Design of Gate-All-Around Silicon MOSFETs for 6-T SRAM Area Efficiency and Yield" the author makes use of gate all round MOSFET relevant for the 11.9-nm CMOS technology node and are optimized with device dimensions following the scale length rule. This design has been done with the help of synopsis TCAD tool. The tradeoff between read stability and write ability of 6-T static RAM cell designs implemented with GAA MOSFETs with either square or rectangular nanowire channel regions is then investigated, and a calibrated

6T SRAM

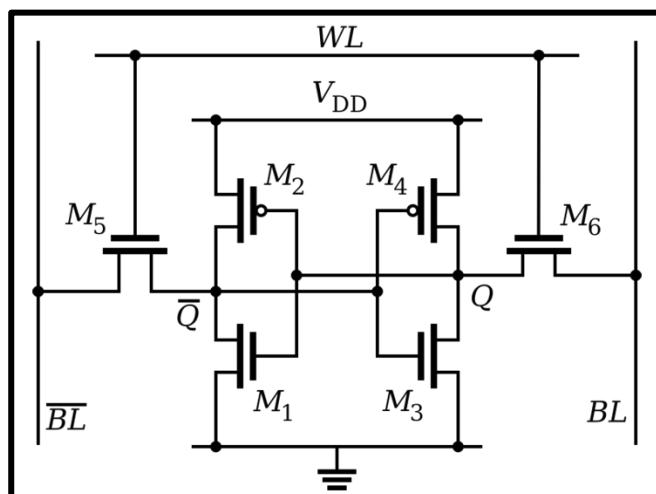
transistor IV compact model is used to estimate cell yield.

In the second paper named “Static Noise Margin Analysis of 6T SRAM” the author presents the static noise margin (STM) analysis of the most favored 6-transistor SRAM or the 6-T SRAM. The STM analysis has been performed for various parameters such as temperature, drain voltage, cell ratio, and threshold voltage to obtain optimization. For memory elements like SRAM consume the majority of the silicon area in a typical integrated circuit, the optimization is critical for major requirements like portability, operating speed, and reduced power consumption etc.

In the third paper named “A New SRAM Cell Design for Both Power and Performance Efficiency” the author presents a new six-transistor static random-access memory cell with significantly reduced power consumption that achieves high read and write performance. This design implemented with UMC 90 nm, 1.0-V supply voltage CMOS technologies. Compared to conventional six transistor SRAM cells, the new cell design reduces power consumption by 40-60%.

The fourth and fifth reference is the books I have referred for my design. These 2 books will give the correct direction for the design of the 6T SRAM.

SCHEMATIC OF 6-T SRAM:



Schematic of a 6-T SRAM (Ref: Wikipedia)

The schematic of the 6-T SRAM is as shown in the figure. The transistors M1 and M2 will form an inverter, and similarly the transistors M4 and M3 also forms an inverter. These 2 inverters will be inter connected to each other. This is the main circuit which is used for storing the bit. M5 and M6 are called the access transistors, where these two transistors gates are connected to each other. This control is called as the write line. When write line is high then the access transistors will be turned ON and if write line is low then the access transistors will be turned OFF. The source or drain of these access transistors will be connected to the bit line and bit line bar. These bit line and bit line bar are crucial for the operation of the SRAM, because for read operation we will be accessing the data to this line and for write operation we will be giving the data from this line. Hence this line is very important.

The points Q and Q bar are the 2 node points where the data can be taken out or written into the actual SRAM cell. Suppose if we are doing the write operation the data should be written to

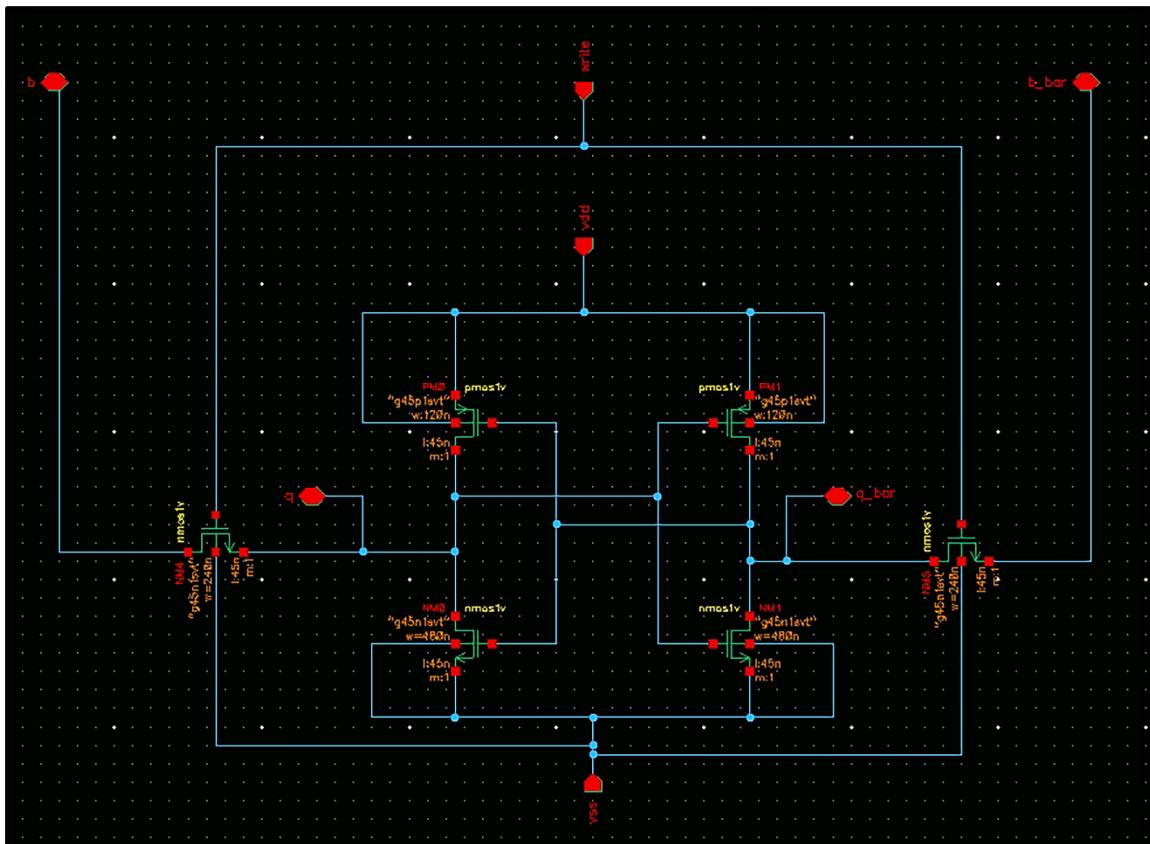
6T SRAM

the point Q and while reading, we should be reading the data from this point. If Q is high then data read should be high else low.

DESIGN METHODOLOGY:

The design and simulation of the 6T SRAM cell is conducted in Cadence Virtuoso software. First we will be doing the schematic design and then for the cell designed we are designing a testbench for analysis and simulation. For simulation we will be using ADEL simulator. Next after this we will be designing the layout of the cell and do the DRC and LVS test, later will do the quantus design and for the generated view we will be doing the post layout simulation again for the designed layout. Next for the design we will be checking the power analysis and SNA for the design. The complete details of the design will be given below.

(i) SCHEMATIC OF SRAM AND TRANSISTOR SIZING:

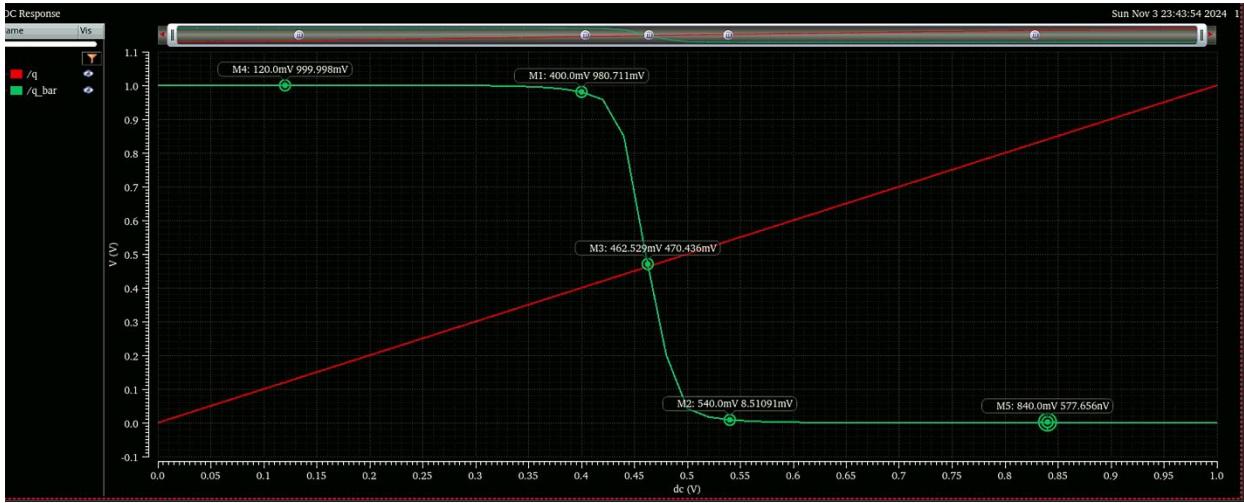


The schematic of the 6T SRAM is designed as shown above. In the above schematic we have used 6 transistors of different sizes. The set of transistors i.e. PM0 and NM0 is one inverter and another set of transistors i.e. PM1 and NM1 is another inverter. As we can see in the schematic these two inverters are interconnected with each other. One inverter output is connected to another inverter input and vice versa.

We have also put 2 inout pins names q and q_bar, these inputs are like the inputs that we can give to the inverter and also the value that is stored inside the inverter can be used by these pins.

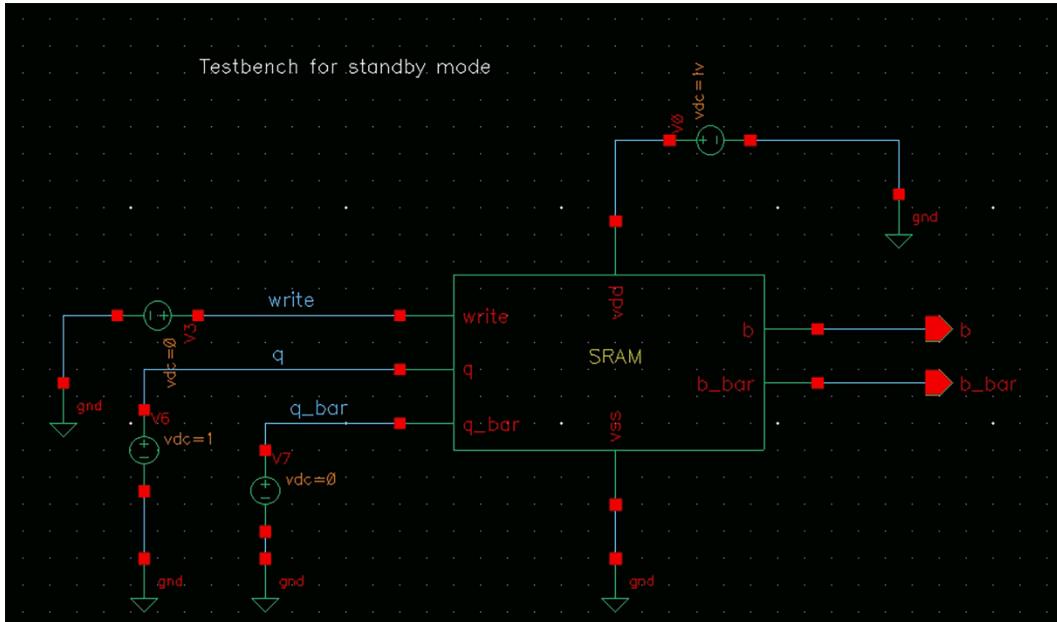
Also, we have another set of inout pins those are b and b_bar. These are connected to the access transistors i.e. NM4 and NM5. These transistors are controlled by the write pin.

6T SRAM



In the above figure we have plotted the DC characteristics of the SRAM design. As we can see we have 2 plots i.e. q and q_bar that we have plotted. The actual DC voltage is varied from 0V to 1V. the write signal, b and b_bar signal is given by the pulse signal.

(ii) STANDBY MODE OF OPERATION

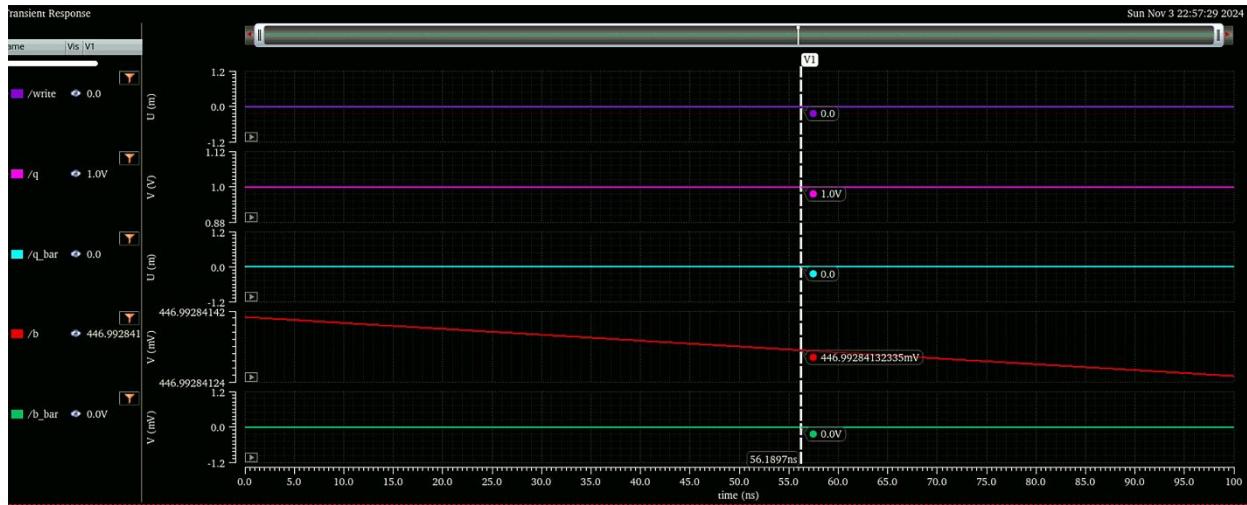


The above figure is the design that we have used as the testbench for the simulation of the standby mode. Basically, the standby mode is the type of operation mode when the SRAM is either not used for fetching the data nor writing the data. For this operation we will be setting the write pin to 0V.

Since the write pin is 0V the access transistors will be turned off and hence the interconnected inverter will not be in contact with the b and b_bar pin. Hence, we cannot fetch anything from the SRAM not write anything from the SRAM.

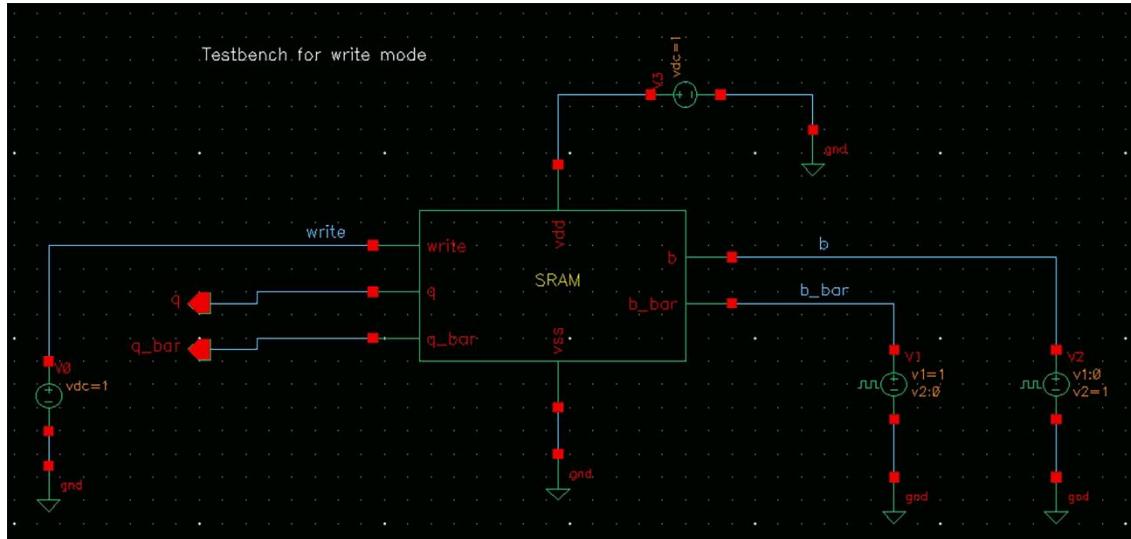
The q value and q_bar value are given as 1V and 0V respectively. This will tell us that the SRAM is storing the value of 1 and 0 at the points q and q_bar.

6T SRAM



The transient analysis of the SRAM is as shown in the above figure. As we can see the bit and bit_bar is almost equal to 0V. This shows that if access transistors are turned off then the data is not shared to the output pins.

(iii) WRITE MODE FOR BOTH LOGIC 0 AND 1

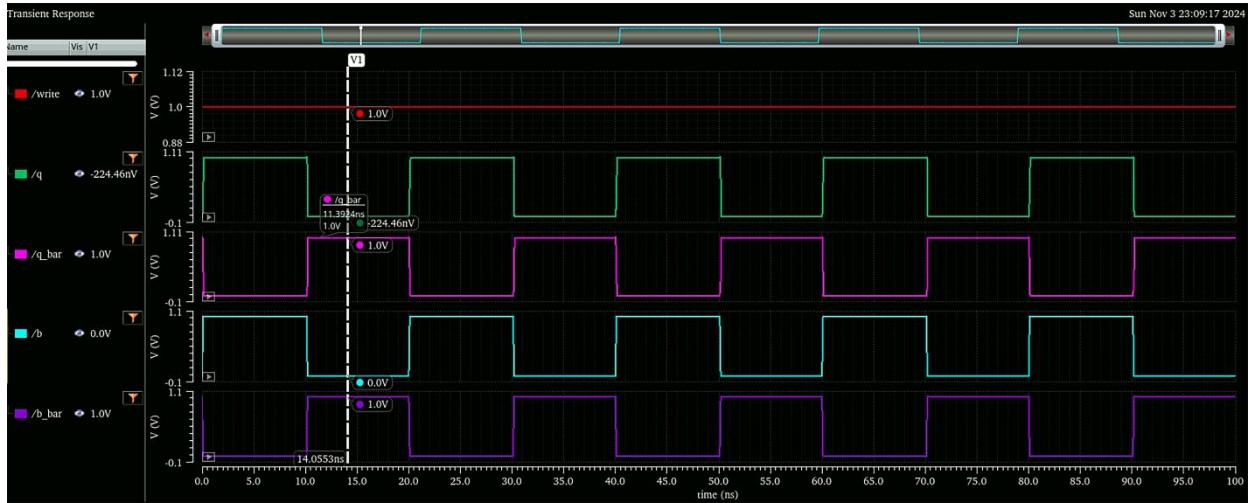


Testbench of write mode test bench

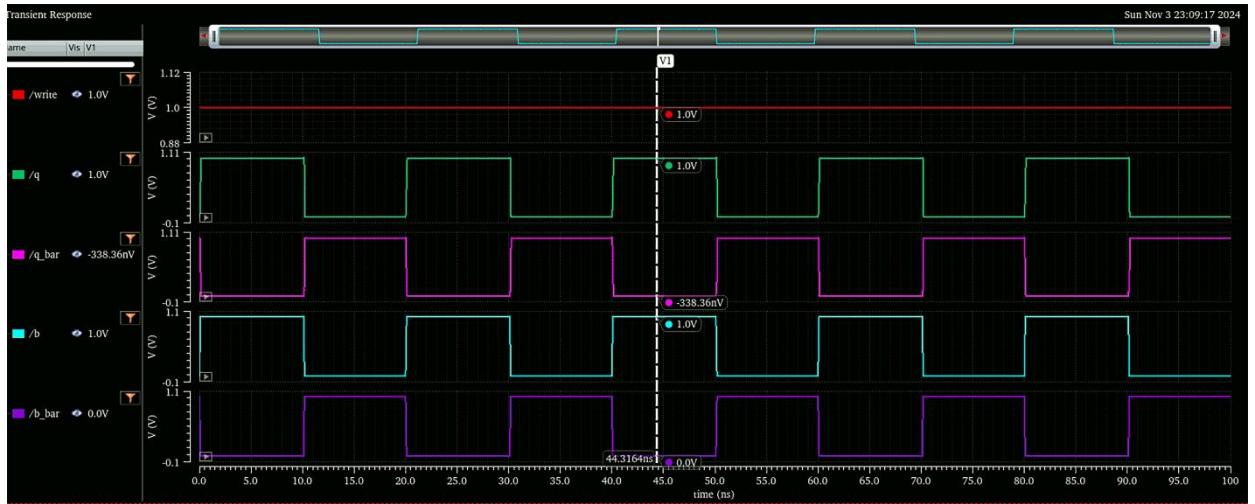
As we can see the testbench for the write mode is as shown in above picture. Here the write pins is given a positive supply voltage and both the access transistors are turned ON.

For this working the data which is present in b and b_{bar} should reflect to the q and q_{bar} . By this we verify that the data from out pins is sent to the input of the SRAM

6T SRAM



Waveform for write mode

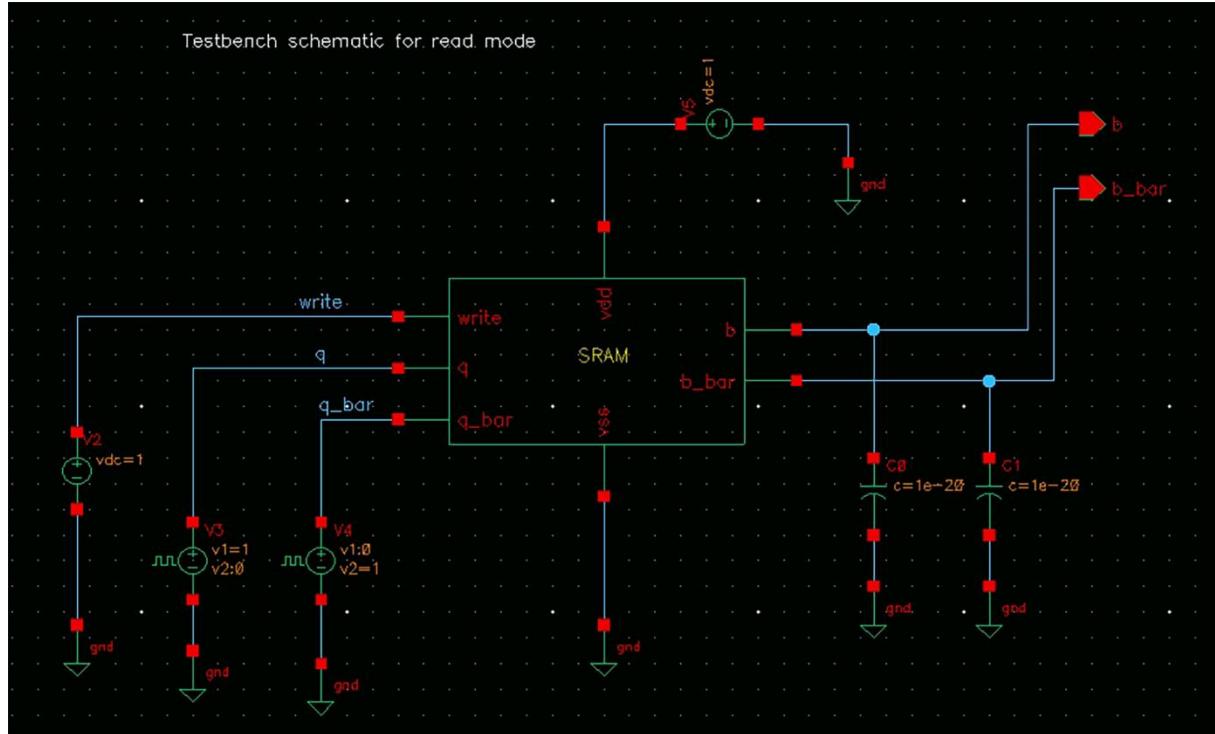


Waveform for write mode

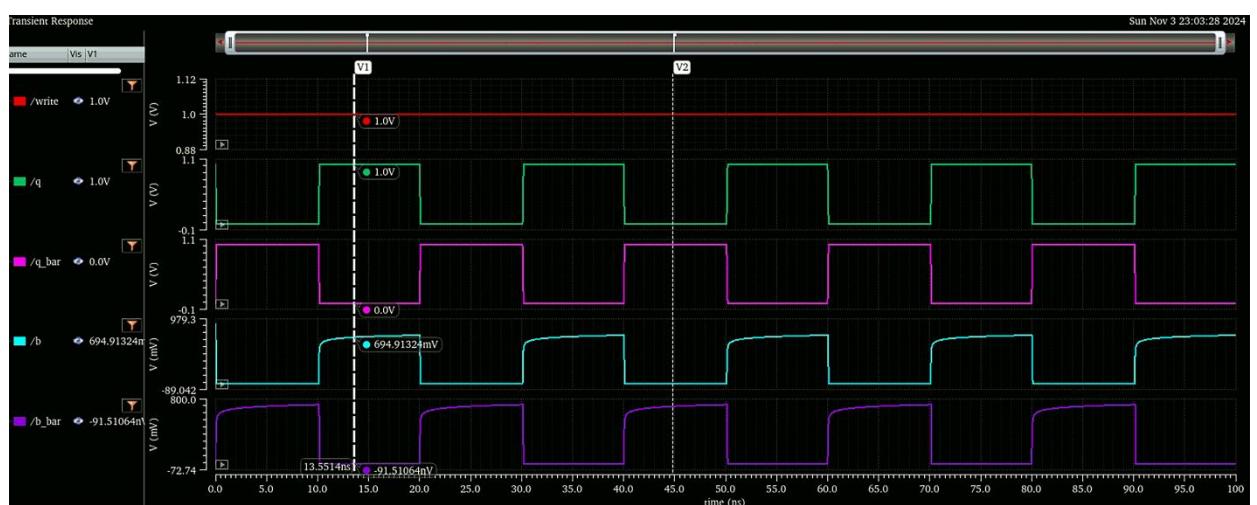
As we can see in the above waveform the data in b and b_{bar} is completely written to the q and q_{bar}. If we observe the testbench we are taking the output data from the q and q_{bar}.

We can also observe that the write pin is charged to Vdd i.e. voltage high. So now we can confirm by saying that the access transistors are turned ON.

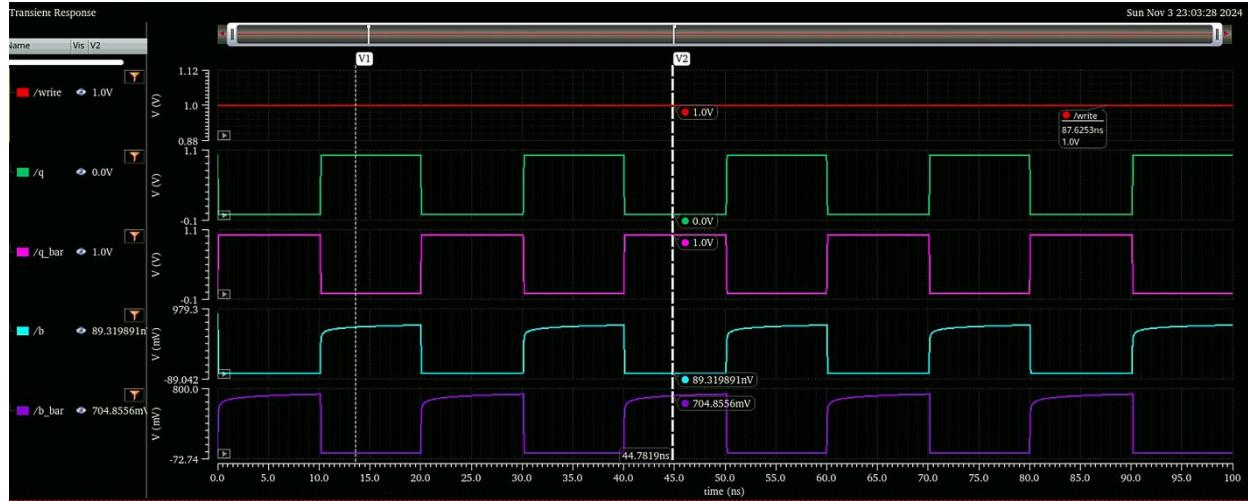
(iv) READ MODE FOR BOTH LOGIC 0 AND 1



As we can see in above testbench, the write pin is given the high voltage or supply here also. We have also added the capacitors at the output pin of the SRAM, to hold the read value for some amount of time. Here the data which is present in the q and q_bar must be read to the output pin i.e. b and b_bar.



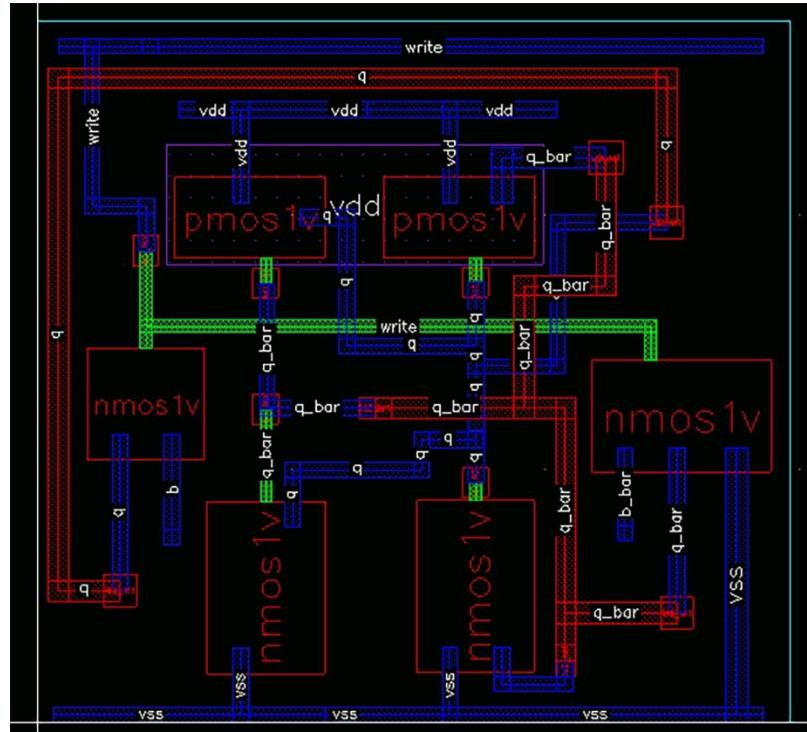
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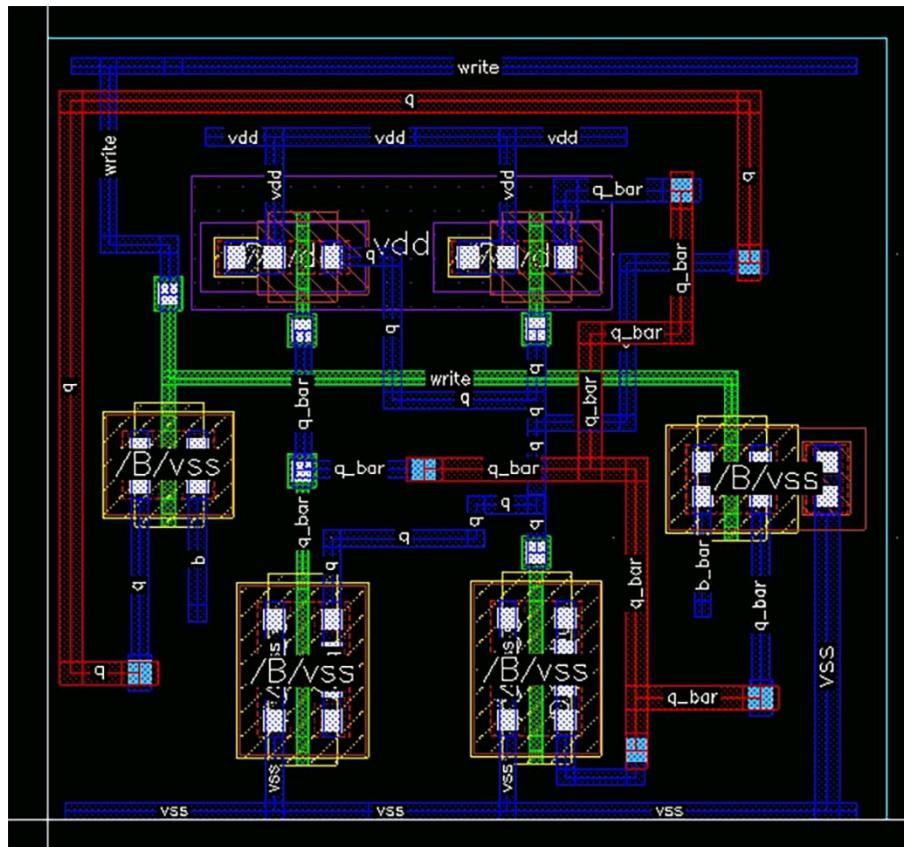
Waveform of the read mode of the SRAM

As we can clearly observe from the waveform, the b and b_bar is same or reading same as that of the q and q_bar. We can also observe that the charging and discharging of the output pins i.e. b and b_bar.

(v) STICK DIAGRAM AND LAYOUT OF THE CELL



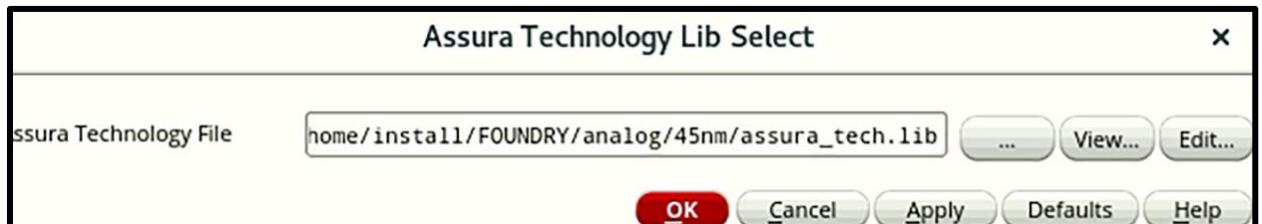
Layout of the SRAM cell



Layout of the SRAM cell

As we can see in the above pictures, we have completed the SRAM cell layout design. We have used 2 metals for the complete design from the layout.

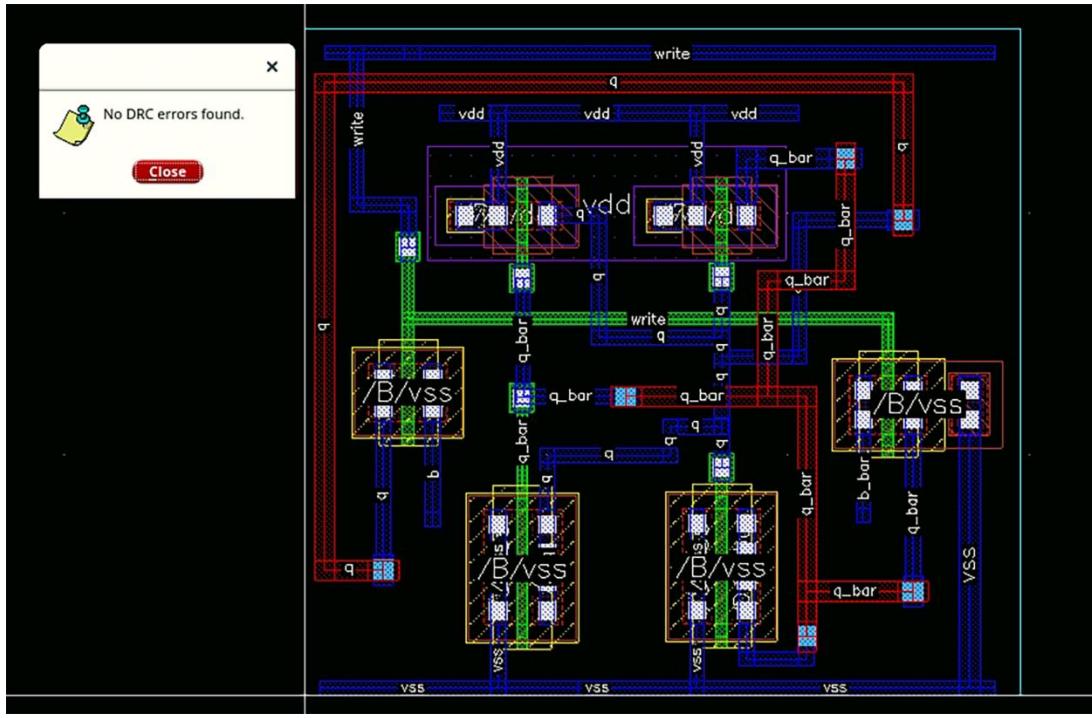
(vi) TECHNOLOGY LIBRARY USED



Technology file used

We can observe from the above picture that we have used 45nm technology library for the layout validation or tests like DRC, LVS and Quantus.

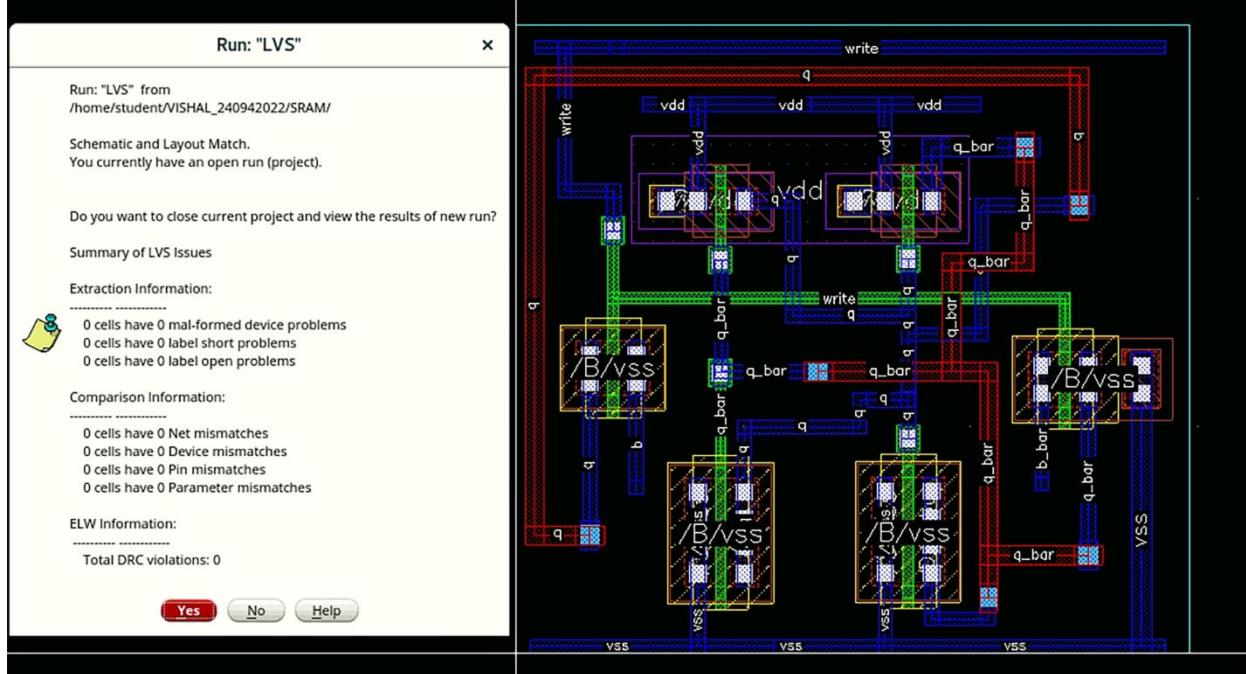
(vii) DESIGN RULE CHECK (DRC)



DRC test done

As we can see in the above diagram, we can see that the design we have done is passing the DRC rules check of the 45nm technology.

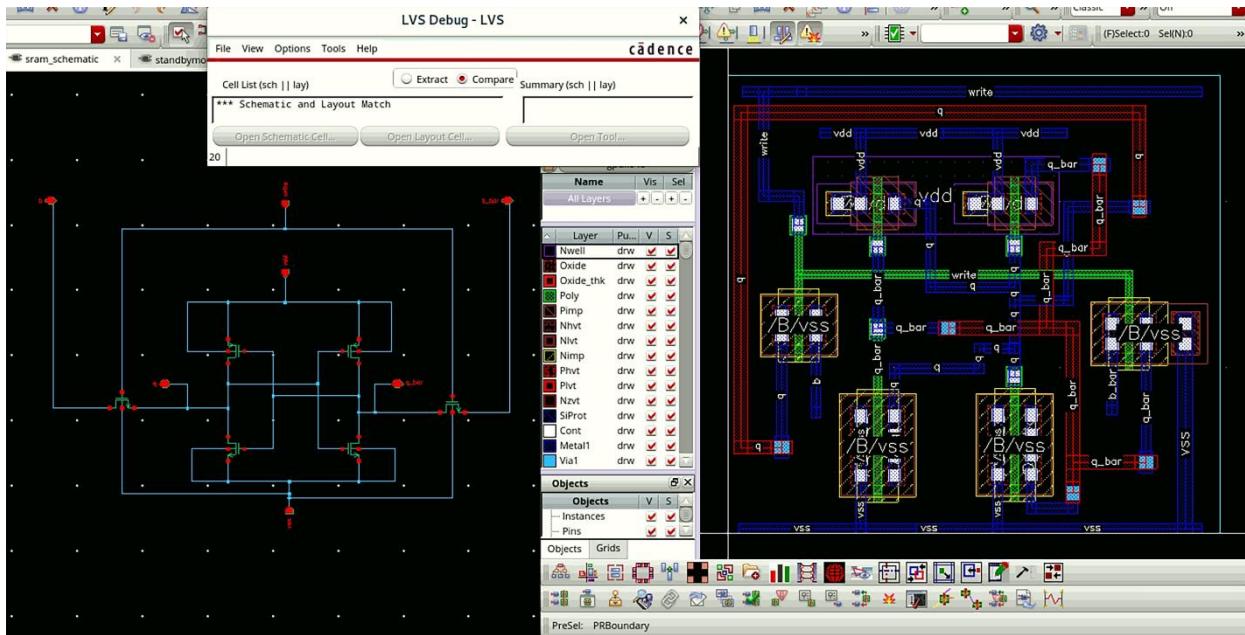
(viii) LAYOUT VERSUS SCHEMATIC (LVS)



LVS test done

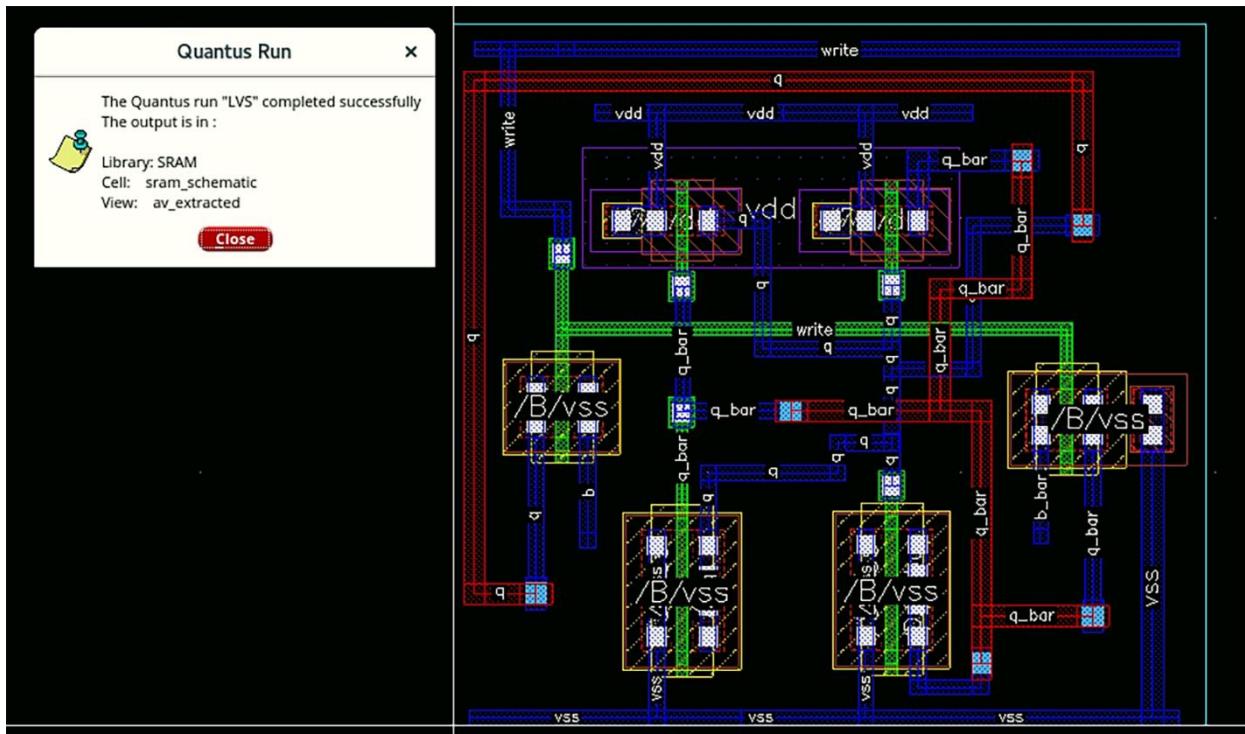
As we can see the design is passing the layout versus schematic test. This means that the schematic and layout is matching completely.

6T SRAM



layout versus schematic matched

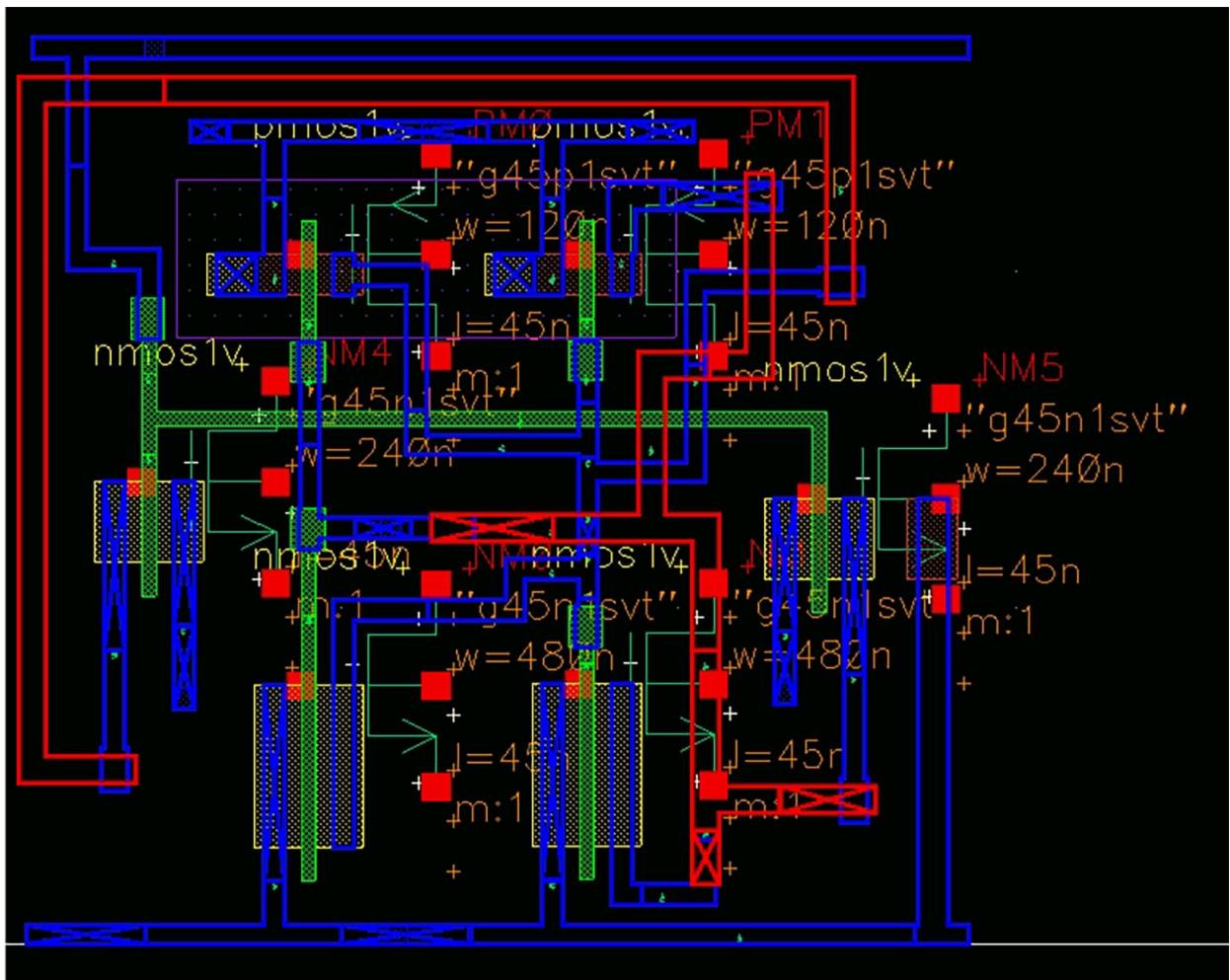
(ix) QUANTUS RUN



Quantus run test done

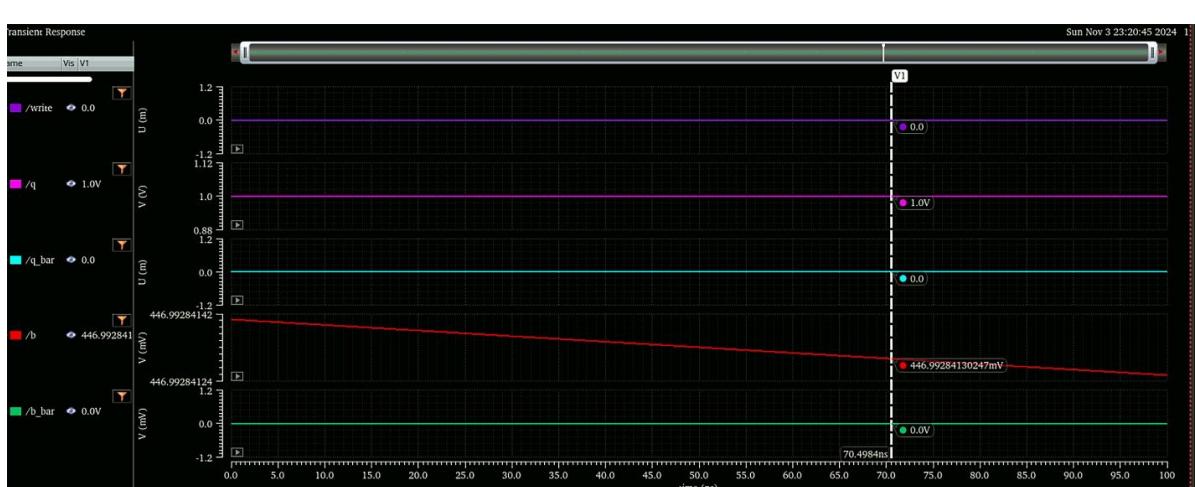
As we can see in the above picture the RC extraction process which is done using quantus is done to our design and quantus run is successfully done.

(x) AV_EXTRACTED FILE



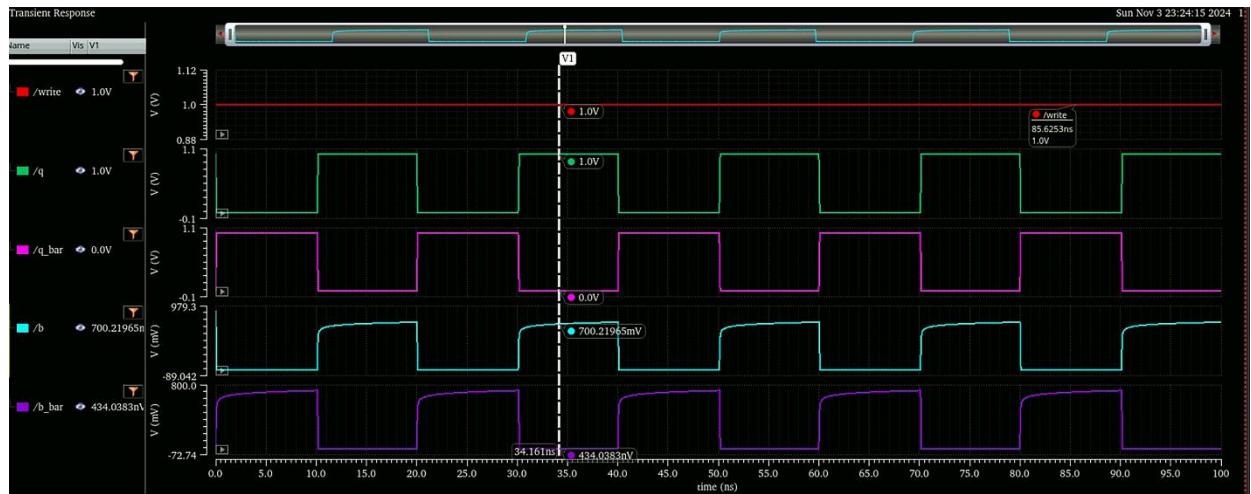
As we can see in the above figure after quantus test, this AV_Extracted file is generated and the SRAM cell is looked like this finally.

(xi) POST LAYOUT ANALYSIS



Post layout analysis of standby mode

6T SRAM



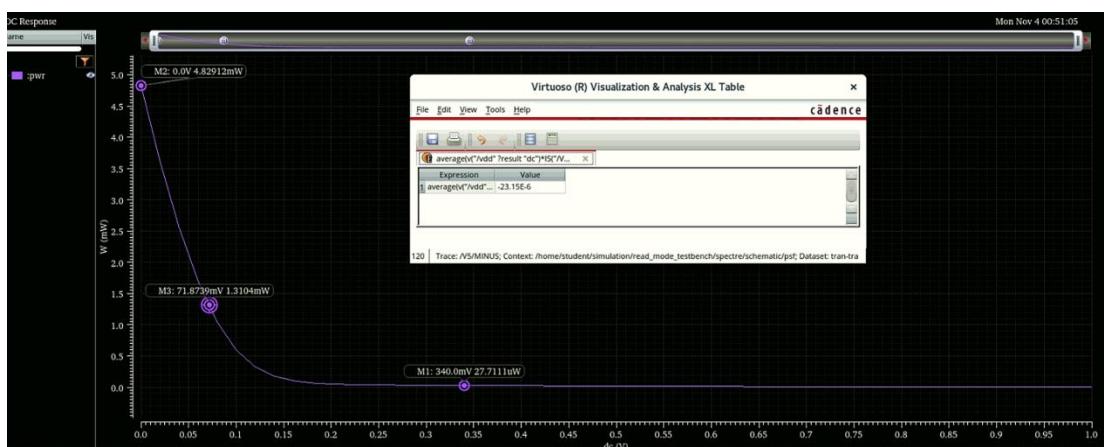
Post layout analysis of the read mode



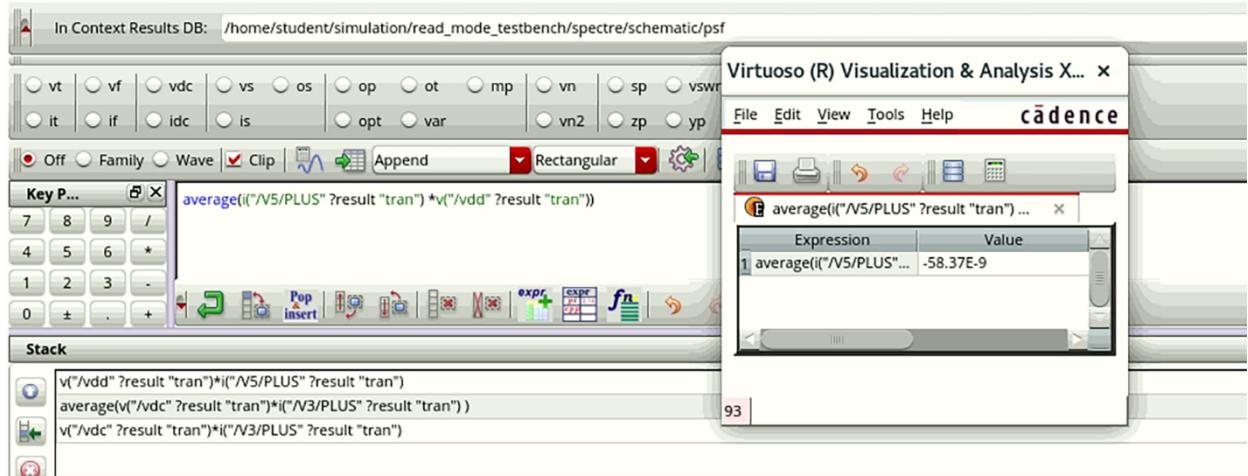
Post layout analysis of the write mode

As we can see in the above waveforms, we did the transient analysis on the post layout design and output is same as pre layout simulation that we had done before. This confirms that the layout design is completed successfully

(xii) POWER DISSIPATION DURING READ AND WRITE OPERATION OF THE CELL

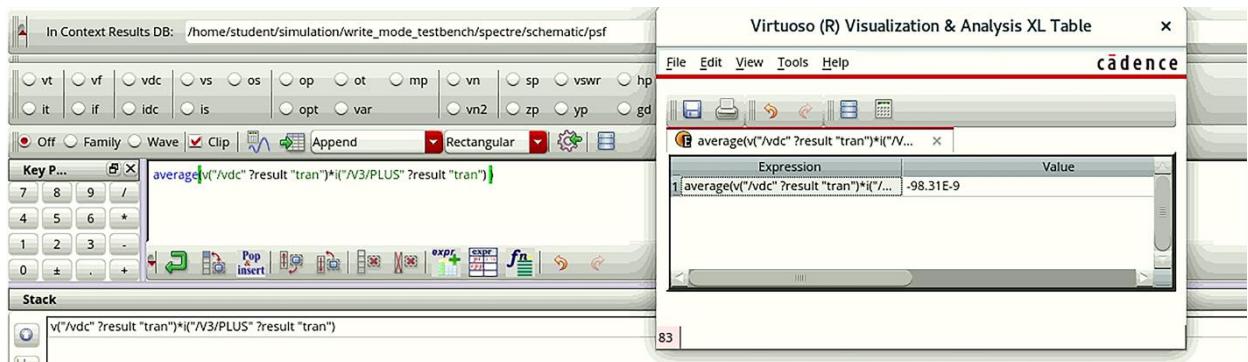
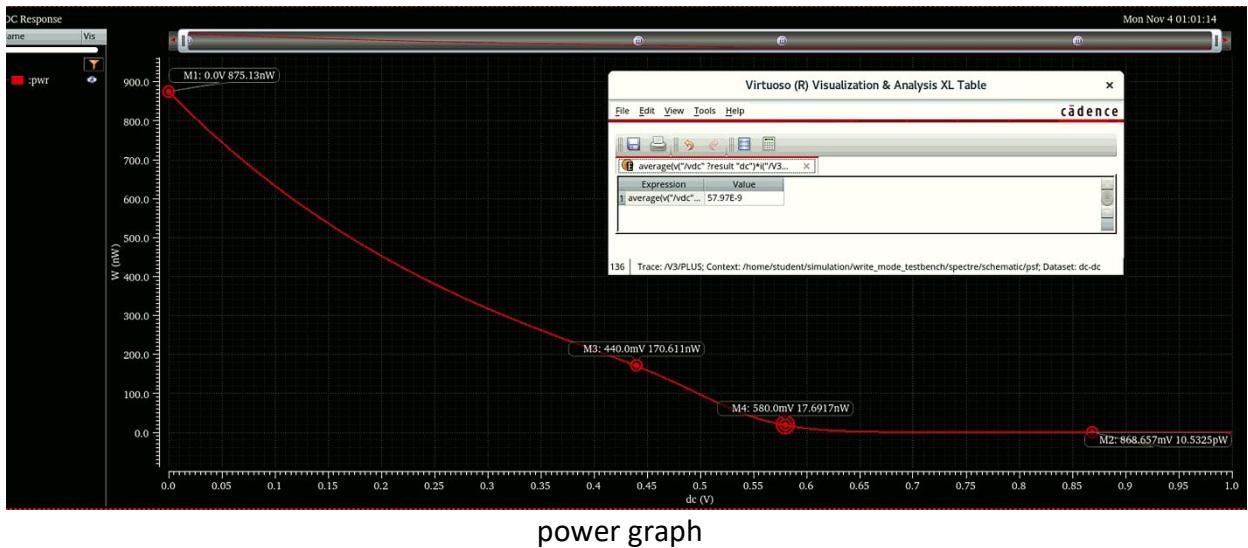


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Power analysis for the read mode

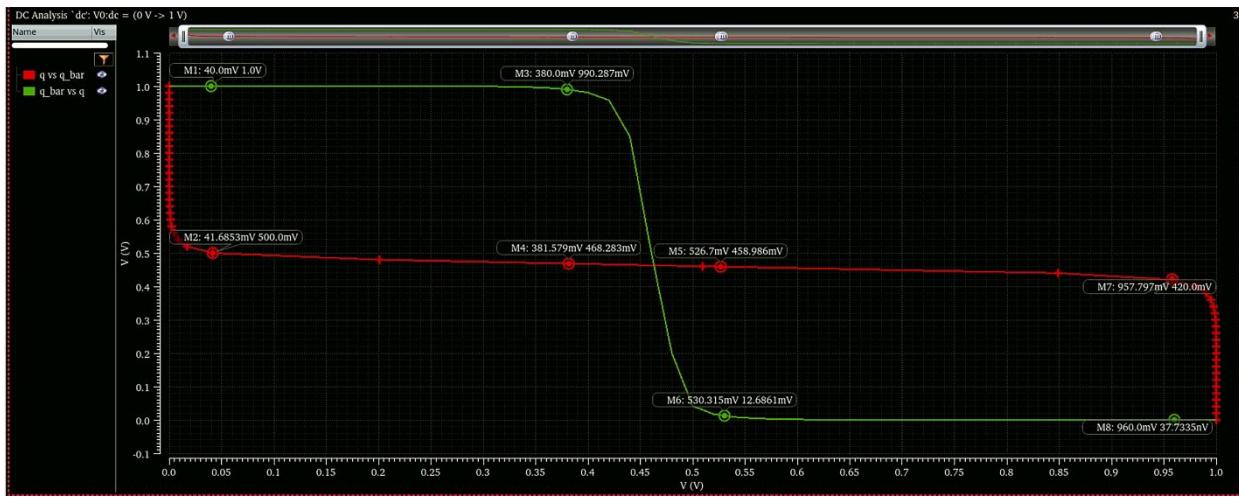
As we can see from the above graph, we know that the average power that we are getting is around 58nW.



Power analysis for write mode

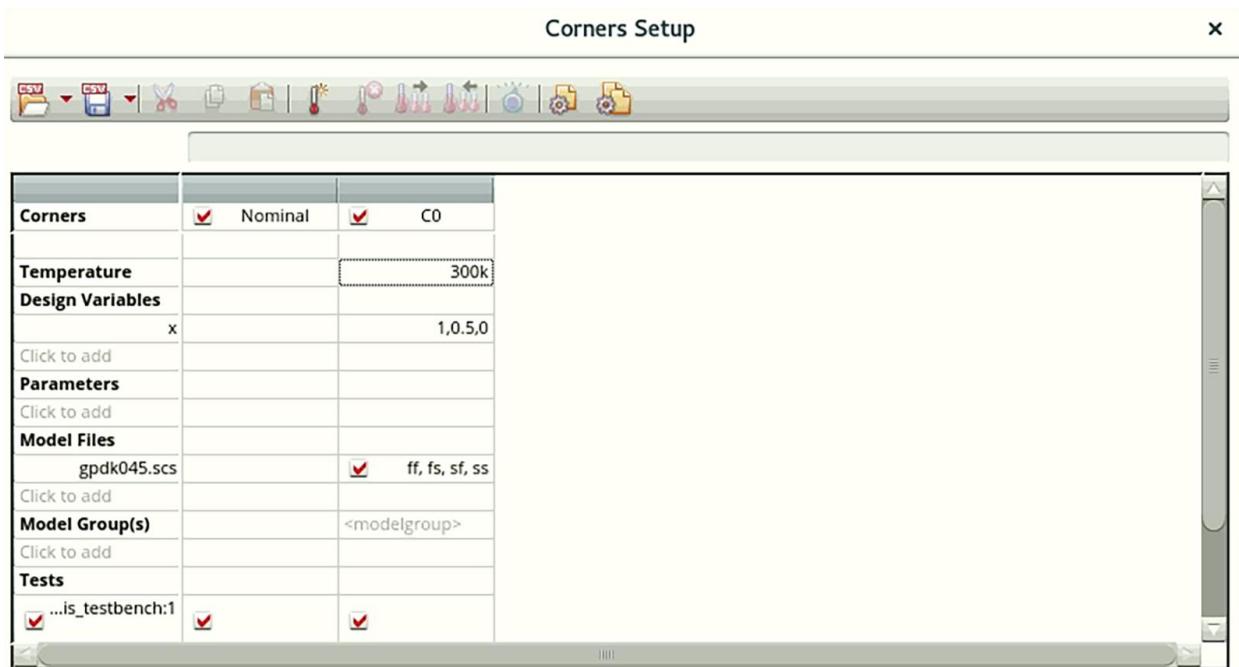
As we can see from the above graph, we know that the average power that we are getting is around 98nW.

(xiii) STATIC NOISE MARGIN OF THE CELL USING BUTTERFLY CURVE

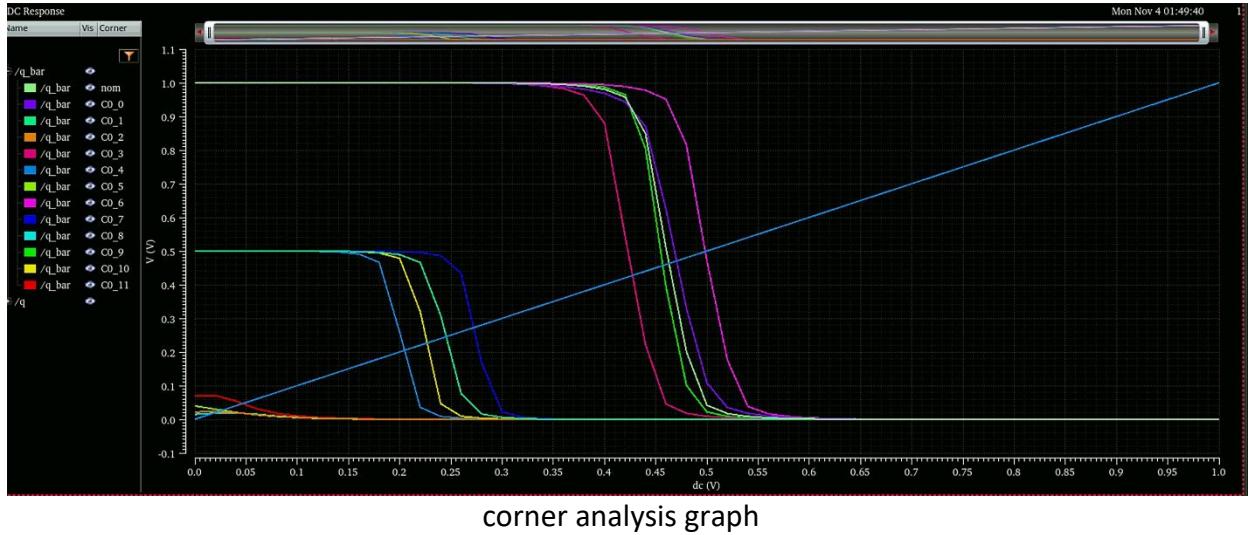


Static Noise Margin (SNM) for SRAM (Static Random Access Memory) is a measure of the stability of an SRAM cell, specifically its ability to retain data without flipping state due to noise or disturbances. It indicates the maximum noise voltage that can be tolerated by the SRAM cell before it loses its data, making SNM a crucial factor in determining the robustness and reliability of SRAM cells.

(xiv) PROCESS CORNER ANALYSIS



6T SRAM



As we can see in the above graph we can see the graph of DC characteristics of different supply voltages. If we observe the graph, we can see for higher voltages we are getting different DC characteristics.

(xv) GDS II FILE



GDS file generated

As we can see, since we have completed the schematic, layout and post layout simulation we have generated the GDS file. This file is used by the foundries for the manufacturing of the design on the chip.

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