DESIGN AND IMPLEMENTATION OF THE 4-BIT ALU USING 90nm CMOS TECHNOLOGY

Submitted by

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CERTIFICATE

This is to certify that the project entitled **Design and implementation of 4-bit ALU using 90nm CMOS technology** was carried out by **Vishal Sanjay Raju** (*Reg. No. 240942022*) under my guidance for the fulfilment of the requirement for the completion of RMTC Lab during the academic year 2024.

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Last but not least, I wish to acknowledge our Parents and Friends for giving moral strength and encouragement.

ABSTRACT

This paper presents a 4-bit Arithmetic Logic Unit (ALU) design and implementation using 90nm CMOS (Complementary Metal-Oxide-Semiconductor) technology. The ALU is a fundamental building block of any central processing unit (CPU), microcontroller unit (MCU), GPU's, DSP's etc. and is responsible for performing arithmetic and logical operations. The design process involves the schematic design of adder, subtractor, comparator, 1's complement and decoder for the development of the ALU architecture followed by simulation of the design using Cadence Virtuoso EDA (Electronic Design Automation) tools. The implementation phase focuses on layout design to ensure the functionality and manufacturability of the ALU. The performance metrics such as power consumption, area, and speed are analysed to validate the efficiency of the design. The successful realization of the 4-bit ALU showcases the potential for advancements in integrated circuit design and the practical application of CMOS technology in modern computing systems.

Keywords*: ALU, adder, 90nm, CMOS, virtuoso.*

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CHAPTER 1
INTRODUCTION

This chapter introduces the project which focuses on designing 4-bit Arithmetic Logic Unit or also called as ALU is a digital circuit that performs a range of arithmetic and logical operations on 4-bit binary numbers. As one of the core components in processors, the ALU enables execution of basic calculations and decision-making tasks, serving as the "computational brain" within microprocessors, digital signal processors (DSPs), and embedded systems. By working with 4-bit data units, this ALU is suited for small-scale computing applications and educational purposes, providing a compact yet functional approach. The ALU consists of many blocks like adder, subtractor, magnitude comparator, 1’s complement and decoder.

The 4-bit ALU design typically includes two main categories that is, arithmetic operations for numerical calculations and logical operations for bitwise manipulations. This design enables efficient processing of data, allowing for basic computing and control logic functions that are essential in various digital systems. Implementing a 4-bit ALU also provides insights into the key principles of digital design, such as binary arithmetic, circuit simplification, and the integration of logical gates to achieve multifunctional capability. Its simplicity makes it a versatile tool in digital electronics, ideal for introductory learning as well as foundational experiments in more complex digital architectures.

1.1. Introduction to the area of work

This project presents the design and implementation of a 4-bit Arithmetic Logic Unit (ALU) using Cadence Virtuoso software, making use of the 90nm CMOS technology node. The 4-bit ALU serves as a fundamental component in digital processors, performing a range of essential arithmetic and logical operations on binary data. Designed with compactness and efficiency in mind, the ALU can execute basic functions such as addition, subtraction, magnitude comparison, 1’s complement and decoder block all critical for various computational tasks in microprocessors, digital signal processing units, and embedded systems. By using 90nm CMOS technology, the ALU achieves a balance between performance, area, and power consumption, which is crucial in modern, resource-constrained digital circuits.

1.2.Present day scenario of the area of work

This project, while not at the forefront of modern high-performance computing, remains highly relevant in educational settings and certain low-power applications. This project provides foundational experience in CMOS technology, enabling students and researchers to explore critical concepts such as power optimization, timing, and layout design without the added complexity of advanced nodes. In practical applications, 90nm technology is still used in cost-

sensitive and low-power devices, such as IoT and embedded systems, where high performance is less crucial than efficiency and reliability. Additionally, the skills and principles gained from designing a 4-bit ALU at this node are directly applicable to more complex digital circuits and can serve as a stepping stone for scaling designs to smaller, modern nodes.

1.3.Motivation to do the Project work

- **Shortcomings in the previous work**:

  Previous work on 4-bit ALU design using 90nm CMOS technology has highlighted several limitations, primarily related to performance and power efficiency. Designs at the 90nm node often encounter higher leakage currents and increased power dissipation compared to smaller technology nodes, which can impact energy-sensitive applications. Additionally, earlier implementations may have limited functionality, with a focus on basic arithmetic and logic operations without optimized handling for delay and noise. Furthermore, previous designs might lack layout optimization, resulting in increased area consumption, which is less efficient for integration into larger systems. These shortcomings suggest opportunities for refining power management, minimizing delay, and enhancing layout compactness in future designs.

- **Importance in present context**:

  In the present context, designing a 4-bit ALU using 90nm CMOS technology holds importance as it bridges foundational digital design principles with practical applications in low-power and embedded systems. While advanced technology nodes are prioritized for high-performance computing, 90nm remains relevant for educational purposes and cost-effective applications, particularly in IoT and low-power devices. This technology node provides a suitable balance between complexity and manufacturability, making it accessible for academic projects and prototyping. Furthermore, understanding ALU design at 90nm prepares designers to tackle modern challenges, including power efficiency and circuit optimization, which are increasingly crucial in today's energy-conscious computing landscape.

- **Uniqueness of the methodology**:

  The methodology for designing a 4-bit ALU using 90nm CMOS technology is unique in its comprehensive approach to balancing performance, power, and area constraints at a modest scale. Unlike traditional designs that may focus solely on functionality, this methodology incorporates meticulous steps for optimizing layout, reducing leakage, and minimizing delay, tailored specifically for the 90nm node. By leveraging Cadence

Virtuoso for precise schematic and layout creation, the design achieves both accuracy and efficiency, ensuring robustness against noise while meeting target specifications. This method also integrates iterative testing and simulation to refine the ALU's performance, making it a versatile and scalable approach suitable for low-power applications and adaptable for educational or industrial uses.

1.4. Significance of possible end result

The significance of the anticipated end results a fully functional 4-bit ALU designed using 90nm CMOS technology lies in its potential to serve as a foundational building block for low-power digital systems and as an educational model for digital circuit design. Achieving a balanced design with optimized power, area, and speed characteristics at this node could make the ALU suitable for integration in cost-sensitive applications, such as simple processors in IoT devices or embedded controllers. Additionally, the successful completion of this project demonstrates a hands-on application of CMOS design principles, providing valuable insights into the trade-offs involved in circuit design. The refined end result could also serve as a reliable framework for future projects, facilitating enhancements or adaptations to more complex architectures or more advanced technology nodes.

1.5. Objectives of the work

- To design and implement a 4-bit ALU that performs essential arithmetic and logic operations, including addition, subtraction, comparison, 1's complement and decoding with accuracy and stability.
- To optimize the ALU's layout in 90nm CMOS technology, minimizing area and power consumption while maintaining efficient performance for potential low-power applications.
- To evaluate and validate the ALU's functionality through simulation and testing, ensuring robustness against noise and reliability across various operating conditions.

1.6. Target Specifications

The target specifications for this 4-bit ALU design using 90nm CMOS technology aim to balance performance, power efficiency, and area compactness. Key specifications include achieving a maximum operating frequency that supports basic arithmetic and logic operations with minimal delay, allowing seamless integration into low-power digital systems. The ALU should have a low power dissipation, keeping leakage currents and dynamic power within acceptable limits to meet energy efficiency requirements. Additionally, the design must be compact in layout, optimized for the 90nm node, ensuring it occupies minimal chip area while

maintaining functionality. These specifications are essential for making the ALU suitable for embedded systems, IoT applications, and educational prototypes.

1.7. Project work Schedule

Phase 1: Designing the schematic and testbench of the adder, subtractor and magnitude comparator circuit. These blocks will be simulated and checked by analysing the waveform

Phase 2: Designing the schematic and testbench of the 1's complement and decoders circuit. These blocks will be simulated and checked by analysing the waveform.

Phase 3: Combining all the blocks and making the ALU block completely. This block will be analysed by the waveform simulation.

Phase 4: Designing the layout of all the individual blocks and checking the DRC and LVS of all the blocks.

CHAPTER 2
BACKGROUND THEORY

In this chapter we will be discussing on the various works that has been presented in various journals and conferences. we will explore existing research and methodologies related to the design and implementation of Arithmetic Logic Units (ALUs) using CMOS technology, with a specific focus on 90nm process nodes. This will include a review of various ALU architectures, their design considerations, and optimization techniques for power, area, and speed. We will also examine previous works on the use of 90nm CMOS technology in digital circuit design, highlighting the advantages and challenges associated with this node. Additionally, the literature survey will cover relevant topics such as ALU performance metrics, layout strategies, and the tools used for simulation and verification, providing a comprehensive understanding of the current state of ALU design and the gap this project aims to address.

2.1 Introduction to project title

The project titled "Design and Implementation of a 4-bit ALU using 90nm CMOS Technology" focuses on developing a compact and efficient Arithmetic Logic Unit (ALU) that can perform basic arithmetic and logical operations on 4-bit binary numbers. The ALU is a critical component in digital systems, handling operations such as addition, subtraction, comparison, 1’s complement and decoding which are fundamental for any computational task in microprocessors and embedded systems. By using 90nm CMOS technology, the project aims to strike a balance between performance, power consumption, and area efficiency, leveraging the advantages of this technology node to optimize the design. This project involves not only the conceptualization and design of the ALU but also its simulation, testing, and layout using Cadence Virtuoso, making it an ideal exploration of modern digital design principles and CMOS technology.

2.2. Literature Review

2.2.1. Background theory

The Arithmetic Logic Unit (ALU) is a crucial component of any digital system, especially in processors, where it performs a wide range of arithmetic and logical operations. At its core, an ALU operates on binary numbers and supports operations such as addition, subtraction, comparison, decoding and bitwise logical operations like 1’s complement. These operations are essential for various computational tasks, from simple calculations to more complex decision-making processes in microprocessors, digital signal processors, and embedded systems. In this project, a 4-bit ALU is designed to perform basic arithmetic and logic functions, with its size limited to 4 bits for simplicity and educational purposes. The design is

based on CMOS (Complementary Metal-Oxide-Semiconductor) technology, widely used in digital integrated circuits for its efficiency, scalability, and low power consumption.

CMOS technology, specifically the 90nm node, is chosen for its ability to balance performance with power efficiency. At the 90nm scale, transistors are small enough to achieve fast switching speeds while maintaining relatively low power consumption compared to smaller nodes. This allows for a practical implementation of digital circuits that require minimal power dissipation, an essential characteristic for modern, energy-efficient devices. The design and implementation of a 4-bit ALU using 90nm CMOS involves creating the appropriate logic gates, using full adders and subtractors for arithmetic operations, and integrating them into a compact layout. The project also involves the use of EDA tools like Cadence Virtuoso for schematic design, simulation, and layout generation, ensuring the final ALU design meets functional and performance requirements while optimizing for area and power consumption.

2.2.2. Recent developments in the work area

Recent developments in the design of Arithmetic Logic Units (ALUs) and CMOS technology have focused on improving power efficiency, speed, and integration in response to the growing demand for low-power, high-performance digital systems. With the continuous scaling down of transistor sizes, new techniques in 90nm and even smaller process nodes have emerged to tackle challenges like leakage current and power dissipation, which are critical in modern electronics. Research has increasingly focused on optimizing ALU designs for specific applications, such as embedded systems and IoT devices, where power consumption is paramount. Additionally, advancements in layout optimization, including the use of advanced routing algorithms and reduced area designs, have helped further enhance the performance of ALUs while minimizing chip area. In parallel, there has been a growing interest in utilizing machine learning and AI-driven approaches to automate the design process, improving the efficiency of verification and simulation in complex digital circuits. These developments continue to push the boundaries of ALU design, contributing to the evolving landscape of digital integrated circuit technology.

2.2.3. Literature Survey

In the first paper named Design and implementation of 4-bit ALU using FINFETS for nano scale technology, the author has described about FINFET based Arithmetic Logic Unit (ALU) is developed which acts as core part of a CPU, with the arithmetic functions such as addition, subtraction, and logical functions such as AND, OR etc. The authors have told that there are several issues in the MOSFET based design such as, Gate oxide tunnelling leakage, Self

heating, Soft Error Rate, Strained-Si channel and high-K gate etc. They say that the FINFET offers distinct advantages for scaling to very short gate lengths. Fabrication of the FINFET is similar to that of the conventional CMOS process, with only minor disruptions, offering the potential for a rapid deployment to manufacturing. They have also calculated the delay and power calculation and we are getting the result as 7.83nm delay for adder and 1.74nW power consumption for the adder.

In the second paper named High Performance GDI-ALU using 10T Adder Cells, has used gate diffusion input which is a new technique that has been significant in improving the digital logic performance while incorporated in CMOS VLSI circuit design. The author has concentrated on design and execution of 4-bit CMOS gate diffusion input ALU suitable for low power and high-speed processing. The author first has done a low power 10T Full adder has been designed with GDI technique using 22nm CMOS scaling, then the design has been benchmarked with the conventional CMOS ALU and CMOS pass transistor based ALUs for substantiating the performance statistics such as power, delay and Power Delay Product. The authors have also compared the transistors count for CMOS, PTI and GDI types of designs.

In the third paper named construction of an RSFQ 4-bit ALU with half adder cells, the author constructed a rapid single flux quantum (RSFQ) 4-bit arithmetic and logic unit (ALU) in a pipelined structure. For the sake of speeding up of the circuit, the author has used a forward clocking scheme. This design consists of ten RSFQ Half Adders, 2 switches, and several D flip-flops. This design is also fabricated using the Korea Photonics Technology Institute's ten-level 1.0 kA/cm/ process. size of the ALU was 3.0 mm, 1.5 mm, fitting in a 5 mm chip. This complete design is operated correctly at up to a 5 GHz clock frequency and it worked correctly. The author has also tested the fabricated 4-bit ALU and was successfully tested at low speed for all four arithmetic and logic operations (ADD, AND, OR and XOR). They also tested the high-speed operation of the circuit by using the high-speed eye diagram technique.

In the fourth paper named Design and Evaluation of a 4-bit ALU and RAM System: A Step towards Ultra-Low Power Computing, the author presents the design and implementation of a low-power 4-bit Arithmetic Logic Unit (ALU) with a Random-Access-Memory (RAM) module on Cadence platform. The designed ALU architecture aims to address the growing demand for energy-efficient processors in modern computing systems. They have advanced low-power design techniques to optimize the ALU's static leakage power by around 66.24% while ensuring minimal performance degradation. This design uses minimum required transistors with power gating to reduce dynamic and static power dissipation. The author introduces an integrated RAM module within the ALU architecture to enhance overall data handling capabilities and minimize data access latency. The results demonstrate significant improvements in power efficiency compared to conventional ALUs without compromising on critical performance metrics.

In the fifth paper named 4-Bit Arithmetic Logic Unit (ALU) based on Neuron MOS Transistors, the author designed a 4-Bit Arithmetic Logic Unit (ALU) based on Soft-Hardware-Logic. This implementation is based on the device known as neu-MOS (ν-MOS), a floating-gate MOS transistor with more than one control gate used for the digital signal processing. The author has demonstrated that using a universal circuit, basic Boolean functions like AND, NAND, OR, NOR, Exclusive-OR and Exclusive-NOR can be configured using Multiple-Input Floating-Gate (MIFG) Transistors or neu-MOS. For this purpose, they have used a graphical method called Floating-gate Potential Diagram (FPD). During FPD a very basic 4-Bit ALU was designed and simulated for a couple of arithmetic and logic functions taking advantage of the weighted sum performed at the floating gate of the neu-MOS. The author has used Onsemi's 500nm technology for the design of the ALU.

In the sixth paper named Design and Implementation of a high speed 4bit ALU using BASYS3 FPGA Board, the author deals with the construction of Arithmetic Logic Unit (ALU) using Xilinx VIVADO 2016.2 and implement them on Field Programmable Gate Arrays (FPGAs) to analyse the design parameters. The main objective of designing this ALU is to develop algorithms in order to achieve an efficient utilization of the available hardware. The author measures efficiency of an algorithm by speed improvement, less power consumption and better utilization of ALU. This designed ALU will perform addition, subtraction, multiplication, division, AND, OR, NOT, XOR and XNOR etc. This also includes shift operations. This design has 4-bit select lines, so based on that select lines we will be selecting which operation need to be done. The author has also shown the RTL schematic of the design. The simulation was done in vivado software. The RTL codebase was written in Verilog HDL language.

In the seventh paper named Design of 4-bit ALU using TEAM Memristor Model and CMOS Logic, the author presents a modular design of Arithmetic Logic Unit based on memristor and CMOS logic. This design has been implemented using Threshold Adaptive Memristor model (TEAM). The author has given a small introduction on Memristor model and threshold adaptive memristor model. The author has also compared the total number of transistors we have used for memristor, hybrid transistors and CMOS transistors. In this comparison the author says that the transistors count for hybrid transistors is very small compared to memristors and largest transistors count is given by CMOS transistors.

In the eighth paper named A 2.319uW, 37.34 MHz Transmission Gate Based 4-Bit ALU for Contemporary Low-powered, High-Speed Microprocessors, the author makes use of the four different logic techniques, namely CMOS, dynamic, pseudo NMOS, and transmission gate, within the system. The author has done the comparative study on all the techniques and reveals that transmission gate yields the most favourable outcomes, for instance slew rate of 173.24 GV/s and propagation delay of 27.27ps on average. The design has achieved a staggering 2.319μW static power and a silicon area of 537 um^2. The design has proven to be

best for the popular Arm Cortex A7, a low powered microprocessor, whose total power dissipation is less than 100μW. They have compared various parameters such as slew rate, propagation power, static power, power delay product, rise time, fall time, fan in etc.

In the ninth paper named Design and Implementation of ALU Using Ring Counters, the author is designing an ALU using 8-bit Programmable Ring counter, that is a combination of straight and twisted ring counters. The design accepts two 4-bit binary numbers, perform ALU operations and results the output. The author compares the performance of ALU between Ring counters in terms of various aspects. This ALU performs several arithmetic and logical operations on two 4-bit values, that includes addition, subtraction, logical AND, OR, XNOR, left shift and right shift. The design result is based on the values of the select lines received from the Ring Counters, multiple ALU outputs are possible. The processor's ALU is implemented using Xilinx software, namely the integrated simulator in Xilinx ISE Design Suite 14.2. The author compared the different ALU and checking what is the delay of the different ALU and for the completion of the execution. They have also checked the path delay for different designs.

In the tenth paper named Pipeline Architecture for N=K*2L Bit Modular ALU: Case Study between Current Generation Computing and Vedic Computing, the author performs mathematical operations using Vedic sutra for upward compatibility in pipeline manner. They also describe the design architecture for this performance. The author has increased the area, performance and reduced power, Vedic architecture have observed to be inherently compatible with higher efficiency for pipeline architecture. The author says that the generalized N-bit ALU, can always be realized using pipeline modular architecture. The authors have extensively verified modular architecture for 4-Bit modules for 16 bit and 32-bit pipelined operations. The MAC unit which involves multiplication algorithms used in FFT and IFFT using sutras of Vedic mathematics and it is possible to achieve reduce version in-terms of speed and delay, compared to different generations of ALU.

2.3. Summarized outcome of the Literature Survey

The literature survey reveals several advancements in the design and optimization of 4-bit ALUs, each addressing different challenges in terms of power consumption, speed, and efficiency. The papers reviewed showcase a variety of techniques, including the use of FINFETs for scalability in nano-scale technologies, Gate Diffusion Input (GDI) for low-power and high-speed operations, and RSFQ for high-speed, low-power designs. Moreover, the integration of advanced logic techniques such as memristor-based designs and neu-MOS transistors highlights innovations for enhancing ALU functionality and efficiency. Other studies focus on reducing power dissipation with low-power CMOS designs, the use of transmission gates for improved performance, and the development of ALUs for specific

applications such as low-power microprocessors and high-speed computing. These advancements underscore the ongoing efforts to improve ALU designs for various computing needs, from embedded systems to high-performance processors, and provide valuable insights into potential strategies and tools for the current project**.**

2.4. Theoretical discussions and general analysis

In the theoretical discussion and general analysis of the 4-bit ALU design, the focus is on understanding the underlying principles of ALU functionality and the design choices that influence its performance. The ALU is constructed using basic logic gates (AND, OR, XOR) and arithmetic components such as adders and subtractors to perform various operations. At the core of the design lies the ability to process binary inputs and produce corresponding outputs based on the selected operation, which is controlled by select lines. A key aspect of the ALU design is the trade-off between speed, power consumption, and area. For instance, optimizing gate delays and minimizing power dissipation are critical for achieving efficient performance, especially when working with CMOS technology, where leakage currents and switching speeds play a significant role. The analysis also considers layout optimization, where techniques like reducing parasitic capacitances and ensuring efficient routing contribute to lowering power consumption while maintaining fast operation. Furthermore, the comparison of different ALU implementations, as seen in the literature, helps identify the best practices for achieving a balanced design, considering factors like power delay product, transistor count, and functional correctness. This analysis forms the foundation for improving the 4-bit ALU design in terms of both theoretical understanding and practical implementation.

2.5. Conclusions

This chapter concludes that significant progress has been made in the design and optimization of 4-bit ALUs, with various techniques being explored to enhance performance, reduce power consumption, and improve scalability. Different design approaches, such as using FINFETs, GDI, RSFQ, and memristor-based technologies, offer distinct advantages for specific applications, from high-speed computing to low-power systems. The analysis of these studies reveals the ongoing challenges and opportunities in balancing speed, power, and area, particularly in advanced CMOS nodes. By understanding these advancements, the current project can build upon established methodologies and incorporate optimized strategies for designing an efficient 4-bit ALU in 90nm CMOS technology. This chapter highlights the diverse approaches and serves as a foundation for the design decisions made in this project.

CHAPTER 3
METHODOLOGY

3.1 Introduction

In the methodology chapter, the design and implementation process of the 4-bit ALU using 90nm CMOS technology will be discussed in detail. This chapter will outline the step-by-step approach taken, starting from the conceptualization of the ALU architecture to the final layout generation. The key components, such as the arithmetic and logical units, full adders, and multiplexers, will be described along with the logic behind their design. The methodology will also cover the tools and software used, including Cadence Virtuoso for schematic design, simulation, and layout optimization. Furthermore, the chapter will discuss the considerations made for power efficiency, speed optimization, and area minimization, along with the simulation and validation techniques employed to verify the functionality and performance of the ALU.

3.2 Methodology

3.2.1 Detailed methodology

In this project, the methodology for designing the 4-bit adder, 4-bit subtractor, 4-bit magnitude comparator, 3:8 decoder and 4-bit 1's complement was based on 90nm CMOS technology using Cadence Virtuoso. The first step involved creating the schematics for each of the components. For the 4-bit adder and subtractor, full adders and subtractors were designed using CMOS logic gates, ensuring that both operations could handle 4-bit inputs and produce accurate sum and difference outputs. The 4-bit magnitude comparator was designed to compare two 4-bit inputs and generate the corresponding output based on equality, greater than, or less than conditions. The 3:8 bit decoder will decode the input 3-bit and give the 8-bit output. The 4-bit 1's complement will invert the input 2 4-bit and give 2 4-bit as output. After the schematic design, the next step was to create the corresponding test benches for all five blocks. These test benches were constructed to validate the functionality of the blocks under various input conditions, simulating both normal and edge cases.

Following the schematic and test bench creation, the waveform analysis was performed using Cadence Virtuoso's simulation tools. The simulation allowed for observing the behaviour of the designed circuits under different input combinations and ensured that the outputs met the expected results. By analysing the waveforms, any discrepancies in the operation, such as incorrect outputs or timing issues, could be identified and rectified. The simulation results confirmed the correct functionality of the 4-bit adder, subtractor, magnitude comparator, 1's complement and decoder. This process of schematic design, test bench creation, and waveform

analysis ensured the reliability and correctness of the individual blocks, laying a solid foundation for their integration into a larger ALU design.

3.2.2. Circuit design and layout

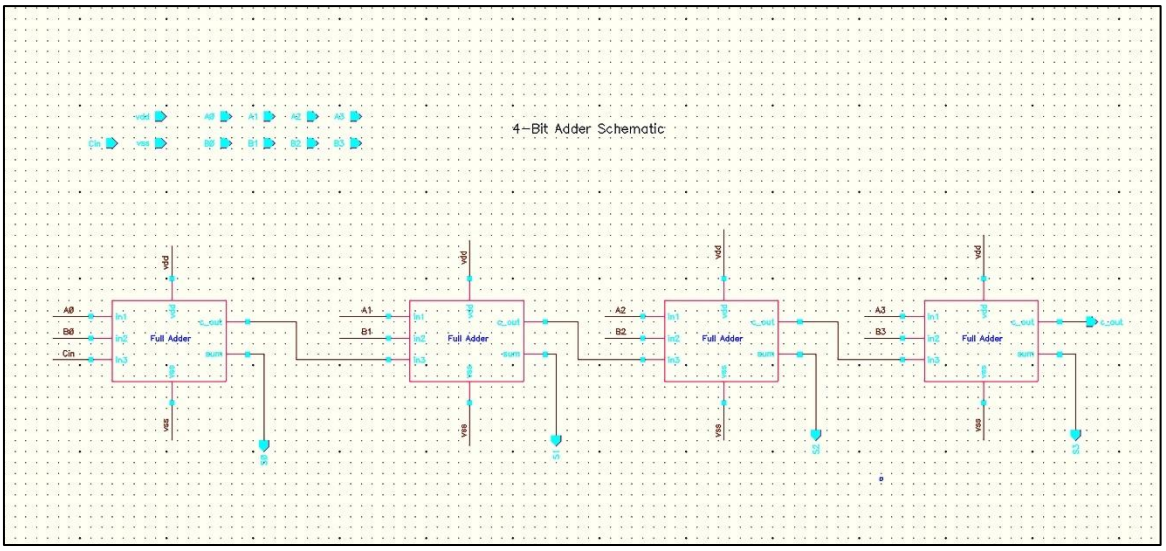

Fig3.2.1 Schematic of the Full adder

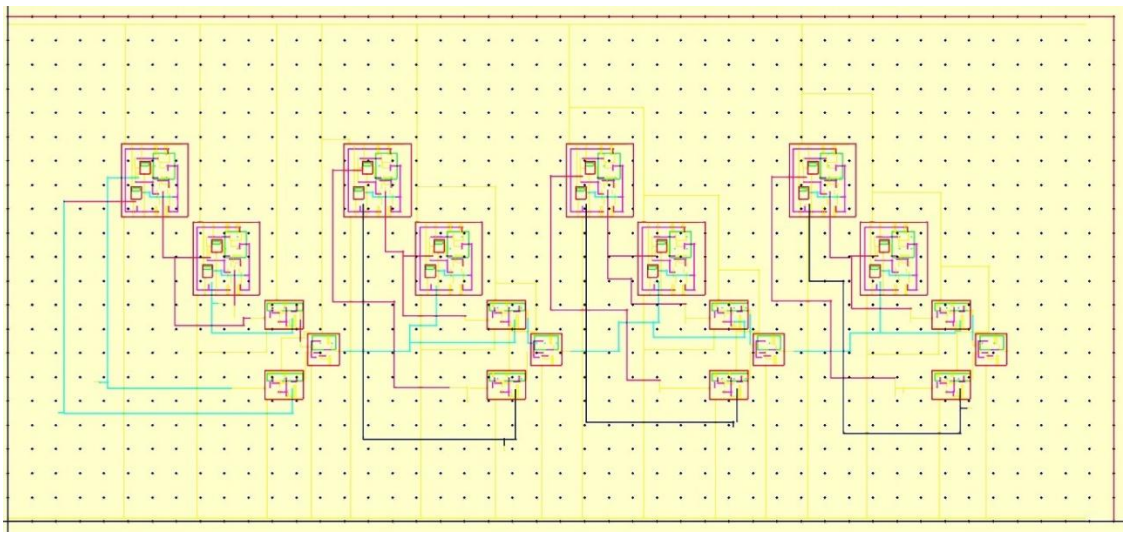

Fig3.2.2 Layout of the Full adder

The image above shows the schematic diagram and layout of a 4-bit full adder implemented using 90nm CMOS technology. This full adder takes three inputs: A, B, and Carry-in (Cin), and produces two outputs: Sum and Carry-out (Cout). The design utilizes basic CMOS logic gates, including NAND, NOR, and XOR gates, to achieve the desired arithmetic functionality. The full adder's role is to perform the addition of two binary bits along with a carry-in bit, generating a sum and a carry-out bit. The schematic demonstrates the integration of these logic gates, ensuring that the full adder functions correctly within the larger 4-bit adder block. The use of CMOS technology ensures low power consumption and high-speed performance, crucial for efficient digital circuit design.

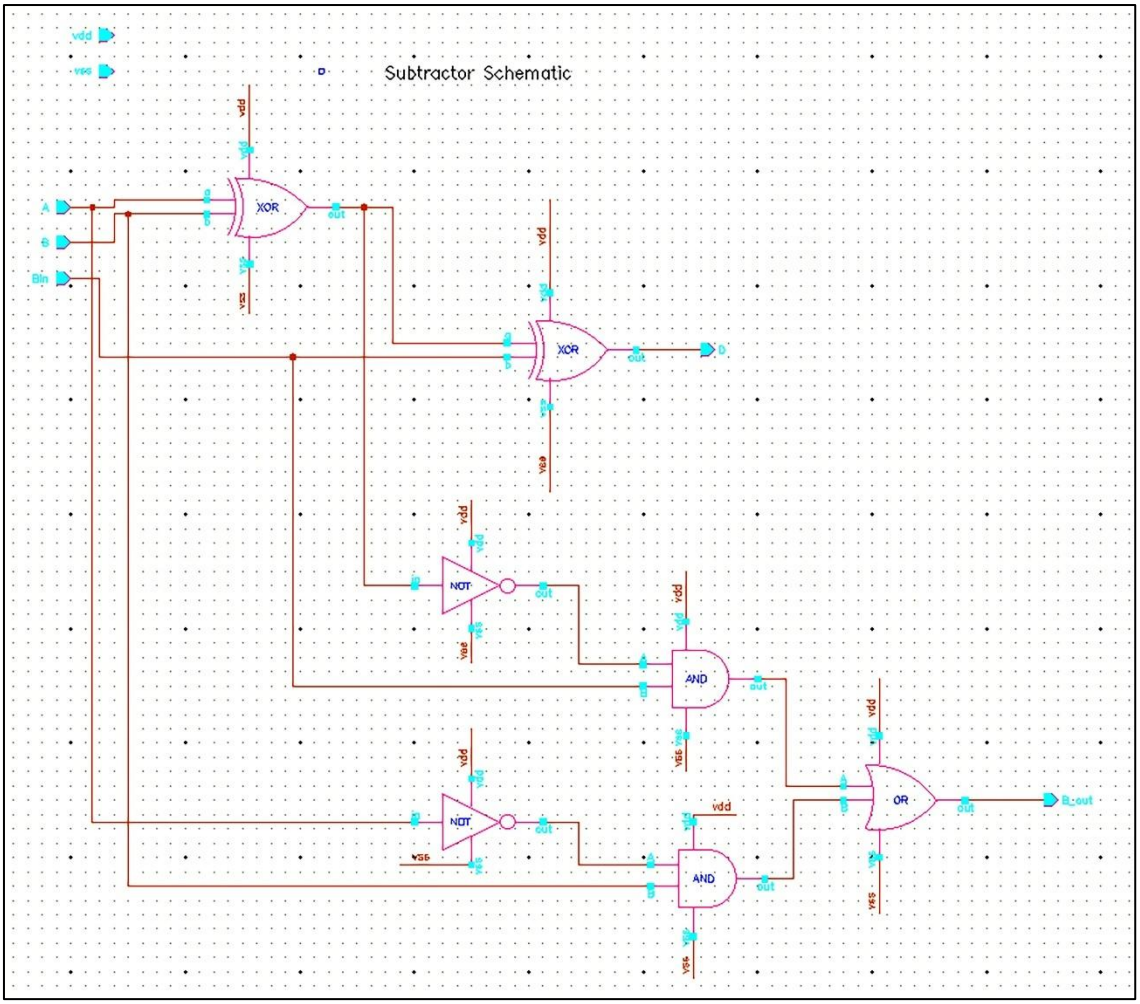

Fig 3.2.3 Schematic of the subtractor

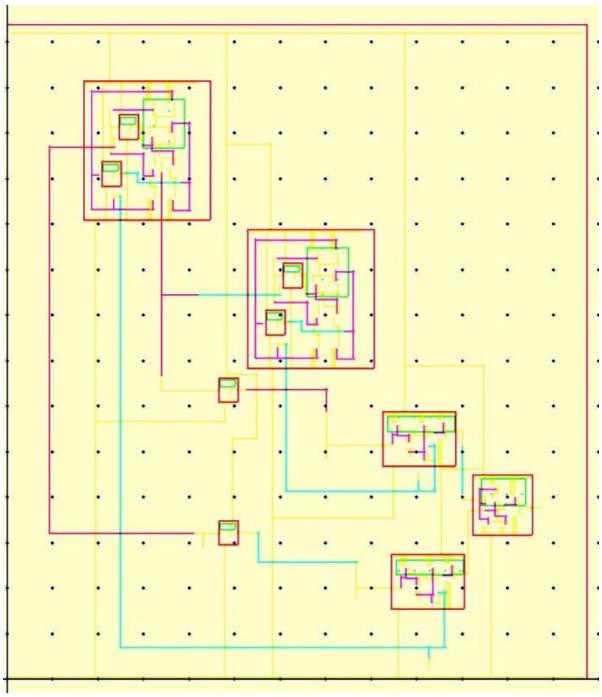

Fig 3.2.4 layout of the subtractor

The image above shows the schematic diagram and layout design of the 4-bit subtractor designed using 90nm CMOS technology. This subtractor is responsible for performing the subtraction operation on two 4-bit binary numbers. It takes two inputs: A and B, along with a Borrow-in (Bin) input, and produces two outputs: Difference and Borrow-out (Bout). The design is based on CMOS logic gates, including XOR, AND, and OR gates, to implement the subtraction operation. The subtractor works by applying the 2's complement method for binary subtraction, where the Borrow-in represents the carry-over from previous bits. The schematic illustrates how these gates are connected to achieve the correct difference and borrow outputs for all possible input combinations. The CMOS-based design ensures low power consumption and high-speed operation, making it suitable for efficient digital processing in the 4-bit ALU.

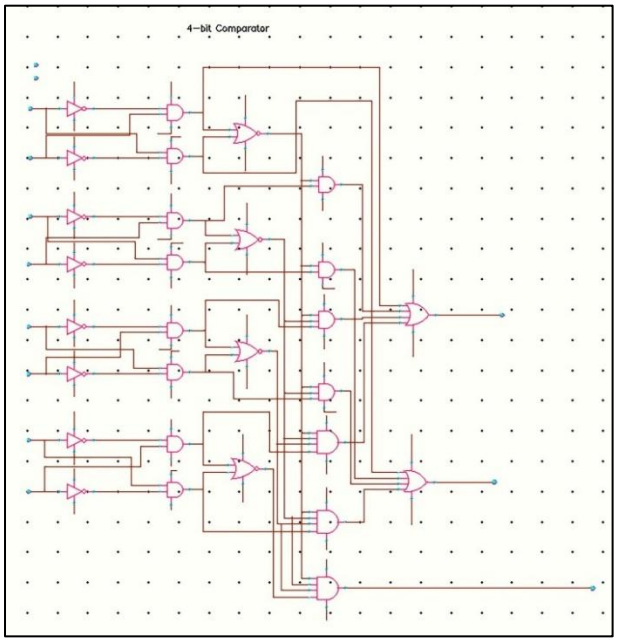

Fig 3.2.5. Schematic of the 4-bit magnitude comparator

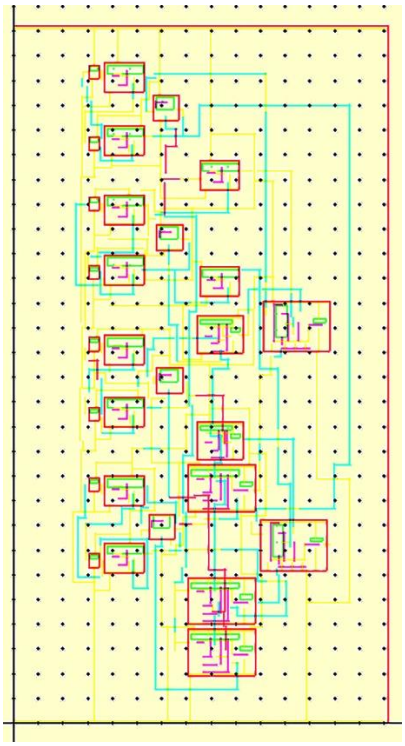

Fig 3.2.6. layout of the 4-bit magnitude comparator

The image above illustrates the schematic diagram of the 4-bit magnitude comparator designed using 90nm CMOS technology. This comparator takes two 4-bit inputs, A and B, and compares their values to determine whether A is greater than, less than, or equal to B. The circuit is implemented using basic CMOS logic gates such as AND, OR, and NOT gates, which are arranged to produce three output signals: A > B, A < B, and A = B. These outputs indicate the result of the comparison between the two 4-bit inputs. The schematic showcases how these gates are interconnected to perform the magnitude comparison efficiently. This design ensures accurate and reliable comparison of binary numbers, which is a key component in various arithmetic and logical operations within the 4-bit ALU.

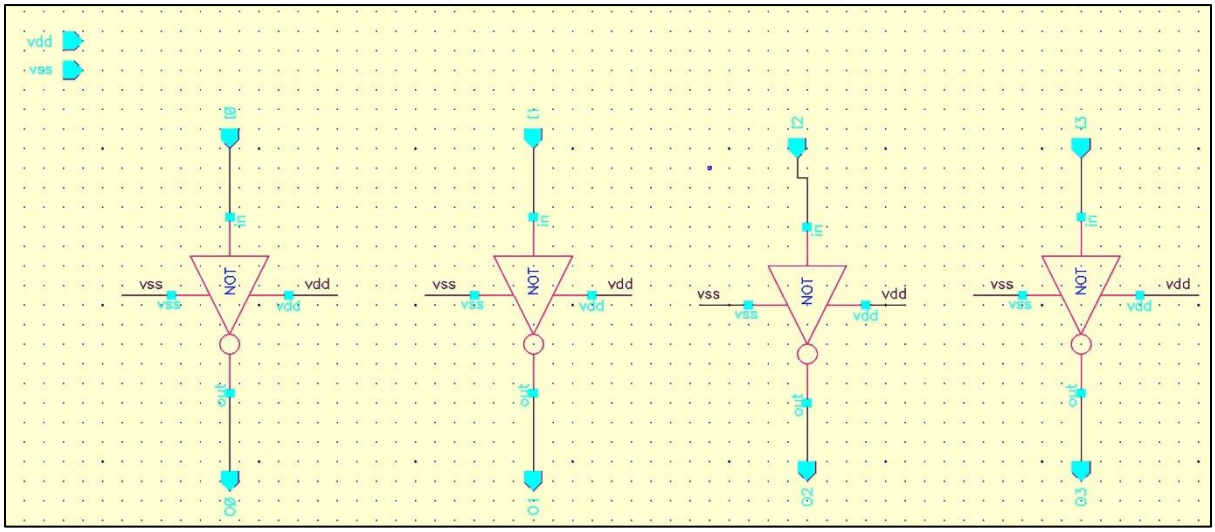

Fig 3.2.7. Schematic of the 4-bit one's complement

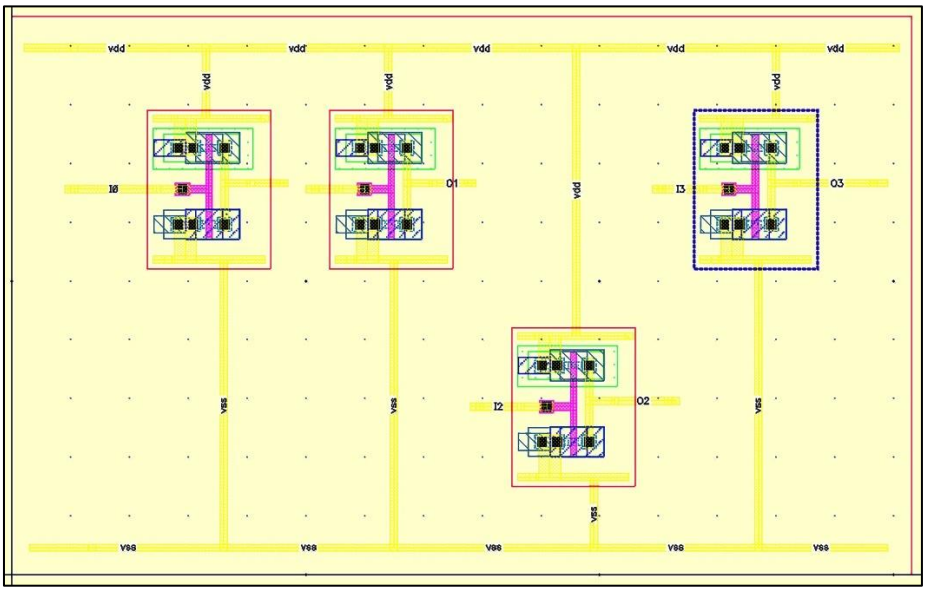

Fig 3.2.8. layout of the 4-bit one's complement

The image above is a schematic design and layout of a 4-bit One's Complement circuit using four inverters. The design consists of a simple yet effective implementation where each bit of the 4-bit input is inverted using a dedicated CMOS inverter to generate its complement. The schematic was created using 90nm CMOS technology, ensuring optimized performance and minimal power consumption. After designing the circuit, a testbench was developed to verify its functionality through transient analysis, confirming that each input bit correctly flips to its complement. The simulation results validate the expected behaviour, demonstrating the feasibility of this approach for basic arithmetic and logical operations in digital circuits.

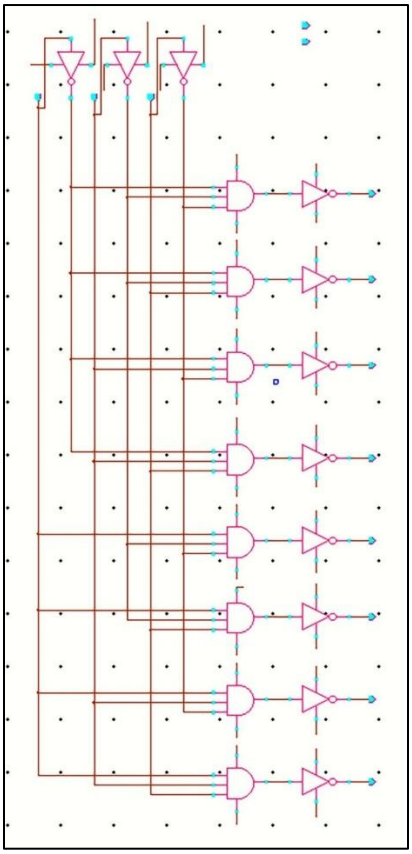

Fig 3.2.9. Schematic of the 3:8 decoder

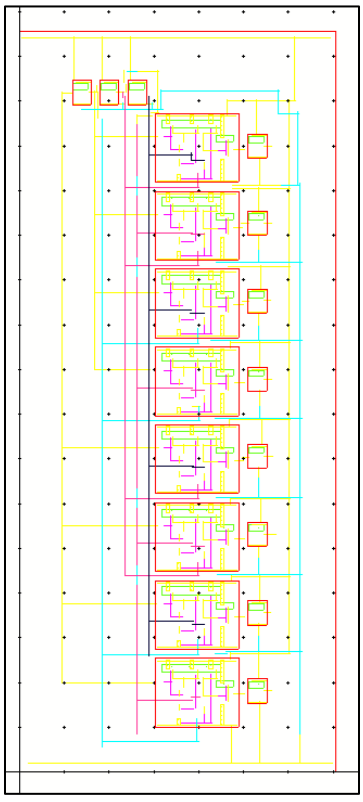

Fig 3.2.10. layout of the 3:8 decoder

The image above is schematic diagram of a 3-to-8 decoder using logic gates in Cadence Virtuoso. The circuit takes a 3-bit binary input and generates eight unique output lines, where each output corresponds to one of the possible input combinations. The design was implemented using AND and NOT gates, ensuring correct decoding logic while maintaining minimal propagation delay. The schematic was developed using 90nm CMOS technology, optimizing power and area efficiency. A testbench was created to verify the functionality through transient analysis, confirming that each output line is activated exclusively based on the input combination. The simulation results validate the expected operation, making this design suitable for applications in memory address decoding and control logic circuits.

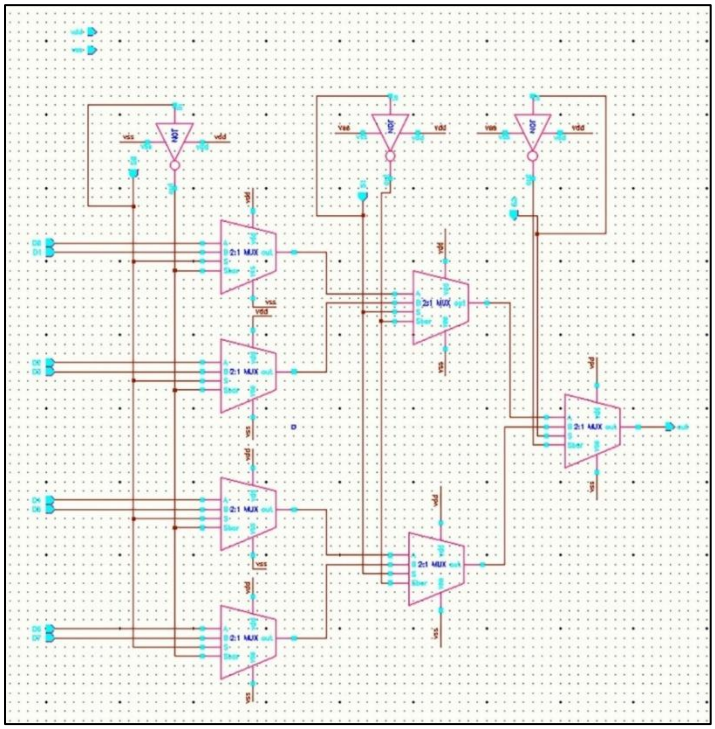

Fig 3.2.11. Schematic of the 8:1 Mux

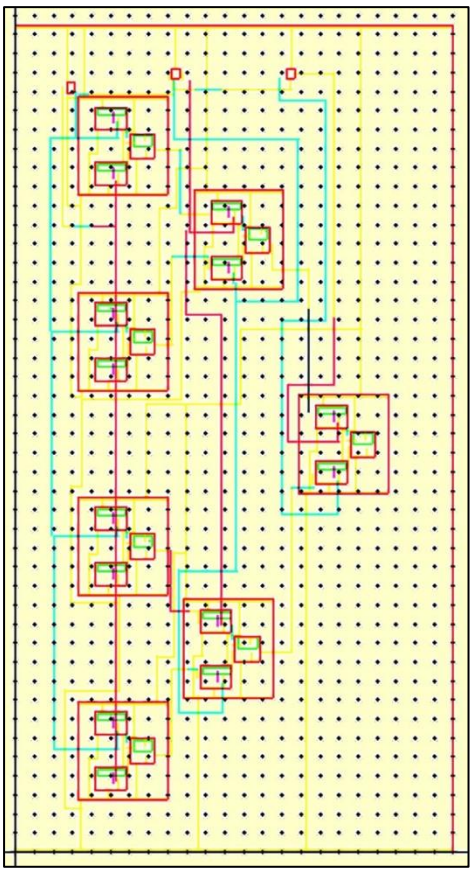

Fig 3.2.12. Layout of the 8:1 Mux

The image about is the schematic diagram and layout of an 8:1 multiplexer (MUX) using seven 2:1 multiplexer in Cadence Virtuoso. The hierarchical design follows a tree-like structure, where the first stage consists of four 2:1 MUX selecting between input signals, the second stage has two 2:1 MUX selecting between the first stage outputs, and the final stage uses one 2:1 MUX to produce the final selected output based on the 3-bit select lines. The design was implemented using 90nm CMOS technology, ensuring efficient switching performance with minimal delay. The simulation results validate the expected behaviour, demonstrating the reliability of this design for digital signal selection and data routing applications.

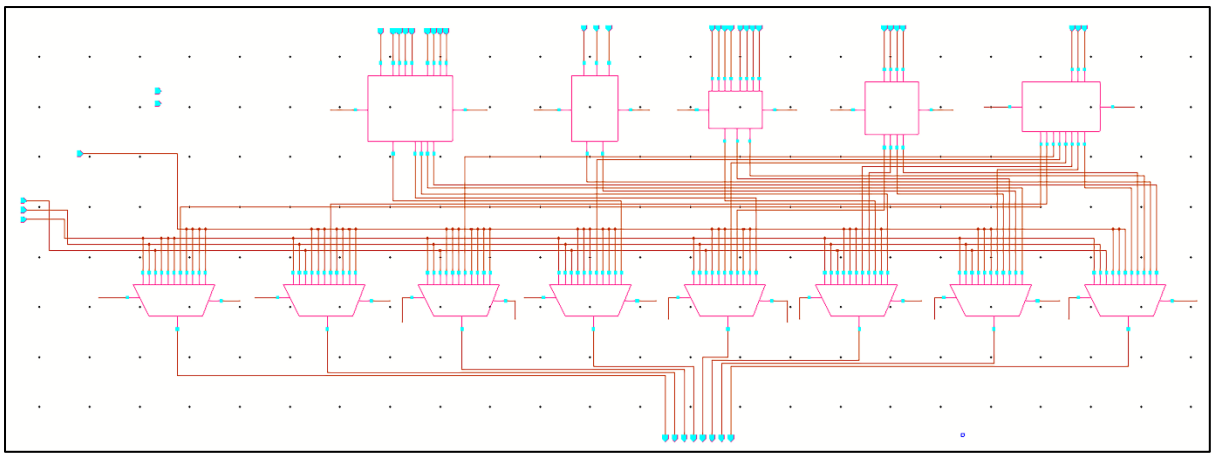

Fig 3.2.13. Schematic of the 4-bit ALU

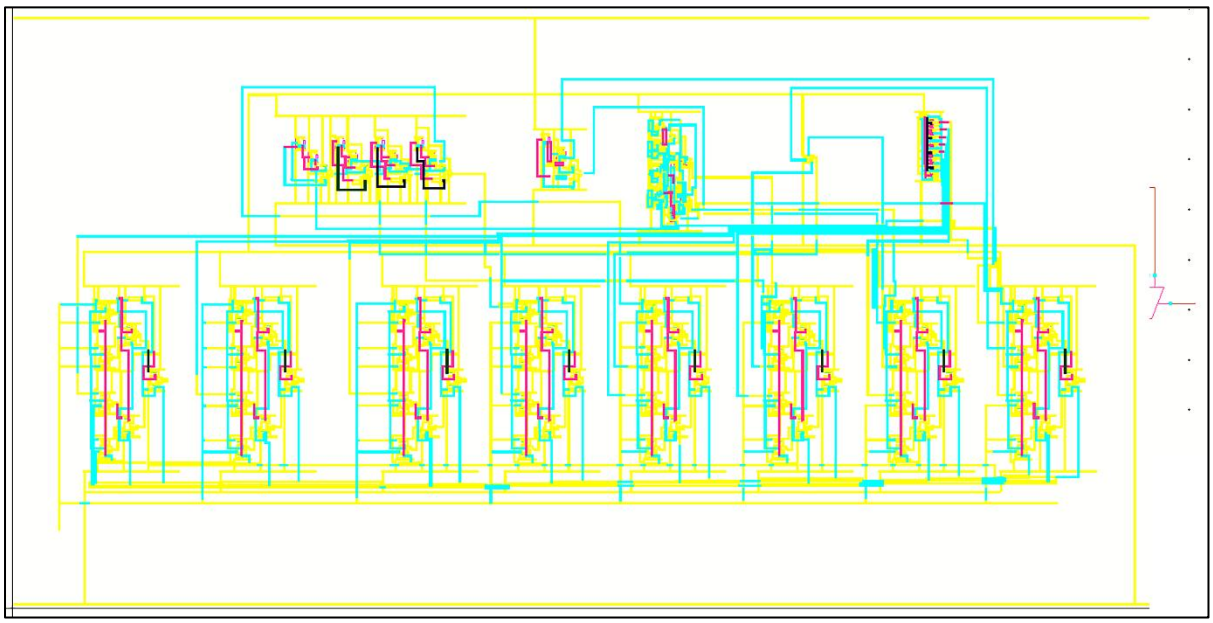

Fig 3.2.14. layout of the 4-bit ALU

The above images show the schematic diagram and layout design of a 4-bit Arithmetic Logic Unit (ALU) in Cadence Virtuoso, implementing basic arithmetic and logical operations. The ALU takes two 4-bit operands and a set of control signals to perform operations such as addition, subtraction, magnitude comparison, ones complement and 3:8 decoder. The design was implemented using 90nm CMOS technology, ensuring optimized performance in terms of speed and power consumption. The design includes 8 8:1 mux for the control of all output. The simulation results validate the expected behaviour, demonstrating the efficiency and accuracy of this ALU for fundamental computing tasks in digital processing applications.

3.3. Tool used

Cadence Virtuoso is the primary tool used in this project for designing, simulating, and verifying the functionality of the 4-bit adder, subtractor, magnitude comparator, one’s complement and 3:8-bit decoder circuits. It is a comprehensive suite of software tools used for custom IC design, offering a range of features for schematic capture, layout design, simulation, and verification. Virtuoso's analog and mixed-signal simulation capabilities, particularly its integration with Spectre and other simulators, enable detailed waveform analysis of the circuit behaviour under various input conditions. The tool also supports advanced design capabilities for 90nm CMOS technology, allowing for accurate device modelling, layout optimization, and extraction of performance parameters such as delay, power consumption, and area. Cadence's extensive reference data sheets and documentation provide valuable insights into the design process, offering detailed information on simulation models, technology libraries, and recommended design practices, which were instrumental in successfully completing the project.

3.4. Conclusion

In conclusion, the methodology adopted for designing and verifying the 4-bit adder, subtractor, magnitude comparator, one’s complement and 3:8-bit decoder circuits using 90nm CMOS technology proved to be effective and efficient. The design process, starting with schematic creation and followed by testbench development, ensured that each block operated correctly under various input conditions. The use of Cadence Virtuoso for simulation and waveform analysis allowed for detailed examination of the circuit behaviour, enabling the identification and correction of any potential issues. Through this systematic approach, the functionality and performance of all three blocks were thoroughly validated, ensuring their readiness for integration into a larger ALU design. The methodology emphasized accuracy, efficiency, and reliability, forming a solid foundation for further advancements in digital circuit design.

CHAPTER 4
RESULT ANALYSIS

4.1 Introduction

In the results analysis chapter, we will discuss the outcomes of the simulation and performance analysis conducted for the 4-bit adder, subtractor, magnitude comparator, 4-bit 1's complement and 3:8 decoder circuits designed using 90nm CMOS technology. The chapter will focus on the waveform analysis results obtained from Cadence Virtuoso simulations, highlighting the accuracy of the circuit outputs under various test conditions. We will also see the results of verification of the layout design of the 4-bit ALU. Finally, the integration of the individual blocks into the overall ALU design and their performance in the complete system will be discussed.

4.2. Result Analysis

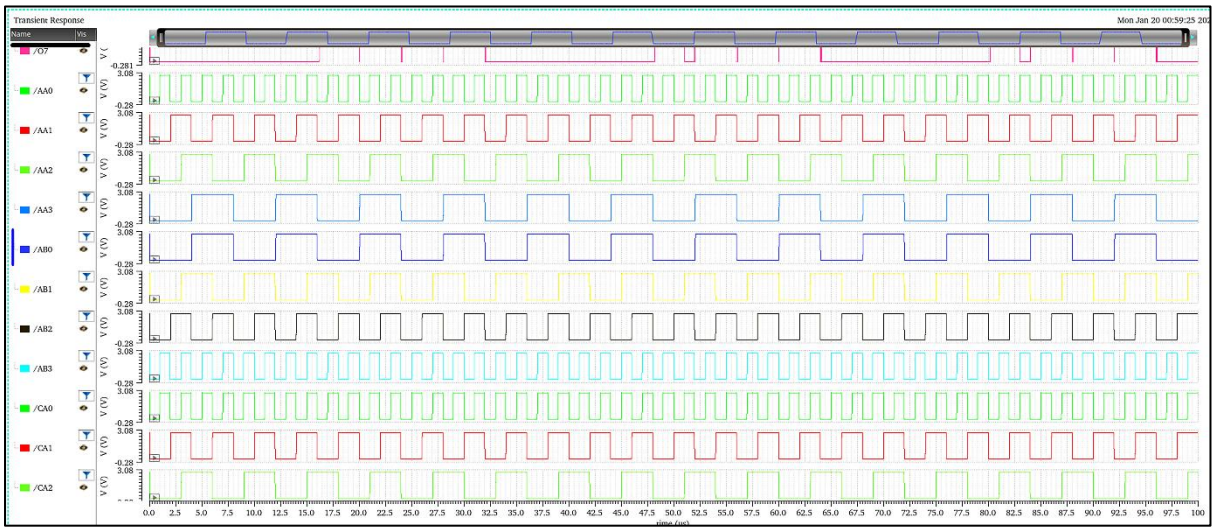

Fig 4.2.1. input waveforms for adder and comparator

In the above image we can see the input waveforms of the adder block and magnitude comparator blocks. We have used square wave of different frequencies as digital input values. As we can see in the above waveform logic low voltage is equal to 0.28V and logic high voltage is equal to 3.08V. When we say adder, it will be having 2 input and each input should be having 4-bit values. So now in the above waveform AA0, AA1, AA2, AA3 are the 4-bit values of input A and similarly AB0, AB1, AB2, AB3 are the 4-bit values of input B to the adder. Now for magnitude comparator also we need 2 inputs A and B for comparing the values. These 2 inputs are of 4-bit each. The input values CA0, CA1, CA2 are the 3-bit of input A, remaining inputs are seen in next image.

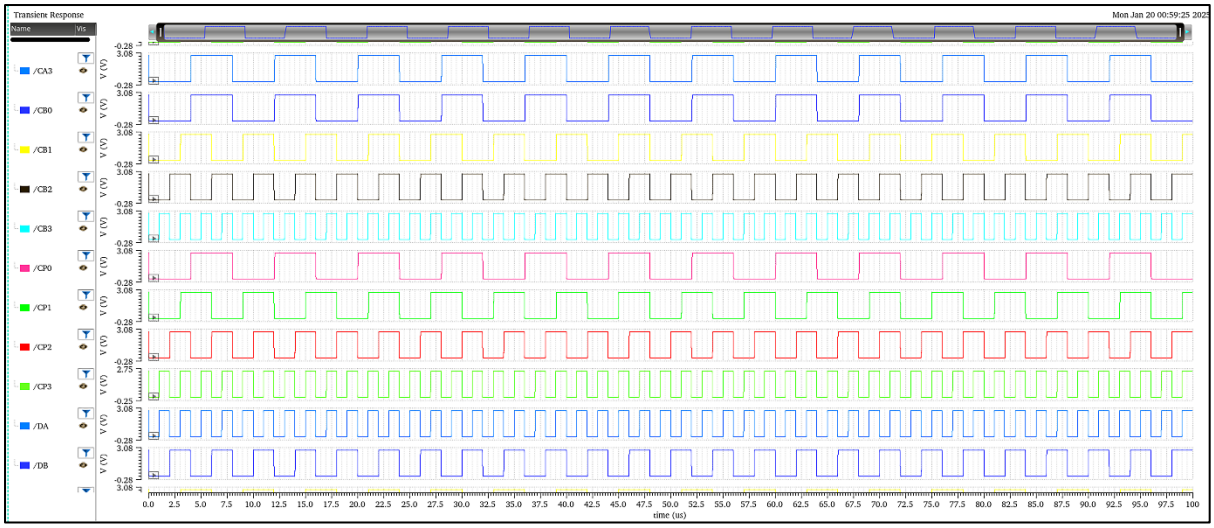

Fig 4.2.2. input waveforms for one's complement

In the above image we can see the input waveforms of the magnitude comparator block and one's complement block. Here also we have used square wave of different frequencies as digital input values. As we can see in the above waveform logic low voltage is equal to 0.28V and logic high voltage is equal to 3.08V. For magnitude comparator we need 2 inputs A and B for comparing the values. These 2 inputs are of 4-bit each. The input values CA3 is the 3rd bit of the input A and CB0, CB1, CB2, CB3 are the 4-bits of the input B. Now for the one's complement input we need 4 inputs so in the above image CP0, CP1, CP2, CP3 are the 4-bit input values of one's complement block.

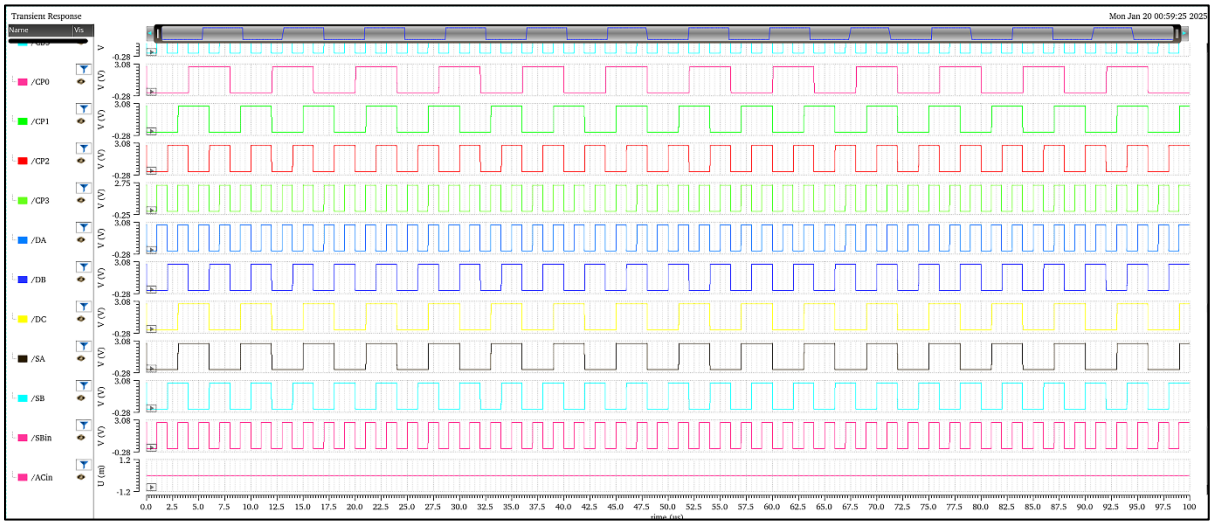

Fig 4.2.3. input waveforms for subtractor and decoder

In the above image we can see the input waveforms of the 3:8 decoder block and subtractor block. Here also we have used square wave of different frequencies as digital input values. As we can see in the above waveform logic low voltage is equal to 0.28V and logic high voltage is equal to 3.08V. For the 3:8 decoder we need 3 inputs, the input waveforms DA, DB and DC

are the 3 input waveforms of the decoder. For subtractor we need 2 inputs and 1 borrow input, the input waveforms SA, SB and SBin are the 3 inputs of the subtractor.

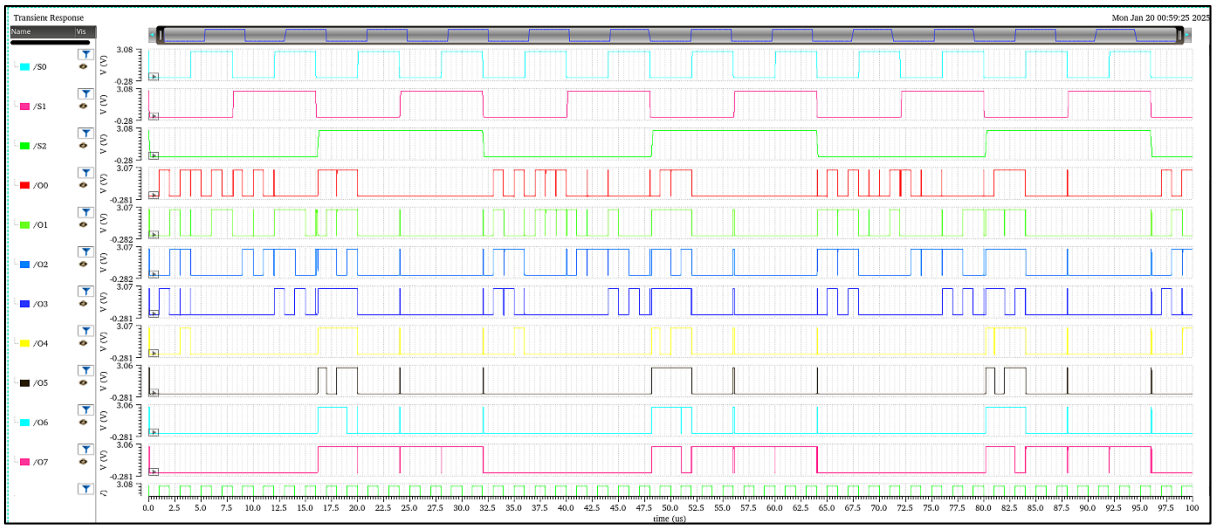

Fig 4.2.4. 8-bit output waveforms based on select line input

In the above image we can see the output waveforms based on the select lines. As we can see in the above output waveforms logic high voltage is 3.06V and logic low voltage is 0.28V. The input waveforms S0, S1, S2 are the 3 select lines of the 8:1 MUX. Based on the select line input the output will be selected for 5 different blocks. The output waveforms O0, O1, O2, O3, O4, O5, O6, O7 are the 8-bit output values.

Select line value	Output value
000	Adder
001	Subtractor
010	Magnitude comparator
011	1’s complement
100	3:8 decoder

Table 4.0.1. output selected based on the input select line values

The table above shows us the output 8-bit is selected from which block among the adder, subtractor, magnitude comparator, 1’s complement and 3:8 decoder. Since we have used 8:1 MUX for the output control, this MUX has 3-bit select lines. Suppose if the select lines are 000 then the output value is taken from the adder output. If the output value is of only 4-bit then the 8-bit output value will be having remaining bits as zero. Since we have 5 blocks of functionality the maximum select line input bit values is till 100, above that value the select line input is not valid.

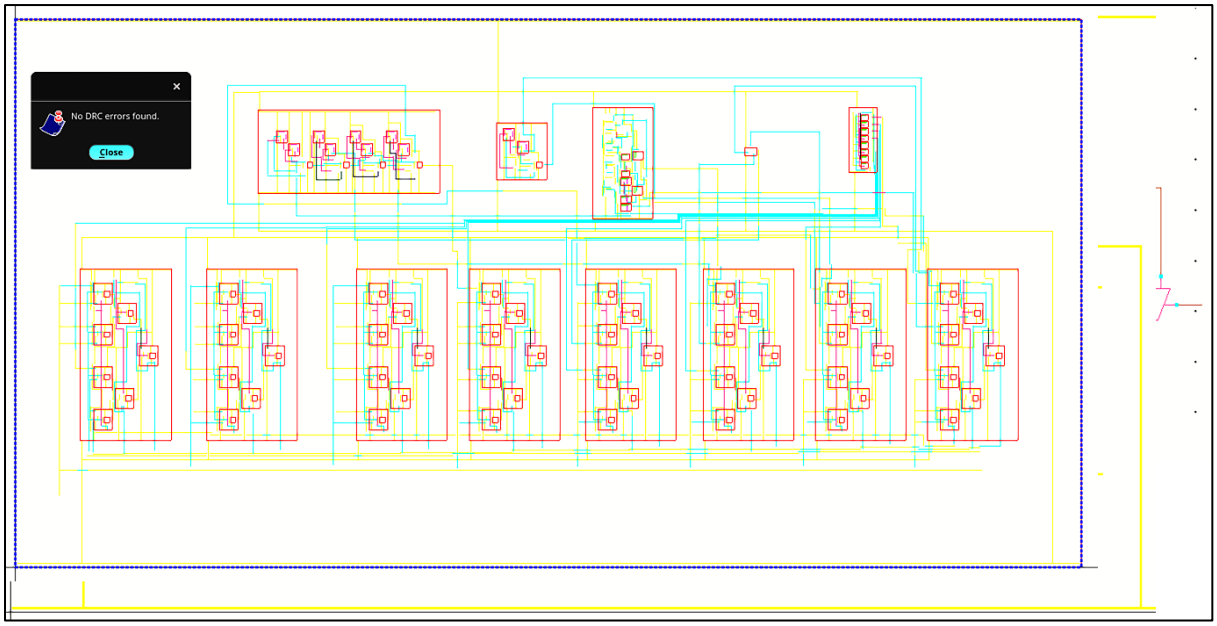

Fig 4.2.5. DRC verification of the 4-bit ALU design

The above image shows DRC (design rule check) verification of the 4-bit ALU layout design. This is a type of verification where the software checks all the wire's connections is proper or not, all cell connections are proper or not, whether via's are connected properly or not etc. Since we have designed this ALU in 90nm CMOS process, for 90nm we will be having unique design rules checks to verify. For our design all the DRC errors have been checked and validated as we can see in the image.

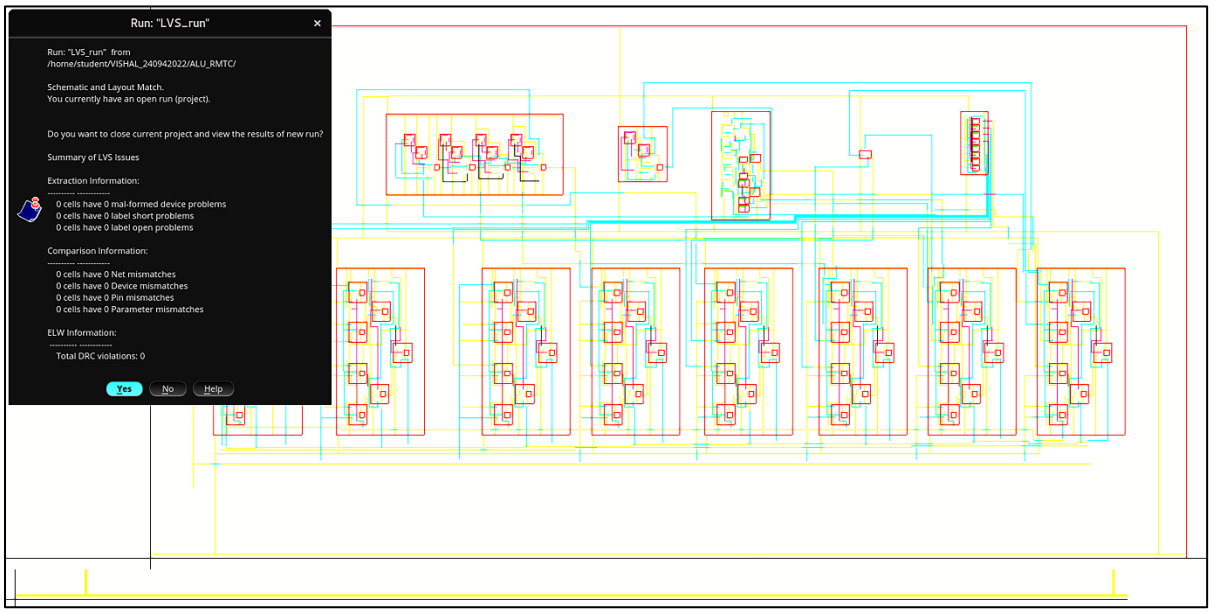

Fig 4.2.6. LVS verification of the 4-bit ALU design

The above image shows the LVS (layout vs schematic) verification for the ALU design. This LVS verification basically means that the layout which we have designed should match with

the schematic design which we have designed. It basically checks all the nets have been connected in the similar fashion as the schematic design or not. If any of the nets is missing or mismatch is happened then it will show as error which needs to be verified. For our ALU design we can see that the layout is matching with schematic and LVS test is being verified.

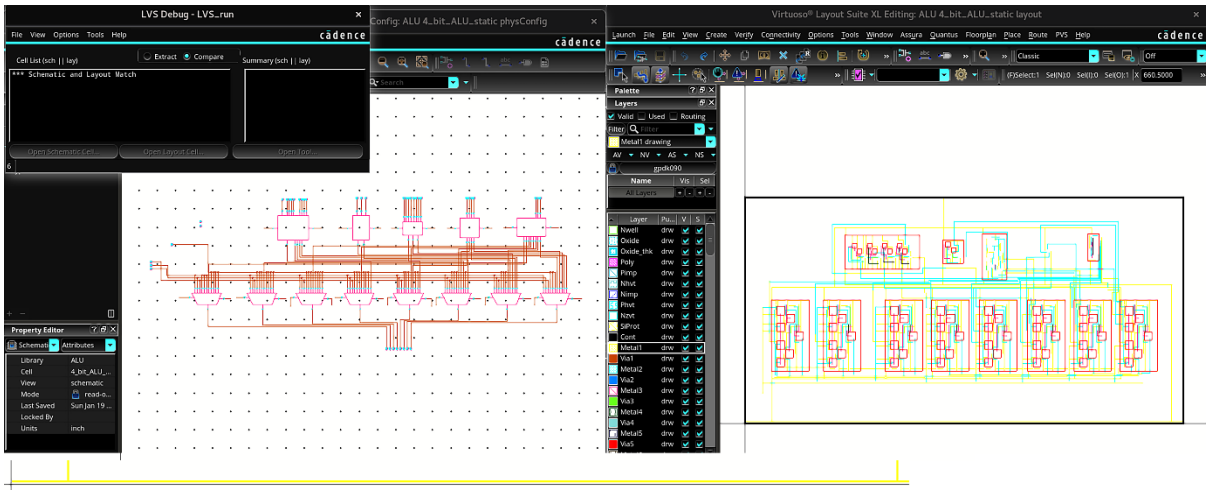

Fig 4.2.7. schematic and layout design match verification of the 4-bit ALU design

The above image shows the schematic and layout match of the ALU design. As we can see since we have DRC and LVS matches, there is a schematic and layout match as shown above. This is an important step for the design process.

4.3. Significance of the results obtained

The results obtained from the design and implementation of the 4-bit ALU demonstrate the successful integration of multiple functional blocks, including an adder, subtractor, magnitude comparator, one's complement circuit, and a 3:8 decoder. The schematic design was carefully developed and simulated in Cadence Virtuoso, ensuring that each block performed its intended operations correctly. Furthermore, the layout design was completed and verified through Design Rule Checking (DRC) and Layout Versus Schematic (LVS) verification, confirming that the physical layout adheres to fabrication constraints and accurately represents the intended circuit functionality. The simulation results validate the correctness of the ALU's operations, with each block producing the expected outputs, reinforcing the reliability and efficiency of the design. The successful completion of DRC and LVS ensures that the ALU is manufacturable, making this project a strong foundation for further optimization and implementation in digital processing applications.

4.4. Conclusions

In conclusion, the results of the 4-bit ALU design confirm the successful implementation of its five key functional blocks: adder, subtractor, magnitude comparator, one's complement, and 3:8 decoder. The schematic simulations verified the correct operation of each module, demonstrating accurate arithmetic and logical processing. Additionally, the layout design was completed and rigorously tested through DRC (Design Rule Check) and LVS (Layout Versus Schematic) verification, ensuring that the layout adheres to fabrication constraints and matches the intended circuit design. The results validate the functionality, correctness, and manufacturability of the ALU, proving its effectiveness for digital computation tasks. This project serves as a strong foundation for further optimization in terms of power, area, and performance, making it suitable for integration into larger digital systems.

CHAPTER 5
CONCLUSION AND FUTURE SCOPE OF WORK

5.1. Brief Summary of the work

In this project, a 4-bit Arithmetic Logic Unit (ALU) was designed and implemented using 90nm CMOS technology. This project focused on the design and implementation of a 4-bit Arithmetic Logic Unit (ALU) using Cadence Virtuoso. The ALU consists of five key functional blocks: adder, subtractor, magnitude comparator, one's complement circuit, and a 3:8 decoder, each designed at the schematic level and verified through simulation. Following the schematic design, the physical layout was created, ensuring proper transistor placement and interconnections. The layout was then validated using Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification, ensuring compliance with fabrication constraints and design accuracy. The successful completion of this project demonstrates a practical approach to digital circuit design and verification, providing insights into the integration of arithmetic and logical operations within an ALU structure.

5.2. Conclusions:

In conclusion, the successful design and implementation of a 4-bit Arithmetic Logic Unit (ALU) in Cadence Virtuoso demonstrate the practical integration of fundamental arithmetic and logical operations in digital circuit design. The project involved designing and verifying key functional blocks, including an adder, subtractor, magnitude comparator, one's complement circuit, and a 3:8 decoder, at both the schematic and layout levels. The transient simulations confirmed the correctness of the circuit operations, while DRC and LVS verification ensured that the layout adhered to fabrication constraints and matched the intended schematic. This project not only strengthened the understanding of CMOS-based digital design but also provided hands-on experience in VLSI implementation and verification techniques. The results validate the ALU's functionality, accuracy, and manufacturability, making it a strong foundation for further optimization and integration into larger computing systems.

5.3. Future scope of the work:

The future scope of the 4-bit ALU design extends beyond its current implementation, offering opportunities for significant advancements. One key area is the scaling of the ALU to higher bit-widths, which would enhance its applicability in more complex systems, such as processors in embedded or high-performance computing. Additionally, exploring power optimization techniques, such as DVFS or MTCMOS, can lead to more energy-efficient designs, a crucial factor in today's demand for low-power devices. The incorporation of advanced circuit technologies like FINFETs can help address the growing need for higher performance while

maintaining low power consumption, especially as semiconductor nodes shrink. Furthermore, integrating the ALU with memory and control units could support more sophisticated operations and multi-cycle execution, improving overall system efficiency. Lastly, testing the design on FPGAs would allow for real-world validation, providing valuable insights for further refinement and broader applications in digital systems.

- Scaling to Higher Bit-widths: The current 4-bit ALU design can be expanded to support 8-bit, 16-bit, or 32-bit data widths to meet the processing requirements of modern computational systems.
- Power Optimization Techniques: Future work could explore advanced power optimization techniques such as Dynamic Voltage and Frequency Scaling (DVFS) or multi-threshold CMOS (MTCMOS) to further reduce power consumption without compromising performance.
- Advanced Circuit Technologies: The implementation of more advanced technologies like FINFET or adiabatic logic can be explored to address power efficiency, speed, and scalability at smaller technology nodes like 45nm or 32nm.
- Integration with Memory and Control Units: The ALU could be integrated with memory blocks or control units for broader applications, supporting multi-cycle operations or pipelining for higher computational throughput.
- Implementation on FPGAs: The design could be implemented and tested on Field Programmable Gate Arrays (FPGAs) to enable real-world validation, optimize the design further, and assess performance in various application scenarios.

CHAPTER 6
HEALTH, SAFETY, RISK AND ENVIRONMENT ASPECTS

The design and implementation of a 4-bit Arithmetic Logic Unit (ALU) using 90nm CMOS technology, although primarily focused on digital circuit design and simulation, still involves some health, safety, and environmental considerations during the project's development phase, especially when the project transitions to physical hardware or testing stages. Below are the key health, safety, and environmental aspects relevant to this project:

Health and Safety Aspects

1. Handling of Electronic Components: While working on the design of the ALU, electronic components such as integrated circuits (ICs), microchips, and semiconductors are frequently handled. Although these components themselves are generally safe, care should be taken to avoid sharp objects or tools that could cause cuts or punctures while working with circuit boards. Additionally, static electricity can damage sensitive components, so antistatic wristbands and mats should be used when handling CMOS chips and other sensitive hardware components.

2. Electrical Hazards: If the project moves into physical prototyping (e.g., via FPGA or actual IC testing), there is a potential risk of electrical hazards. Users must be cautious when testing circuits with power supplies. For example, while testing the ALU design on an FPGA or integrated system, high voltages can sometimes be present, posing a risk of electrical shock if the power supply is not handled properly. Ensuring that the equipment is powered off when making connections and using insulated tools reduces the risk of accidental electrocution or short-circuiting.

3. Exposure to Chemicals: If the project involves the fabrication or etching of physical chips, it might require exposure to hazardous chemicals used in the process. Common chemicals include photoresists, etchants, and solvents, which are used during the chip fabrication phase. These chemicals can be harmful if mishandled, potentially causing skin irritation, eye damage, or inhalation risks. Proper personal protective equipment (PPE), such as gloves, goggles, and face shields, must be worn, and work should be done in a well-ventilated area to avoid chemical exposure.

Risk Management

1. Risk of Data Loss: While the project involves heavy reliance on simulation and design software, there is always a risk of data loss due to hardware failure, software crashes, or human error. To mitigate this risk, regular backups of the design files, simulation results, and documentation should be made. Using cloud storage or external drives for

backups helps safeguard against unforeseen issues, ensuring that progress is not lost during the project.

2. Risk of Design Errors: In digital circuit design, errors in logic or schematic design can lead to incorrect functionality or performance issues. These errors can result in wasted time during testing and debugging. To minimize such risks, detailed verification steps such as unit testing, simulation in Cadence Virtuoso, and peer review of the design should be implemented. Testing each component individually before integrating them into the larger system helps identify and address issues early.

3. Exposure to Radiation (During Fabrication): During the chip manufacturing process, particularly in photolithography, the use of ultraviolet (UV) light is common. UV radiation can pose health risks, including skin and eye damage if exposed for prolonged periods. Again, appropriate safety measures, including shielding and protective eyewear, are necessary when handling such tools. However, if the project remains at the simulation stage without moving to actual fabrication, the risks associated with radiation exposure are minimal.

Environmental Aspects

1. Energy Consumption: The CMOS-based 4-bit ALU design and simulation are largely computational and have minimal environmental impact when conducted on standard office or laboratory equipment. However, if the project moves into physical hardware implementation, such as with FPGA boards or IC chips, the energy consumption of the devices could have a slight environmental impact. Power-efficient design choices, like optimizing for low-power operation in the ALU, can help minimize the energy consumption of the final product.

2. E-Waste and Disposal of Electronics: The eventual disposal of any electronic components or hardware used in the project, such as ICs, FPGA boards, and other electronic devices, must be done responsibly. Electronic waste (e-waste) is a growing environmental concern, as improper disposal can lead to contamination of soil and water with harmful substances such as lead, mercury, and cadmium. To mitigate this, the project team should ensure that any obsolete or unused electronic components are disposed of through proper recycling programs that follow the guidelines set by environmental agencies. Additionally, adopting sustainable practices in design, such as reusing components or designing for longevity, can reduce the overall e-waste generated.

3. Sustainability in Semiconductor Manufacturing: The semiconductor industry is energy-intensive, with the fabrication process involving substantial amounts of water, chemicals, and energy. As part of future work, it's important to focus on sustainability in the design process, especially if the project extends into physical fabrication. Choosing low-power designs, like minimizing leakage currents in CMOS circuits, and advocating for sustainable semiconductor manufacturing practices, such as recycling water and reducing hazardous chemical use, can help mitigate the environmental impact of the project.

4. Reduction of Resource Consumption: In the context of VLSI design, minimizing the number of transistors and optimizing the layout of the ALU can reduce the overall resource consumption. Reducing the silicon area needed for manufacturing the ALU chip leads to a more sustainable approach, as it decreases material waste, energy use, and the overall carbon footprint of the fabrication process.

In conclusion, while the design and simulation of a 4-bit ALU using 90nm CMOS technology present relatively low direct health and safety risks, it is essential to ensure that proper precautions are taken to mitigate potential electrical, chemical, and physical hazards. Moreover, addressing the environmental impact, particularly concerning e-waste and energy consumption, is crucial. By adopting best practices for safety, sustainability, and risk management, the project can contribute to the advancement of digital circuit design while minimizing adverse impacts on human health and the environment.

REFERENCES

[1] L. Dhulipalla and A. Lourts Deepak, "Design and implementation of 4-bit ALU using FINFETS for nano scale technology," *International Conference on Nanoscience, Engineering and Technology (ICONSET 2011)*, Chennai, India

[2] S. Balaji Ramakrishna, A. G. Prasad, P. Anand and T. Aravind, "High Performance GDI-ALU Using 10T Adder Cells," *2018 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT)*, Bangalore, India, 2018

[3] Jin-Young Kim, Sehoon Kim and Joonhee Kang, "Construction of an RSFQ 4-bit ALU with half adder cells," in *IEEE Transactions on Applied Superconductivity*, vol. 15, no. 2, pp. 308-311, June 2005

[4] A. Pathak, S. Gupta and B. Jena, "Design and Evaluation of a 4-bit ALU and RAM System: A Step towards Ultra-Low Power Computing," *2023 International Conference on Next Generation Electronics (NEleX)*, Vellore, India, 2023

[5] E. A. Cortés-Barrón, M. A. Reyes-Barranca, L. M. Flores-Nava and A. Medina-Santiago, "4-Bit Arithmetic Logic Unit (ALU) based on Neuron MOS Transistors," *2012 9th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE)*, Mexico City, Mexico, 2012

[6] A. K. Panigrahi, S. Patra, M. Agrawal and S. Satapathy, "Design and Implementation of a high speed 4bit ALU using BASYS3 FPGA Board," *2019 Innovations in Power and Advanced Computing Technologies (i-PACT)*, Vellore, India, 2019

[7] A. Kumar, B. Kumawat and N. Pandey, "Design of 4-bit ALU using TEAM Memristor Model and CMOS Logic," *2020 International Conference on Communication and Signal Processing (ICCSP)*, Chennai, India, 2020

[8] R. V. Biswas, M. H. Ahanaf and S. T. Nidhi, "A 2.319 uW, 37.34 MHz Transmission Gate Based 4-Bit ALU for Contemporary Low-powered, High-Speed Microprocessors," *2024 6th International Conference on Electrical Engineering and Information & Communication Technology (ICEEICT)*, Dhaka, Bangladesh, 2024

[9] J. L. V. Ramana Kumari, Y. Varshitha, C. Gopi and M. Rakesh, "Design and Implementation of ALU Using Ring Counters," *2023 International Conference on Signal Processing, Computation, Electronics, Power and Telecommunication (IConSCEPT)*, Karaikal, India, 2023

[10] G. N. Chiranjeevi and S. Kulkarni, "Pipeline Architecture for N=K*2L Bit Modular ALU: Case Study between Current Generation Computing and Vedic Computing," *2021 6th International Conference for Convergence in Technology (I2CT)*, Maharashtra, India, 2021

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Project Duration	7 months	Date of reporting	12-03-2025
Internal Guide Details			
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