EXPERIMENT NO. 10

Aim: Implementation of the synthesized RTL of ALU in FPGA board.

Perform the following activities.

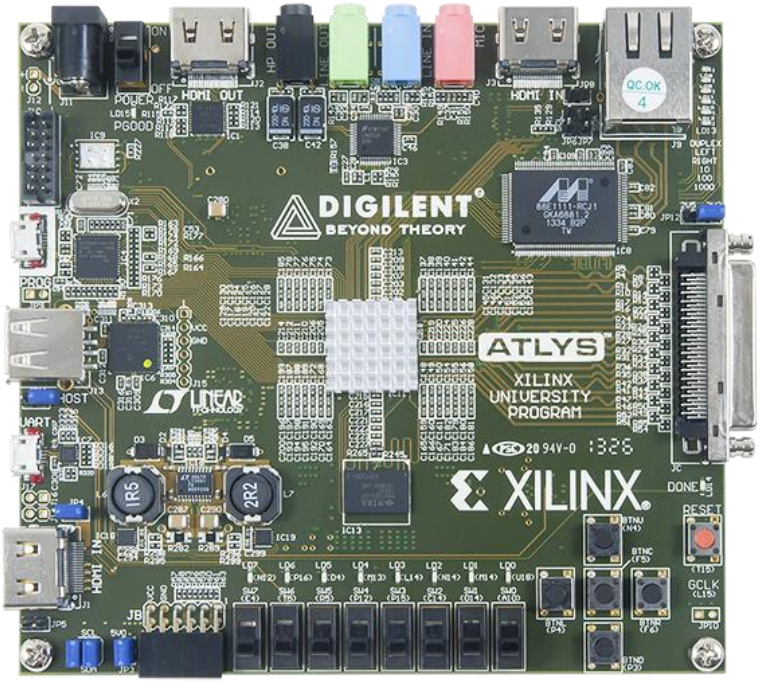
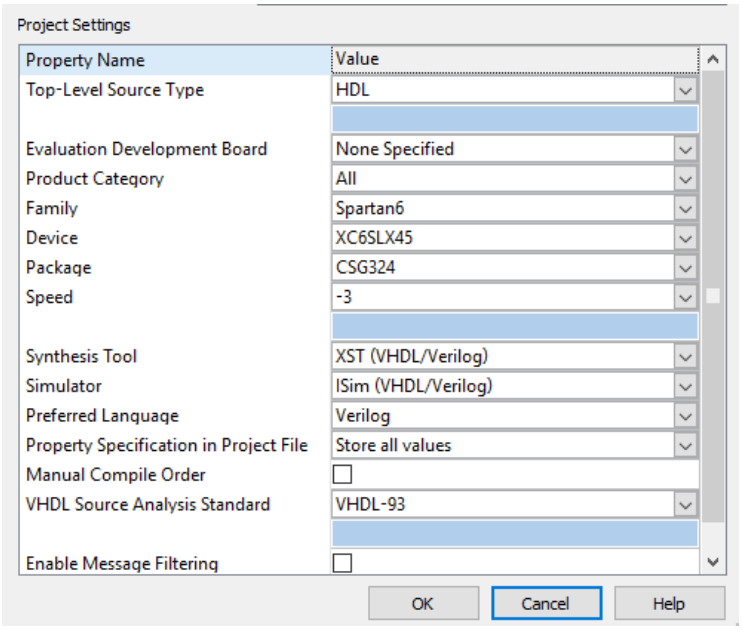


Fig.: DIGILENT XILINX SPARTAN6 Board.

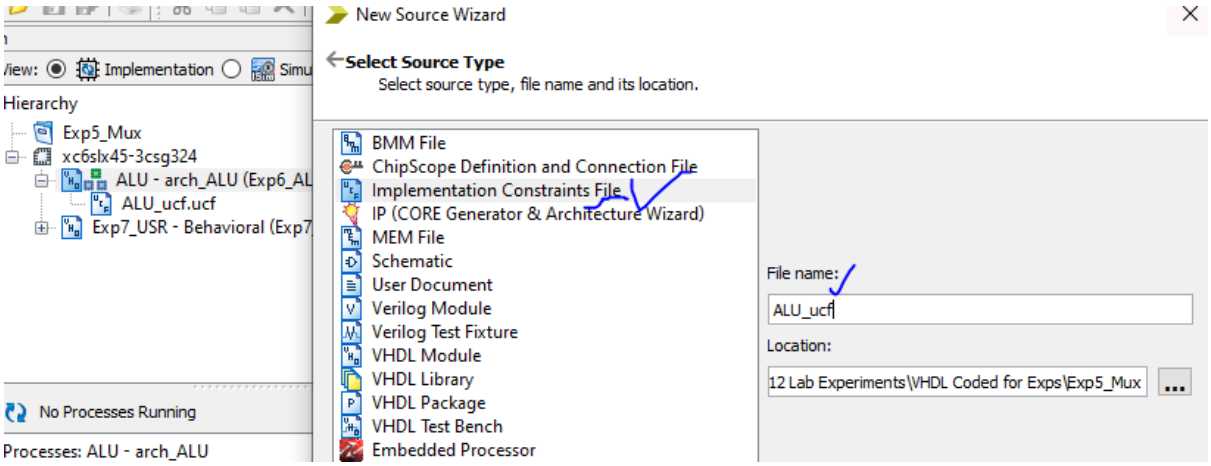
Activity 1: **Se the Spartan 6 FPGA device family, device, package and grade.**



Activity 2: **The VHDL model developed for 4-bit ALU in Exp-7. Convert it for 2-bit inputs and output because there are only 8-input switches in FPGA board.**

- Check the syntax
- Perform the Synthesis

Activity 3: Create the user constraint file and map the ALU inputs and outputs.



Activity 4: In the UCF file map the ALU inputs and outputs with FPGA boards input switches and output LEDs.

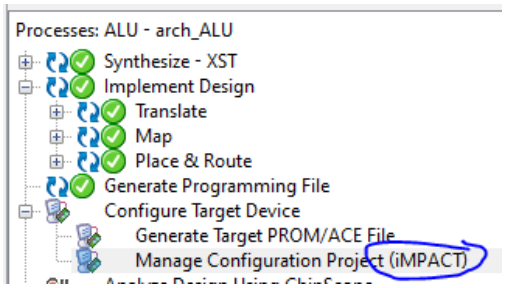
```
1
2   NET "a[1]" LOC = "E4";
3   NET "a[0]" LOC = "T5";
4   NET "b[1]" LOC = "r5";
5   NET "b[0]" LOC = "P12";
6
7   NET "sel[2]" LOC = "c14";
8   NET "sel[1]" LOC = "d14";
9   NET "sel[0]" LOC = "a10";
10
11  NET "y[1]" LOC = "m14";
12  NET "y[0]" LOC = "u18";
```

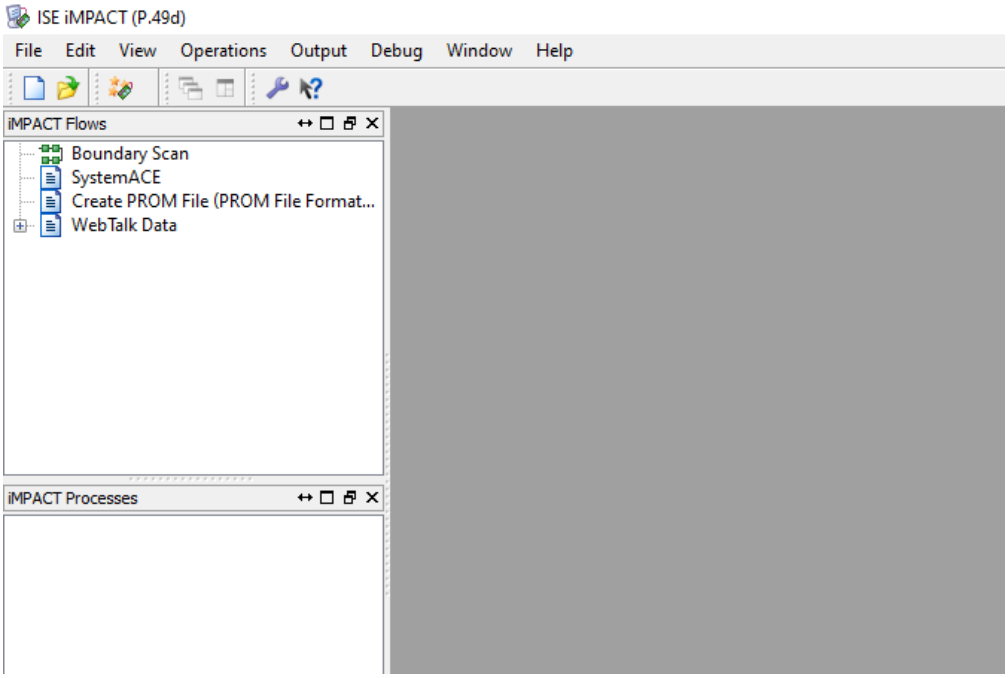
Activity 5: **The VHDL model developed for 4-bit ALU in Exp-7. Convert it for 2-bit inputs and output because there are only 8-input switches in FPGA board.**

- Perform the implementation
- Generate the configuration file i.e. .bit file.

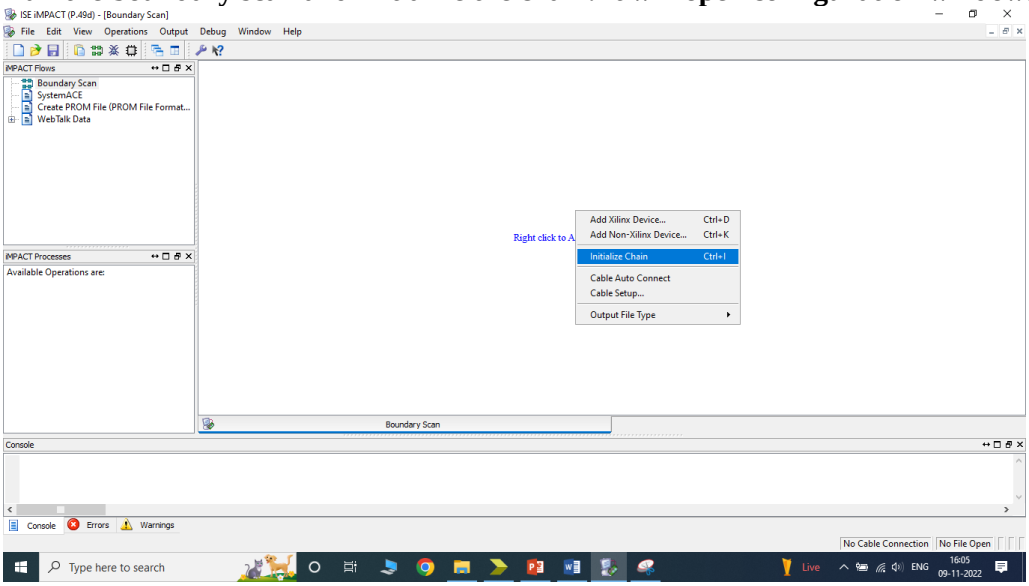
Activity 6: Download the *.bit* file in the FPGA board.

- **Run the manage configuration project. It will open iMPACT window**

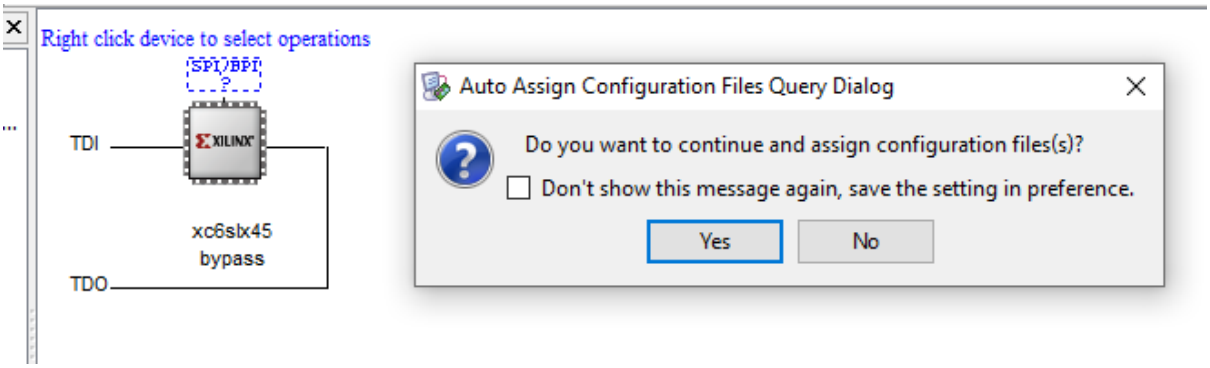




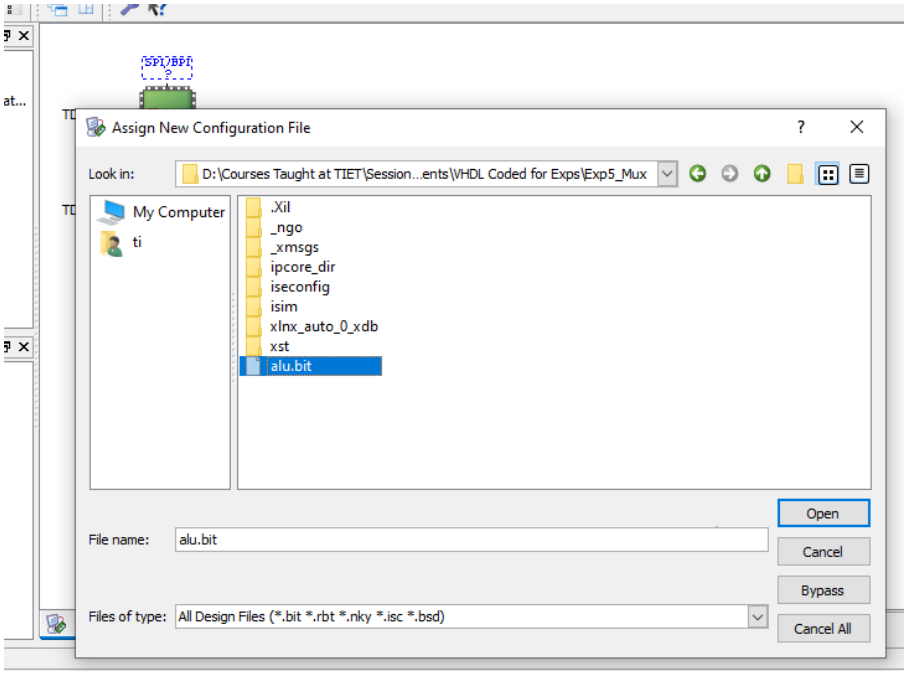
- **Run the boundary scan and initialize the chain. It will open configuration window.**



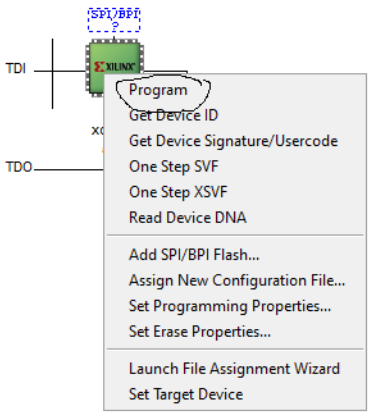
- **Click Yes in configuration window**



- Locate the .bit file i.e. .alu and open it



- Program the device



Activity 4: Apply the inputs and verify the outputs.