(68)

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(Paper code and roll No. to be filled in your answer book)

Paper code: KCS-402/ KIT-402 Roll No. 1 3 2 0 3

B.Tech.
Fourth Semester Examination, 2014-15
Computer Organisation

Time: 3 Hours **Total Marks: 100**

Note: - Attempt all questions. Each questions carry equal marks.

(1) Attempt any four parts of the following: 5x4=20

(a) Explain the functions of different computer units.

(b) Explain the various generation of computer

(c) Define Bus. What are the different buses in a CPU?

(15)

(d) Using 8 bit two's complement integers, perform the following computations.

(i) -35 + (-11)

(ii) 19- (-4)

(e) Explain the implementation of common bus using tri state buffer.

(f) What is the value of the single precision floating point number represented by the 4 A 6 B7 29F?

(2) Attempt any four parts of the following: 5x4=20

(a) Explain carry lookahead adders.

(15)

(b) State the Non-restoring division technique.

(c) What are the various addressing modes? Explain.

(d) Explain various fields of instruction format. Classify the instructions according to address references.

(e) Explain the sequence of operations needed to perform following CPU functions.

(i) Fetching a word from memory

(ii) Performing arithmetic as logical operation.

(f) Explain the operation of micro program sequences.

(3) Attempt any two parts of the following: 10x2=20

(10)

(a) Design a ALU that performs the four arithmetic operations add, subtract increment, decrement, four logic operations of exclusive OR, exclusive –NOR, NOR and NAND two-shift left and right.

(b) What is booth algorithm? What are the two attractive features of Booth algorithm? Explain hardware implementation of Booth algorithm.

(c) (i) Explain the concept of hardware control unit.

(ii) Compare vertical organization and horizontal organization.

4. Attempt any two parts of the following: 10x2=20

(a) (i) What is memory hierarchy? Explain.

(ii) How many 128 bytes RAM chips are required to provide a memory of 2048 bytes? Show details of connection indicating address, data and decoder configuration

(b) What is cache memory? Define hit rate. A block set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16384 blocks and each block contains 256 eight bit words.

(i) How many bits are required for addressing the main memory?

(ii) How many bit needed to represent the TAG, SET, WORD fields?

(c) (i) What is virtual memory? Explain the working of address translation in virtual memory system.

(ii) An address space is specified by 24 bits and the corresponding memory space by 16 bits

(iii) How many words are there in the address space?

(iv) How many words are there in the memory space?

5. Attempt any two parts of the following: 10x2=20

(a) Explain with the block diagram of the DMA transfer in a computer system.

(b) What are interrupts? How are they handled?

(c) (i) Draw and explain the block diagram of I/O system.

(ii) Differentiate between synchronous and asynchronous data transfer.