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K. N. I. T., SULTANPUR

(Paper code and roll No to be filled in your answer book)

Paper code: KEC-302 Roll No. | | | | | | | | | | |

B.Tech. (Main & COP)
Third Semester Examination, 2016-17
Digital Electronics

Time: 3 Hours **Total Marks: 100**

Note: Attempt all questions. Assume missing data suitably.

1. Attempt any four parts of the following: (5x4=20)

(a) The state of 12 bit register is 100110110101. What is it contents if it represents.

(i) The three decimal digits in BCD.

(ii) Three decimal digits in excess-3 code.

(iii) 3 decimal digits in $8\bar{4}\bar{2}\bar{1}$ code.

(b) Assume that the even parity hamming code 1001100 is transmitted and that 1000100 is received. Determine the error bit location & correct the received code using Hamming correction method.

(c) Represent $(1460.125)_{10}$ in single precision & double precision format.

(d) Simplify the given boolean function using tabular method-

$Y(A,B,C,D,E)= \sum m(0,1,2,4,5,7,10,11,13,16,17,19,21,24,27,31)$

(e) Simplify the given Boolean function using K-map method.

$F(A,B,C,D,E)=\sum m\ (8,9,10,11,13,15,17,18,21,23,27,29,31)$

(f) Simplify the following function and implement them-

$F=w\bar{x} + \bar{y}z + \bar{w}y\bar{z}$

(i) Using NAND gates only

(ii) Using NOR gates only.

2. Attempt any four parts of the following: (5x4=20)

(a) Draw the logic diagram of carry look ahead carry adder. If XOR gate, AND gate & OR gate has delay of 30 nsec, 15nsec & 10nsec respectively that what is total propagation delay.

(b) Draw logic diagram of decimal odder with the help of BCD addition & explain.

(c) Design a 3 bit magnitude comparator & explain it.

(d) Design a BCD to seven-segment display decoder.

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(e) Define multiplexer using 4x1 multiplexer. Implement the following Boolean function using 8:1 multiplexer taking 'c' as input:

$F(A,B,C,D)= \sum m(0,1,3,4,8,10,11,15)$

(f) Design a 3 bit combinational logic circuit 2's complement which output generates the 2's complement of input binary numbers.

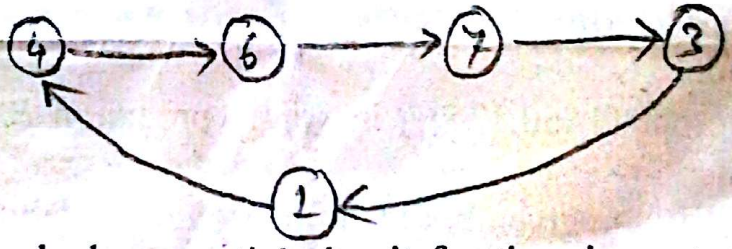
3. Attempt any two parts of the following: (10x2=20)

(a) (i) Explain the operation of S-R latch with help of logic diagram and Draw its timing diagram.

(ii) Draw the logic diagram and timing diagram for MOD-10 ripple-up counter.

(b) (i) Draw logic diagram for 4 bit Bidirectional shift register and explain its operation.

(ii) Design a synchronous counter with given sequence using D flip-flop. Does it suffer from lock out? If yes, then draw state diagram.



(c) Design a clocked sequential circuit for the given state diagram show in fig.(1) with help of J-K flip-flop.

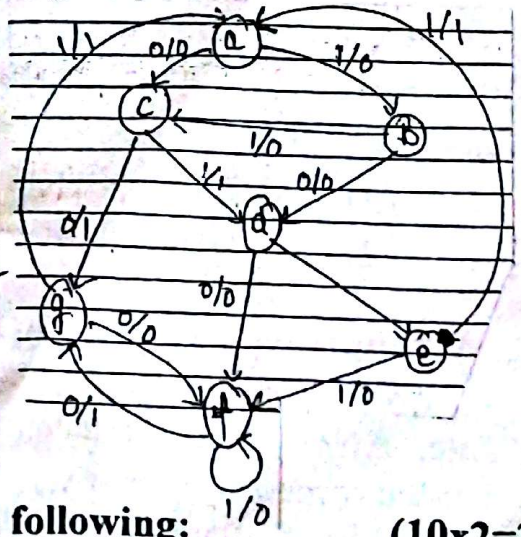


fig.1

4. Attempt any two parts of the following: (10x2=20)

(a) Explain RAM in detail. Draw & explain the timing waveform for write & read cycle of RAM.

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(b) (i) Explain Block diagram of PAL. Implement the given function in PAL.

$A(W,X,Y,Z) = \sum m(0, 2, 6, 7, 9, 12)$

$B(W,X,Y,Z) = \sum m(0, 2, 8, 9, 13, 14)$

$C(W,X,Y,Z) = \sum m(1, 3, 4, 6, 9, 12)$

(ii) Draw the ASM chart for a 2 bit counter having one enable input such that, count is enabled if E= 1 & disabled if E= 0.

(c) Draw state diagram & ASM chart for serial adder & explain it.

5. Attempt any two parts of the following: **(10x2=20)**

(a) What do you mean by Race condition? How critical races can be avoided.

(b) An asynchronous sequential circuit has two internal states & one output has following function describing the circuit as:

$Y_1 = x_1x_2 + x_1y_2 + x_2x_2$

$Y_2 = x_2 + x_1y_1y_2 + x_1y_1$

$Z = x_2 + y$

(i) Draw the logic diagram.

(ii) Derive transition table & output map.

(c) (i) Find the set of maximal compatible using merger graph/table method for the given state-table of the incompletely specified sequential machines.

PS	NS			
	I_1	I_2	I_3	I_4
A	-	C, -	-	-, 1
B	A, 1	-	B, 0	-
C	-	-	-	D, 1
D	C, -	A, -	C, -	F, 0
E	B, -	B, -	F, -	-, 0
F	-, 0	C, 1	-	B, 1

(ii) What do you mean by Hazards in combinational logic circuit? Explain.

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