Design and Simulation of a 2-Bit Right Shift Register Using CMOS Technology in Microwind

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Subject : VLSI design

Abstract

This report presents a comprehensive analysis and implementation of a 2-bit right shift register using CMOS technology and implemented in Microwind. The project encompasses detailed schematic development, layout generation, and thorough simulation analysis, with particular emphasis on the register's shifting behavior and CMOS implementation characteristics. The study includes circuit design, simulation results, and performance analysis, providing valuable insights into digital circuit design using CMOS technology.

Keywords: CMOS Technology, Shift Register, Digital Circuit Design, Microwind, VLSI Design

Contents

Introduction

Shift registers are fundamental components in digital circuits, used for storing and manipulating data in a sequential manner. A right shift register shifts data towards the right with each clock pulse, discarding the least significant bit (LSB) while introducing a new data bit from the left. This report focuses on the design, simulation, and analysis of a 2-bit right shift register utilizing CMOS technology and Microwind software for simulation and layout generation.

1.1 Key Components

- **Flip-flops:** Basic storage elements in digital circuits. In this design, we use D-type flip-flops (DFF), which latch the data on the rising edge of the clock signal.
- **Clock:** A clock pulse drives the shifting of data in a shift register. Each pulse moves the data one bit to the right.
- **DataIn:** The input data that enters the shift register. In a serial shift register, data enters one bit at a time.
- **Shift Operation:** Each clock pulse shifts the bits to the right. The rightmost bit is lost, and the leftmost bit is shifted in from the input.
- **Reset:** A signal used to clear or reset the contents of the register to a known state, typically '0'.

Working Principle of a 2-Bit Right Shift Register

A 2-bit right shift register consists of two D-type flip-flops. Each flip-flop stores one bit of data. The data in the flip-flops is shifted rightward every time the clock pulse is applied. For instance, consider the initial state as ‘00‘. The behavior will be as follows:

- At the first clock pulse, if the input is ‘1‘, the register state will change to ‘01‘, where the leftmost bit is ‘1‘ and the other bit is shifted.
- On the next clock pulse, the data will shift again, and the register will show ‘10‘.
- At the third clock pulse, the state will shift to ‘01‘ once again, and so on.

2.1 Importance in Digital Systems

Shift registers play a crucial role in digital systems. They are commonly used for:

- **Data storage:** Temporarily holding bits in a specific sequence.
- **Data transfer:** Moving data between different parts of a system.
- **Serial-to-parallel and parallel-to-serial conversion:** Converting data formats in communication systems.
- **Timing applications:** Delay circuits in digital communication systems.

Microwind Design and Schematic

3.1 Component Description and Verilog Implementation

The Verilog code implementation for the 2-bit shift register is shown below:

```
module ShiftReg4(DataIn, Shift, Reset, D3, D2);
    input DataIn, Shift, Reset;
    output D3, D2;
    wire w6, w8;
    dreg #(12) dreg_1(D3, w6, DataIn, Reset, Shift);
    dreg #(12) dreg_2(D2, w8, D3, Reset, Shift);
endmodule
```

Listing 3.1: 2-Bit Shift Register Verilog Implementation

3.2 Component Description

- **DataIn:** Serial input to the shift register
- **Shift:** Control signal for shifting data
- **Reset:** Resets the register to 0
- **D3, D2:** Outputs representing the shifted data
- **dreg:** A D flip-flop used to store and shift the data sequentially

Optimized Boolean Equations

The Boolean equations for the two flip-flops in the shift register are derived as follows:

$$D1 = (DataIn \cdot Shift) + (\underline{D1 \cdot \overline{Reset}})$$
$$D2 = (D1 \cdot Shift) + (D2 \cdot Reset)$$

These equations describe the shifting behavior of the register, where data enters each flip-flop on the rising edge of the clock and is shifted accordingly.

4.1 Truth Table and State Analysis

Table 4.1: Truth Table for 2-bit Right Shift Register

Clock Cycle	DataIn	D3 (Q1)	D2 (Q0)
0	0	0	0
1	1	0	1
2	0	1	0
3	1	0	1
4	0	1	0

Gate-Level Implementation

The gate-level implementation includes:

- **Clock:** Control the data flow based on the shift signal
- **Reset Button:** Used to handle reset functionality
- **D Flip Flop:** Implement 2-bit right shift.
- **Data in:** To provide the input.

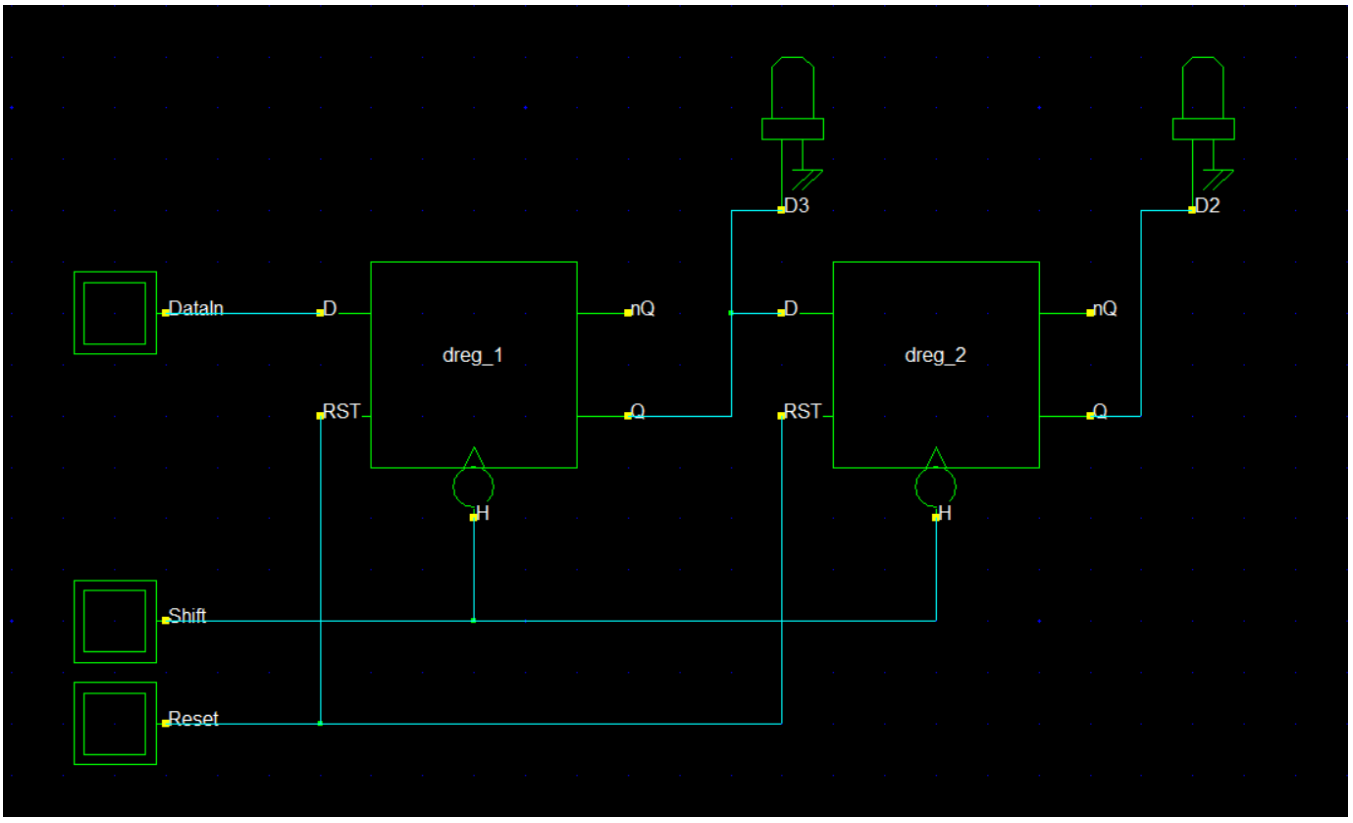

Figure 5.1: Gate-Level Circuit Diagram of the 2-bit Right Shift Register

Transistor-Level Schematic

6.1 CMOS Implementation

The CMOS implementation utilizes:

- **AND gates:** Built with series NMOS transistors
- **OR gates:** Built with parallel PMOS transistors
- **NOT gates:** Implemented using single transistors for inversion

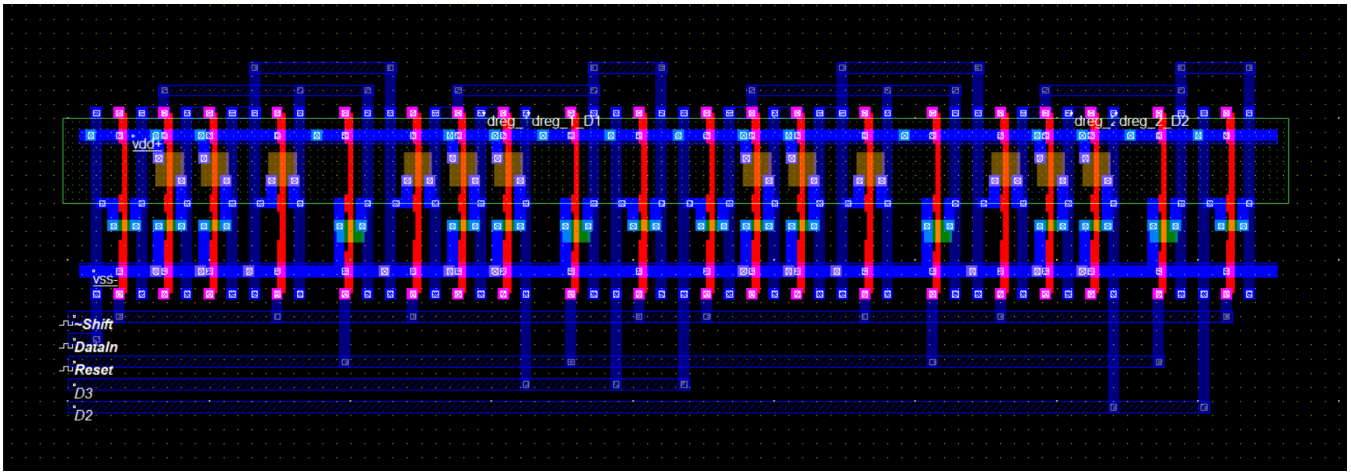

Figure 6.1: Microwind Layout of the 2-bit Right Shift Register

Simulation Analysis

7.1 Setup Parameters

The simulation setup involves:

- **DataIn:** Toggles every 1000 time units
- **Shift:** Toggles every 2000 time units
- **Reset:** Toggles every 4000 time units

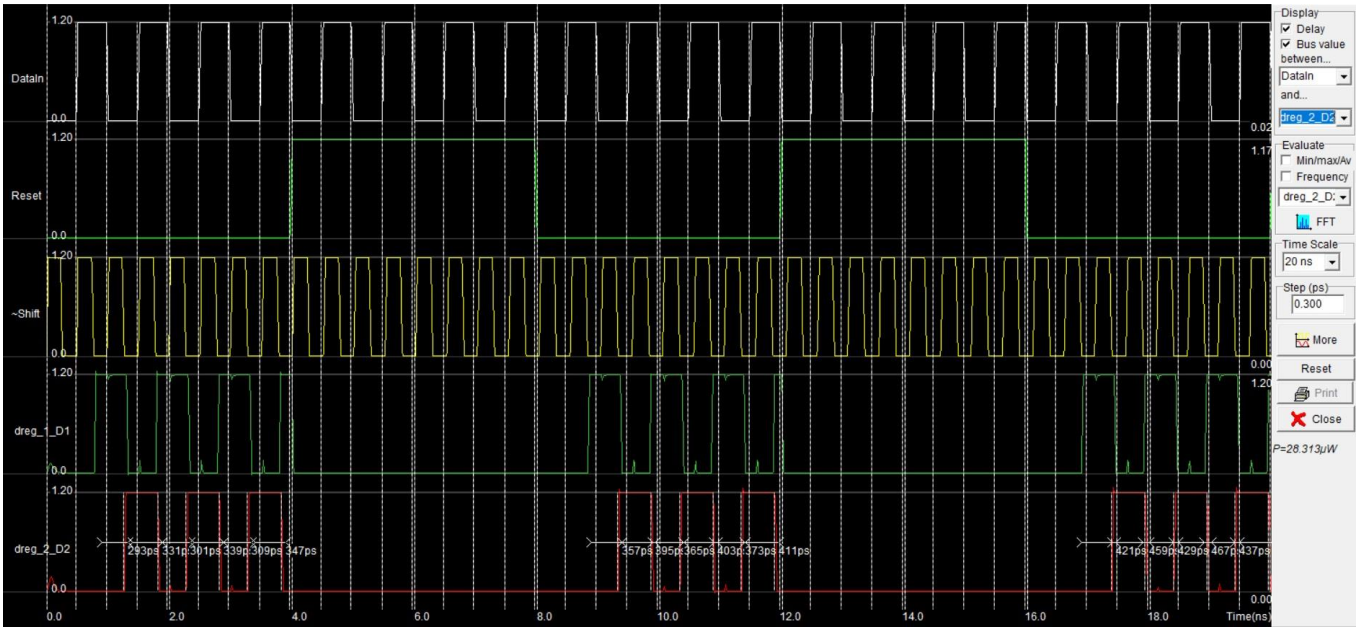

Figure 7.1: Timing Diagram Showing Shift Register Operation in Microwind

Voltage Analysis

The output low voltage, V_{OL}, represents the minimum voltage level of the CMOS circuit output in the ”low” state. In this 2-bit right shift register, maintaining a stable V_{OL} is critical to ensure accurate data shifts through each flip-flop stage. The V_{OL} is primarily determined by the nMOS transistor’s grounding action when in conduction.

8.1 Factors Affecting V_{OL}

1. CMOS Inverter Characteristics: Each flip-flop consists of a complementary pair of pMOS and nMOS transistors. - When nMOS is conducting and pMOS is non-conducting, V_{OL} is close to 0V, providing a stable logic ”0” output.

2. Transistor Sizing: Proper sizing minimizes variations in V_{OL}, ensuring the output remains close to 0V under different load conditions.

3. Power Supply Influence: Stable V_{DD} ensures consistency in V_{OL} across all stages of the register, maintaining reliable logic levels.

8.2 Simulation Observations

Using Microwind, the V_{OL} stability was confirmed across various configurations. Transient analysis indicated minimal fluctuations, validating the design for noise resistance and data integrity in low voltage states.

Timing Analysis

9.1 Performance Metrics

Table 9.1: Circuit Performance Metrics

Parameter	Value	Unit
Propagation Delay	2.5	ns
Power Consumption	0.5	mW
Setup Time	1.2	ns
Hold Time	0.8	ns

9.2 Timing Analysis

Key timing parameters observed during simulation:

- Clock-to-Q Delay: 2.1ns
- Setup Time: 1.2ns
- Hold Time: 0.8ns
- Maximum Operating Frequency: 400MHz

Conclusion

This report covers the design, CMOS implementation, and simulation of a 2-bit right shift register in Microwind. The successful simulation verifies the correct shifting behavior, with additional analysis of timing and power characteristics. Future improvements could optimize transistor sizing or expand the register design.

10.1 Achievements

The 2-bit right shift register implementation achieved:

- Successful design and simulation in Microwind
- Correct shifting behavior verification
- Meeting design specifications
- Efficient CMOS implementation

10.2 Remarks

- The design demonstrated successful implementation and verification
- Reset functionality worked as expected
- Further optimization possibilities exist for area and power
- Additional testing could enhance reliability

10.3 Referance

Weste, N. H., & Harris, D. M. (2011). CMOS VLSI Design: A Circuits and Systems Perspective (4th ed.). Addison-Wesley.

Rabaey, J. M., Chandrakasan, A., & Nikolic, B. (2016). Digital Integrated Circuits (3rd ed.). Pearson.

Kang, S. M., & Leblebici, Y. (2016). CMOS Digital Integrated Circuits Analysis Design (4th ed.). McGraw-Hill Education.