



## B.M.S COLLEGE OF ENGINEERING

(Autonomous College Affiliated to Visvesvaraya Technological University, Belgaum)  
Bull Temple Road, Basavanagudi, Bangalore-560019

# LABORATORY MANUAL

for  
“MIXED SIGNAL DESIGN”  
(19EC6PCMSD)

SEMESTER: VI

ACADEMIC YEAR: 2022-23

COURSE CO-ORDINATOR: Sanjana T

COURSE INSTRUCTORS: Dr. Rajath Vasudevamurthy, Dr. Archana H. R, Smt. Sanjana T, Smt. Ashwini V, Smt. Shrisha M. R.

Dr. Siddappaji  
HOD ECE

## LIST OF EXPERIMENTS

1. Inverter- Transient and DC analysis
2. Inverter- Parametric analysis
3. Inverter- Layout (DRC and LVS check)
4. Common Source amplifier- Transient, DC and AC analysis
5. Common Drain amplifier- Transient, DC and AC analysis
6. Differential amplifier- Transient, DC and AC analysis
7. Operational amplifier- Transient, DC and AC analysis
8. R-2R DAC using Opamp- Transient analysis

## **UNIX COMMANDS TO OPEN CADENCE VIRTUOSO:**

MobaXterm app (any other app for remote connection can be used) is used to connect local machine to remote server

Click on start local terminal

In the terminal type the following commands:

```
ssh -X user1@10.40.4.51
```

Note: user number can be changed, limit is the maximum number of users allowed under licence

```
csh
```

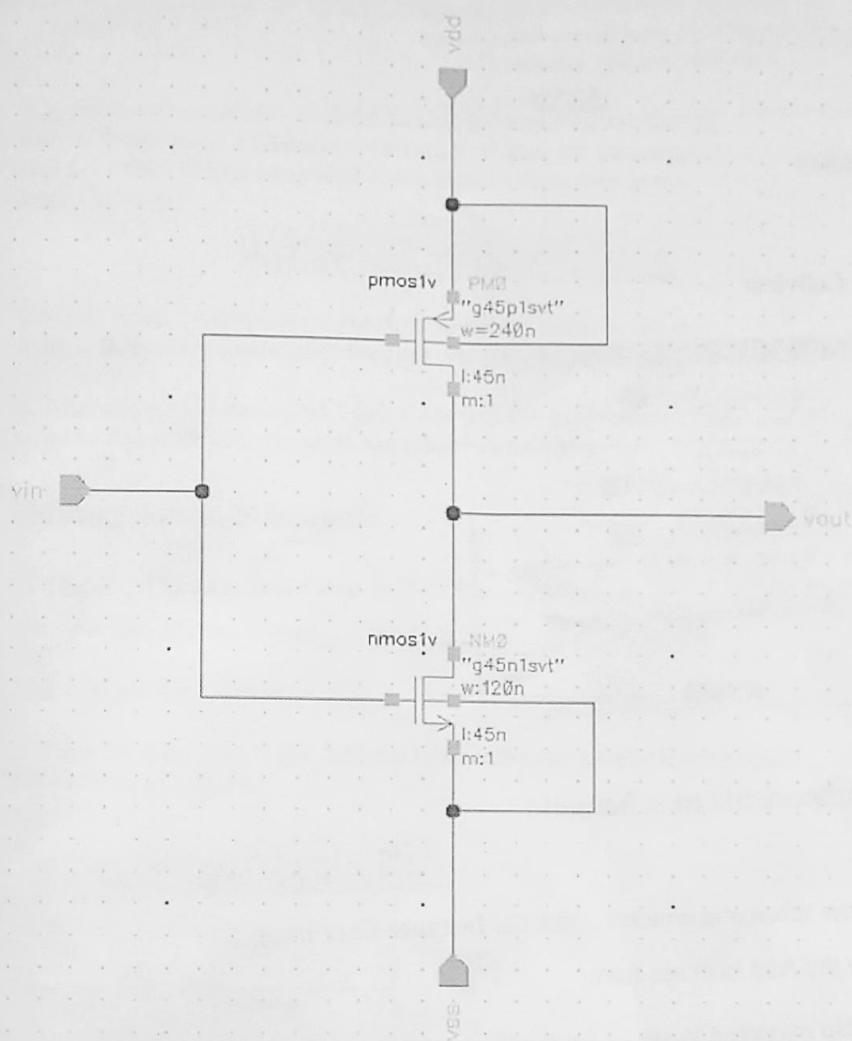
```
source cshrc1
```

```
cd cadence_ms_labs_614
```

```
virtuoso &
```

## EXPERIMENT NO.1: INVERTER- Transient and DC analysis

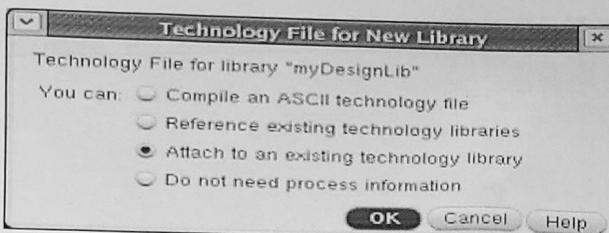
### SCHEMATIC:



### Creating a New library

1. In the Library Manager, execute **File - New – Library**. The new library form appears.
- CCMO2. In the “New Library” form, type “**myDesignLib**” in the Name section.

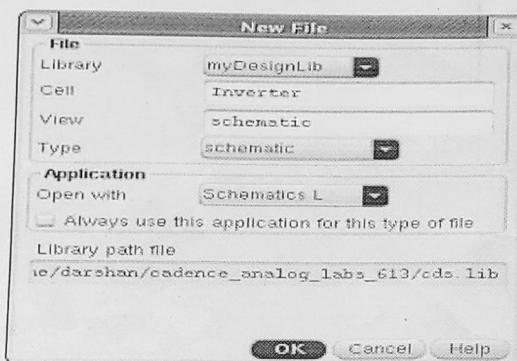
**Note: Library name can be anything (should not include spacing)**



**Choose gpdk045**

**Click on ok**

**File – New – Cellview**



**Adding Components to schematic**



1. In the Inverter schematic window, click the **Instance** fixed menu icon to display the Add Instance form.



**Tip:** You can also execute **Create — Instance** or press **i**.

2. Click on the **Browse** button. This opens up a Library browser from which you can select **components and the symbol view**.

You will update the Library Name, Cell Name, and the property values given in the table on the next page as you place each component.

3. After you complete the Add Instance form, move your cursor to the schematic window and click **left** to place a component.

This is a table of components for building the Inverter schematic.

Library name	Cell Name	Properties/comments
gdk045	pmos1v	W=240n, L=45n
gdk045	nmos1v	W=120n, L=45n

If you place a component with the wrong parameter values, use the **Edit—Properties—Objects** command to change the parameters. Use the **Edit—Move** command if you place components in the wrong location.



You can rotate components at the time you place them, or use the **Edit—Rotate** command after they are placed.

- After entering components, click **Cancel** in the Add Instance form or press **Esc** with your cursor in the schematic window.

## Adding pins to Schematic

- Click the **Pin** fixed menu icon in the schematic window.

You can also execute **Create — Pin** or press **p**.



The Add pin form appears.

- Type the following in the Add pin form in the exact order leaving space between the pin names.

Pin Names	Direction
vin	Input
vout	Output

Make sure that the direction field is set to **input/output/inputOutput** when placing the **input/output/inout** pins respectively and the Usage field is set to **schematic**.

3. Select **Cancel** from the Add – pin form after placing the pins.

In the schematic window, execute **Window—Fit** or press the **f** bindkey.



## Adding Wires to a Schematic

Add wires to connect components and pins in the design.

1. Click the **Wire (narrow)** icon in the schematic window.

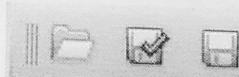
You can also press the **w** key, or execute **Create — Wire (narrow)**.



2. In the schematic window, click on a pin of one of your components as the first point for your wiring. A diamond shape appears over the starting point of this wire.
3. Follow the prompts at the bottom of the design window and click **left** on the destination point for your wire. A wire is routed between the source and destination points.
4. Complete the wiring as shown in figure and when done wiring press **ESC** key in the schematic window to cancel wiring.

## Saving the Design

1. Click the **Check and Save** icon in the schematic editor window.



2. Observe the CIW output area for any errors.

# Symbol Creation

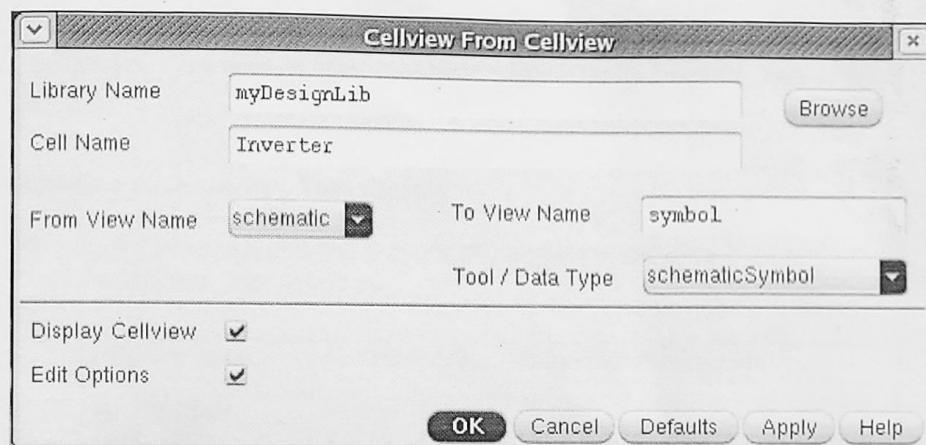
## Objective: To create a symbol for the Inverter

In this section, you will create a symbol for your inverter design so you can place it in a test circuit for simulation. A symbol view is extremely important step in the design process. The symbol view must exist for the schematic to be used in a hierarchy. In addition, the symbol has attached properties (cdsParam) that facilitate the simulation and the design of the circuit.

1. In the Inverter schematic window, execute **Create — Cellview— From Cellview**.

The **Cellview From Cellview** form appears. With the Edit Options function active, you can control the appearance of the symbol to generate.

2. Verify that the **From View Name** field is set to **schematic**, and the **To View Name** field is set to **symbol**, with the **Tool/Data Type** set as **SchematicSymbol**.



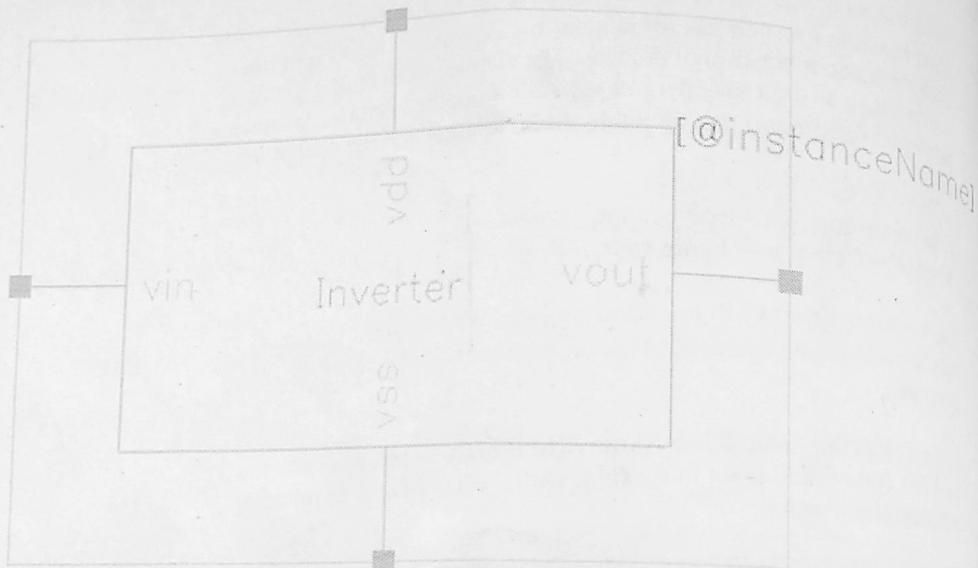
3. Click **OK** in the **Cellview From Cellview** form.

The Symbol Generation Form appears.

4. Modify the **Pin Specifications**

Specify the pins appropriately as top, bottom, right or left pin

5. Click **OK** in the Symbol Generation Options form.
  6. A new window displays an automatically created Inverter symbol
- Editing symbol shape is optional**



# **Building the Inverter\_Test Design**

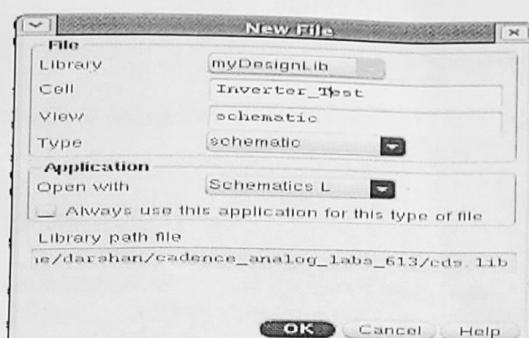
**Objective:** To build an Inverter Test circuit using your Inverter

## **Creating the Inverter\_Test Cellview**

You will create the Inverter\_Test cellview that will contain an instance of the Inverter cellview. In the next section, you will run simulation on this design.

1. In the CIW or Library Manager, execute File— New— Cellview.

2. Set up the New File form as follows:



3. Click **OK** when done. A blank schematic window for the **Inverter\_Test** design appears.

## **Building the Inverter\_Test Circuit**

1. Using the component list and Properties/Comments in this table, build the **Inverter\_Test** schematic.

Library name	Cellview name	Properties/Comments
myDesignLib	Inverter	Symbol
analogLib	Vpulse	v1=0, v2=1.8, td=0 tr=tf=1ns, ton=10n, T=20n
analogLib	vdc, gnd	vdc=1.8

**Note:** Remember to set the values for **VDD** and **VSS**. Otherwise, your circuit will have no power.

**Set Vdc and V2 to 1 V for 45nm technology.**

2. Add the above components using **Create — Instance** or by pressing **I**.

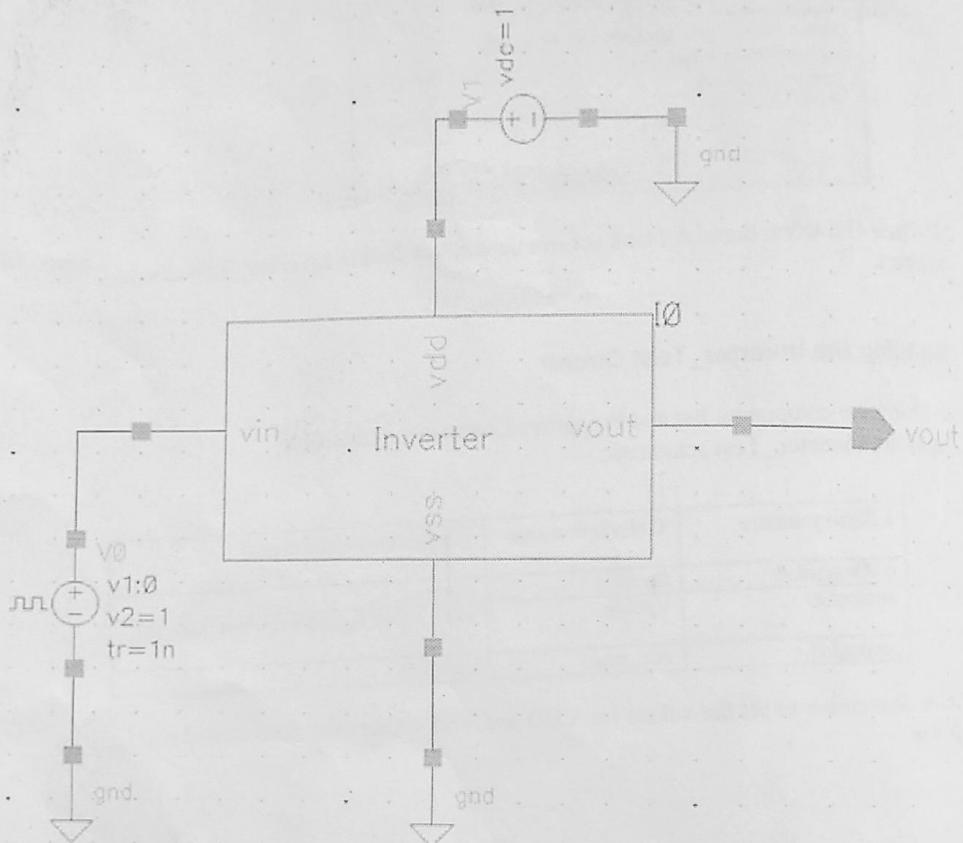
3. Click the **Wire (narrow)** icon and wire your schematic.

**Tip:** You can also press the **w** key, or execute **Create — Wire (narrow)**.

4. Click **Create — Wire Name** or press **L** to name the input (**V<sub>in</sub>**) and output (**V<sub>out</sub>**) wires as in the below schematic.

4. Click on the **Check and Save** icon to save the design.

5. The schematic should look like this.



# Analog Simulation with Spectre

**Objective:** To set up and run simulations on the Inverter\_Test design

In this section, we will run the simulation for Inverter and plot the transient, DC characteristics and we will do Parametric Analysis after the initial simulation.

## Starting the Simulation Environment

Start the Simulation Environment to run a simulation.

1. In the **Inverter\_Test** schematic window, execute  
**Launch – ADE L**

The **Virtuoso Analog Design Environment (ADE)** simulation window appears.

## Choosing a Simulator

Set the environment to use the **Spectre® tool**, a high speed, highly accurate analog simulator. Use this simulator with the **Inverter\_Test** design, which is made-up of analog components.

1. In the simulation window (ADE), execute  
**Setup— Simulator/Directory/Host.**
2. In the Choosing Simulator form, set the Simulator field to **spectre** (Not spectreS) and click **OK**.

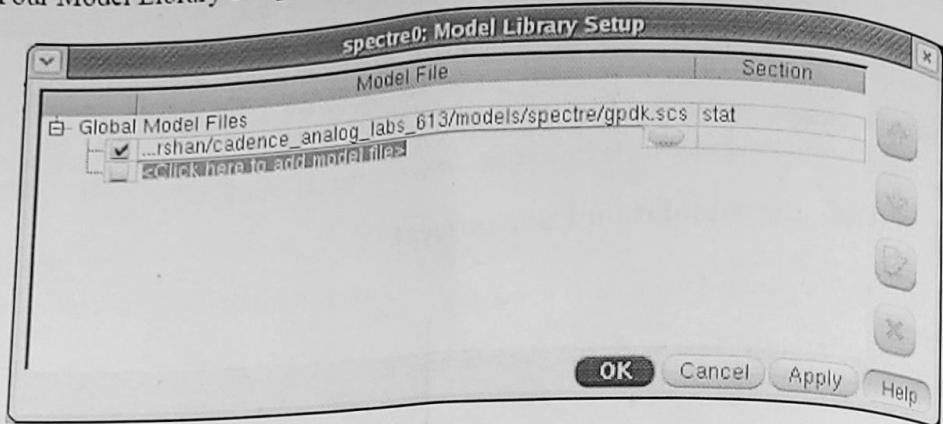
## Setting the Model Libraries

The Model Library file contains the model files that describe the nmos and pmos devices during simulation.

1. In the simulation window (ADE),  
**Execute Setup - Model Libraries.**

The Model Library Setup form appears. Click the **browse** button  to add **gpdk.scs** if not added by default as shown in the Model Library Setup form. Remember to select the section type as **stat** in front of the **gpdk.scs** file.

Your Model Library Setup window should now look like the below figure.



To view the model file, highlight the expression in the Model Library File field and Click **Edit File**.



2. To complete the Model Library Setup, move the cursor and click **OK**.

The Model Library Setup allows you to include multiple model files. It also allows you to use the Edit button to view the model file.

## Choosing Analyses

This section demonstrates how to view and select the different types of analyses to complete the circuit when running the simulation.

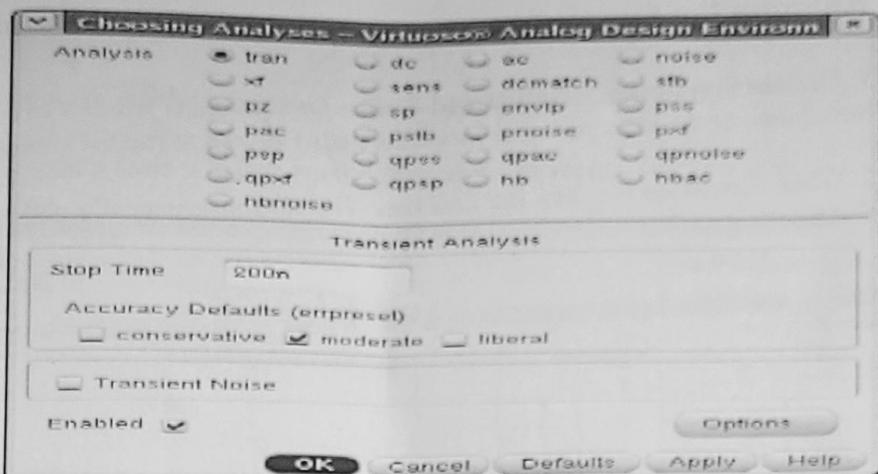


1. In the Simulation window (ADE), click the **Choose - Analyses** icon. You can also execute **Analyses - Choose**.

The Choosing Analysis form appears. This is a dynamic form, the bottom of the form changes based on the selection above.

2. To setup for transient analysis

- In the Analysis section select **tran**
- Set the stop time as **200n**
- Click at the **moderate** or **Enabled** button at the bottom, and then click **Apply**.



3. To set up for DC Analyses:

- In the Analyses section, select dc.
- In the DC Analyses section, turn on Save DC Operating Point.
- Turn on the Component Parameter.
- Double click the Select Component, Which takes you to the schematic window.
- Select input signal **vpulse** source in the test schematic window.
- Select —DC Voltage in the Select Component Parameter form and click OK.
- In the analysis form type start and stop voltages as 0 to 1 respectively.
- Check the enable button and then click Apply.

4. Click OK in the Choosing Analyses Form.

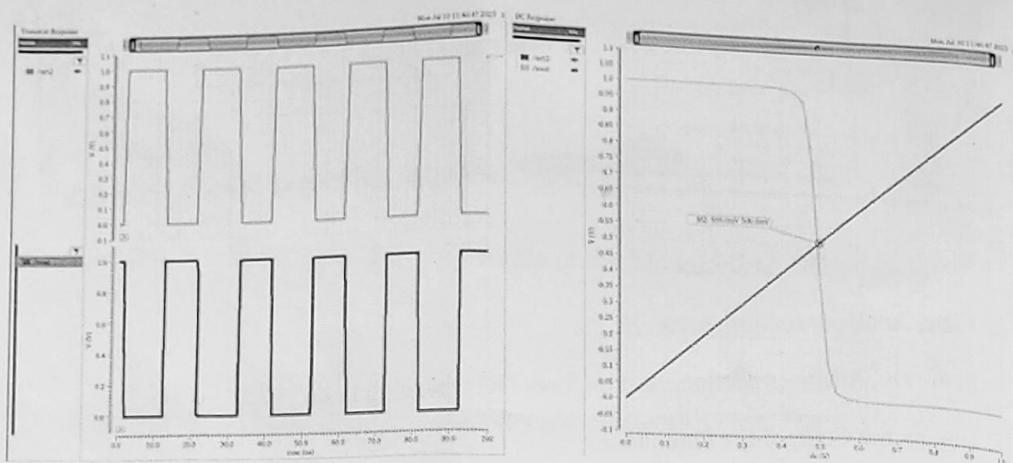
## Selecting Outputs for Plotting

- Execute Outputs – To be plotted – Select on Schematic in the simulation window.
- Follow the prompt at the bottom of the schematic window. Click on output net **Vout**. input net **Vin** of the Inverter. Press ESC with the cursor in the schematic after selecting it.

## Running the Simulation



1. Execute **Simulation – Netlist and Run** in the simulation window to start the Simulation or the icon, this will create the netlist as well as run the simulation.
2. When simulation finishes, the Transient, DC plots automatically will be popped up along with log file.



Result: Note down the operating point

Expected operating point: (500mV, 500mV)

Optional: calculate the delay with the help of transient response and calculator

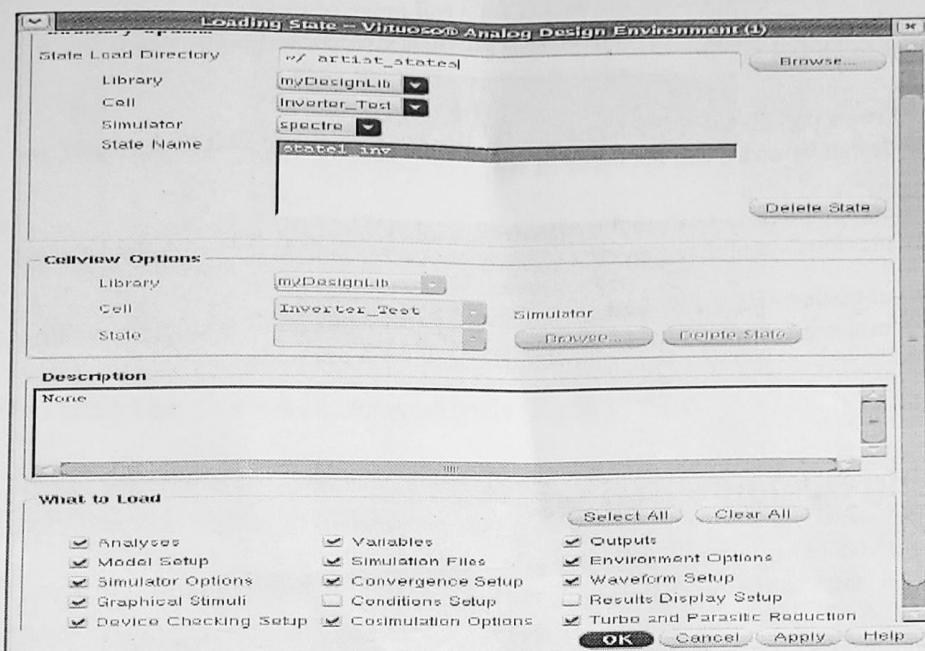
## Saving the Simulator State

We can save the simulator state, which stores information such as model library file, outputs, analysis, variable etc. This information restores the simulation environment without having to type in all of setting again.

1. In the Simulation window, execute **Session – Save State**. The Saving State form appears.
2. Set the **Save as** field to **state1\_inv** and make sure all options are selected under what to save field.
3. Click **OK** in the saving state form. The Simulator state is saved.

## Loading the Simulator State

1. From the ADE window execute Session – Load State.
2. In the Loading State window, set the State name to state1\_inv as shown



3. Click OK in the Loading State window.

## EXPERIMENT NO.2- INVERTER- Parametric analysis

### Parametric Analysis

Parametric Analysis yields information similar to that provided by the Spectre® sweep feature, except the data is for a full range of sweeps for each parametric step. The Spectre sweep feature provides sweep data at only one specified condition.

You will run a parametric DC analysis on the wp variable, of the PMOS device of the Inverter design by sweeping the value of wp.

Run a simulation before starting the parametric tool. You will start by loading the state from the previous simulation run.

Run the simulation and check for errors. When the simulation ends, a single waveform in the waveform window displays the DC Response at the Vout node.

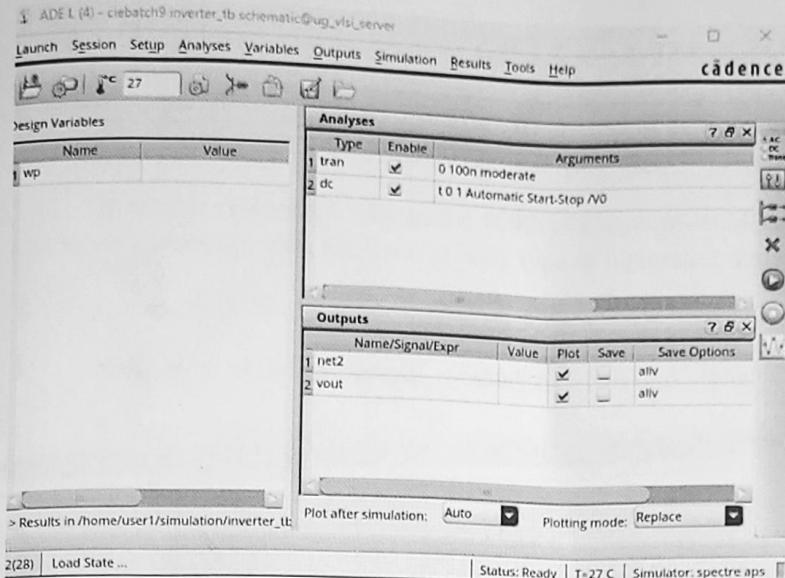
### Setting Design Variables

Set the values of any design variables in the circuit before simulating. Otherwise, the simulation will not run.

1. In the Simulation window, click the **Edit Variables** icon.  
The Editing Design Variables form appears.



2. Click **Copy From** at the bottom of the form.  
The design is scanned and all variables found in the design are listed.  
In a few moments, the wp variable appears in the Table of Design variables section.



## Starting the Parametric Analysis Tool

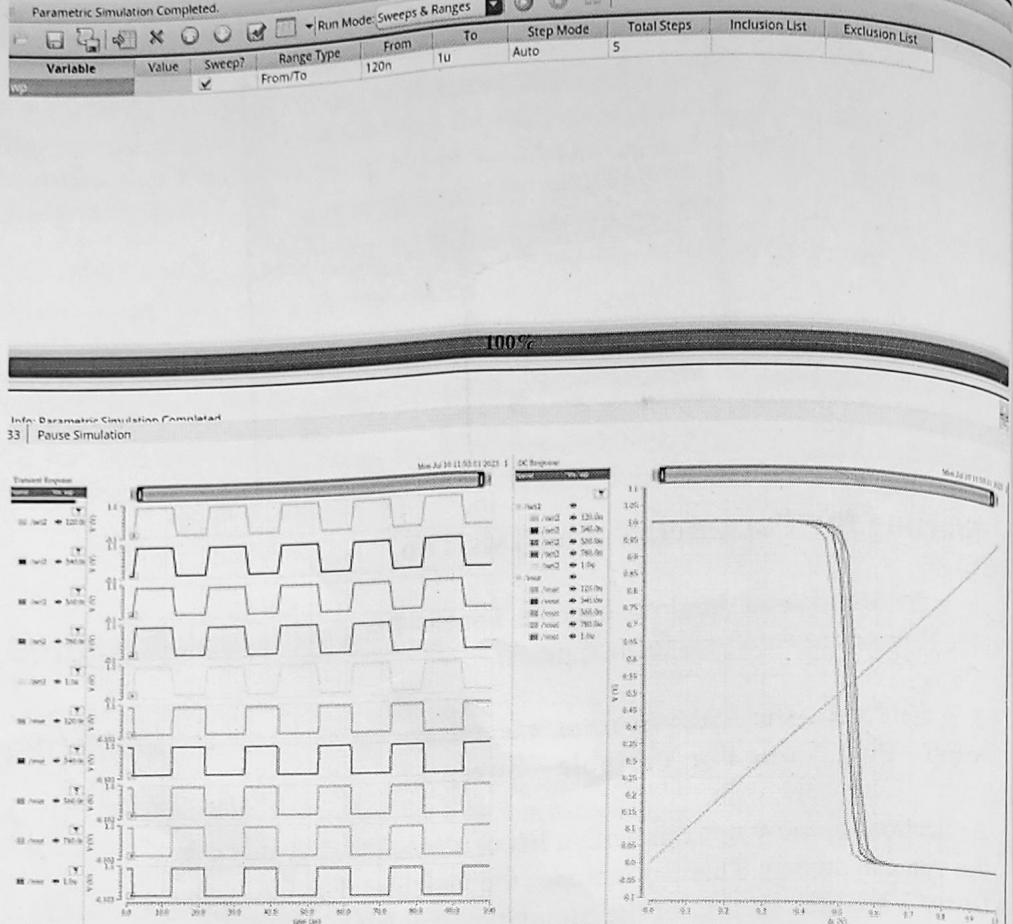
1. In the Simulation window, execute **Tools—Parametric Analysis**. The Parametric Analysis form appears.
2. In the Parametric Analysis form, execute **Setup—Pick Name For Variable—Sweep 1**.

A selection window appears with a list of all variables in the design that you can sweep. This list includes the variables that appear in the Design Variables section of the Simulation window.

3. In the selection window, double click left on **wp**. The Variable Name field for Sweep 1 in the Parametric Analysis form is set to **wp**.
4. Change the Range Type and Step Control fields in the Parametric Analysis form as shown below:

File Analysis Help

Parametric Simulation Completed.



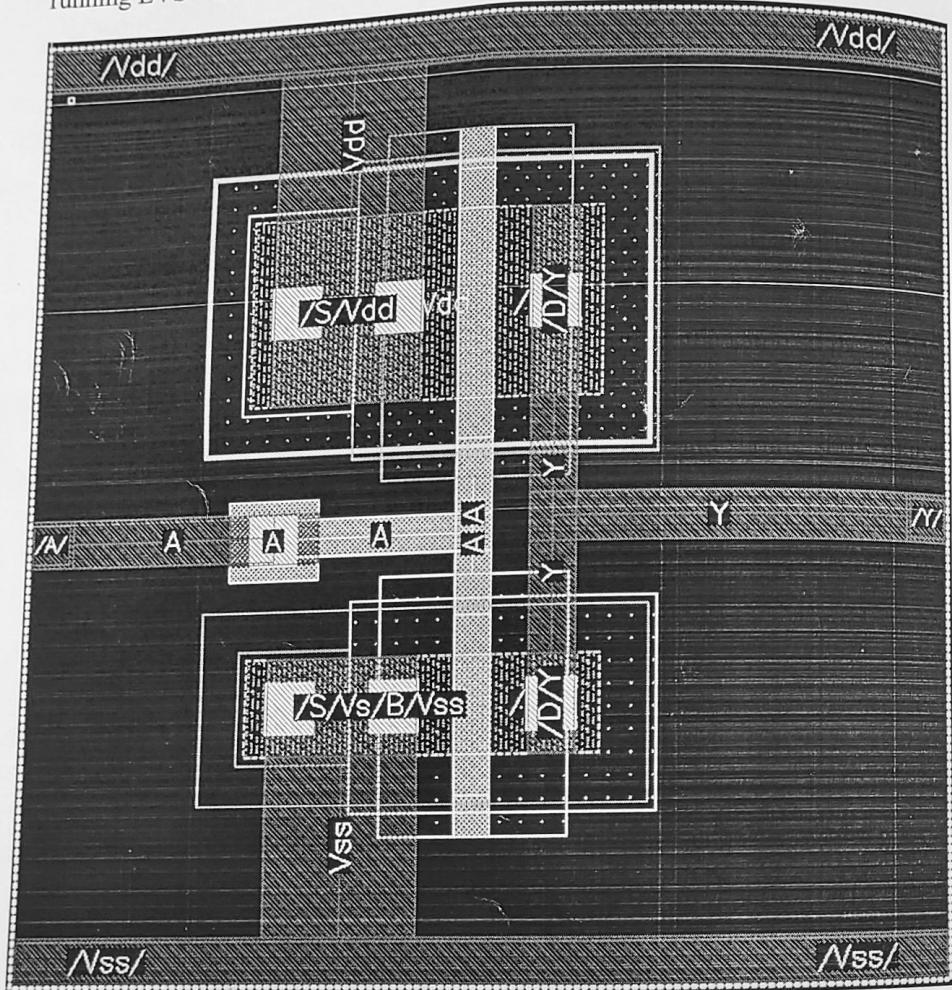
**Result:** Note the shift in the transfer curve and changes in the operating point (use markers)

## EXPERIMENT NO. 3- INVERTER- Layout (DRC and LVS check)

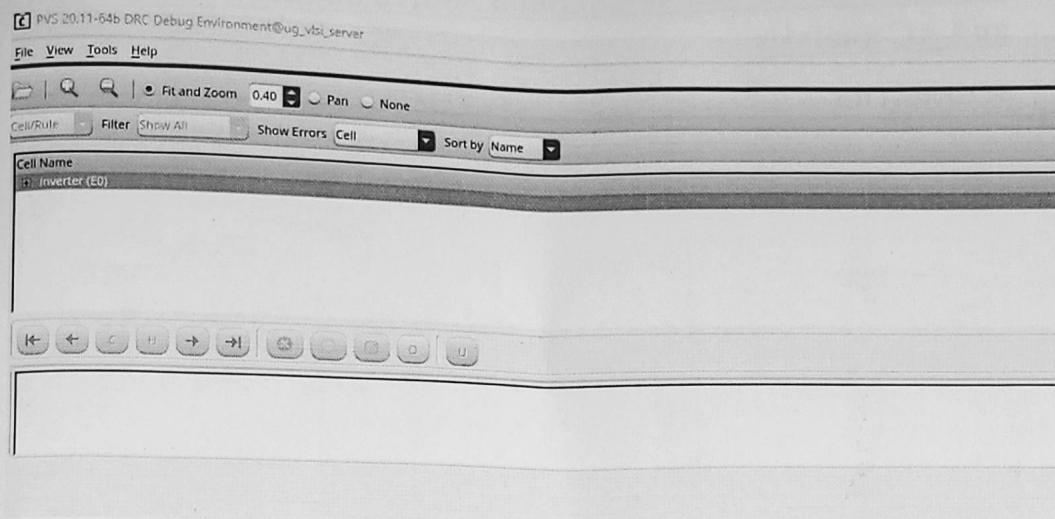
### Steps:

1. In inverter schematic change the width of the pmos to 240nm and right click on pmos and nmos go to properties and change body type to integrated, Launch → Layout XL
2. Connectivity -> generate → all from source
3. Shift +F to view the internal structure of nmos and pmos
4. Select poly from layer window and go to Create → shape → rectangle connect the gates of pmos and nmos
5. Create → via → select M1\_PO and place it between pmos and nmos
6. Select metal1 from layer window Press p on keyboard or create → shape → path connect vin/A pin to via and Select poly from layer window Press p on keyboard and connect the gates with via
7. Select metal1 from layer window Press p on keyboard connect drains of pmos and nmos and connect it in turn to Y/vout
8. Select place → pin placement, select Vdd change edge to top click on apply and click on HRail
9. Select place → pin placement, select Vss change edge to bottom click on apply and click on HRail
10. Select metal1 from layer window Create → wiring → wire, connect source and body of pmos which is integrated to Vdd and connect source and body of nmos which is integrated to Vss
11. Go to create → pin, click on create label and type Vin Vdd Vss Vout (Give the names same as in schematic), click on options and change the height to 0.12, change layer name and layer purpose to same as pin, click on ok
12. According to the sequence click on the appropriate pins on the layout and create a small rectangle on it so that the pins are labelled
13. Save the layout
14. In order to check the layout, Design Rule Check (DRC) and Layout versus Schematic check (LVS) is carried out. Click on PVS → select Run DRC
15. In Run directory choose the path where the current layout file is saved

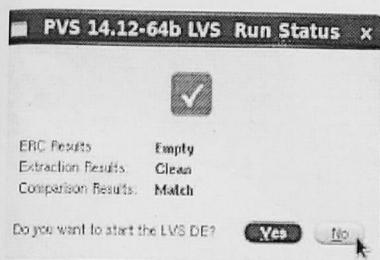
16. Click on Rules-->technology mapping file--->browse-->select gpdk045\_v6\_0->pvttech.lib
17. Select gpdk045\_pvs in the dropdown under Technology, Rule set-->default
18. Select DRC DE in the bottom left corner, click on submit, after the run results will be displayed
19. For LVS check Click on PVS--> Run LVS, follow the same steps as DRC except selecting DRC DE
20. There should not be any errors after running DRC and should show match after running LVS



No DRC errors:



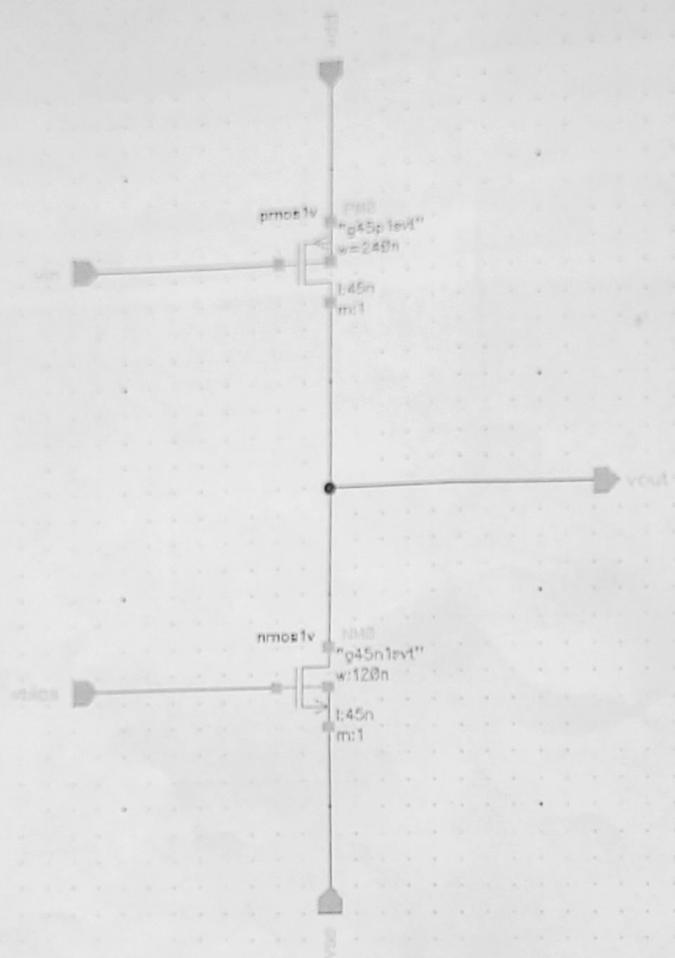
LVS results:



Note: procedure for rest of the experiments are same as inverter, expect for changes in parameters specified in ADE L

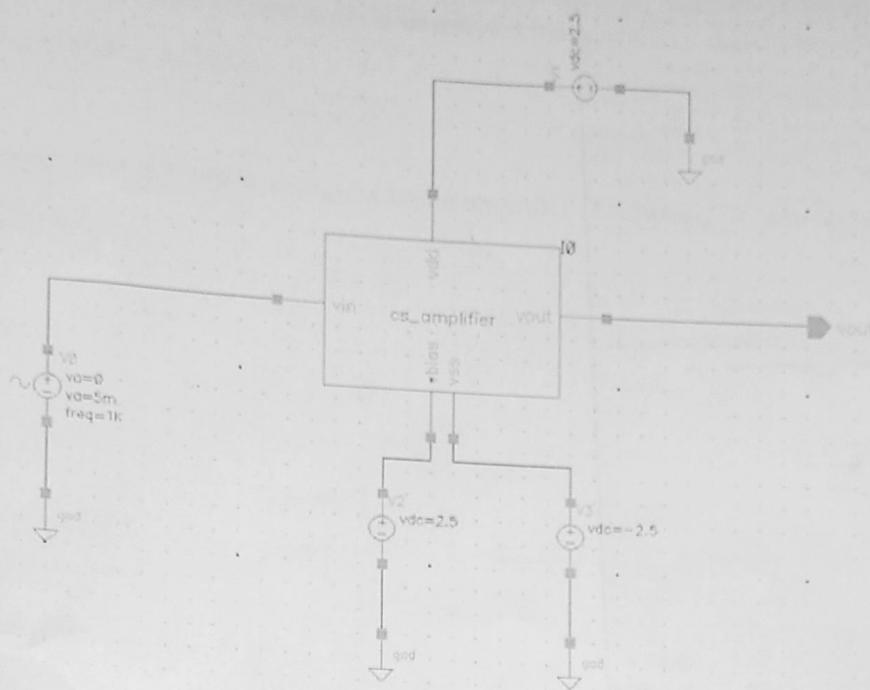
# EXPERIMENT NO. 4- Common Source amplifier- Transient, DC and AC analysis

## SCHEMATIC:



Check and save and create symbol

## TEST BENCH:



Library name	Pin name	Cell Name	Properties/comments
analogLib	vdd	Vdc	DC voltage = 2.5V
analogLib	vss	Vdc	DC voltage = -2.5V
analogLib	vin	Vsin	AC magnitude=1 Amplitude = 5m Frequency = 1K Hz
analogLib	vbias	Vdc	DC voltage = 2.5V/ 1.1V

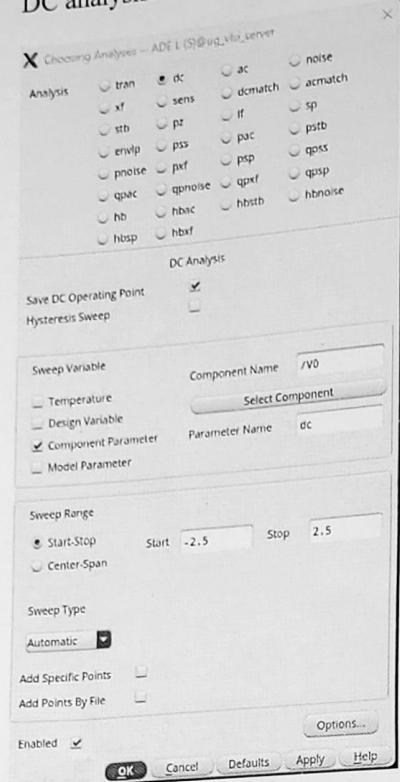
Launch → ADE L → Analysis :

Transient:

Stop time = 5m

Check on moderate

## DC analysis:

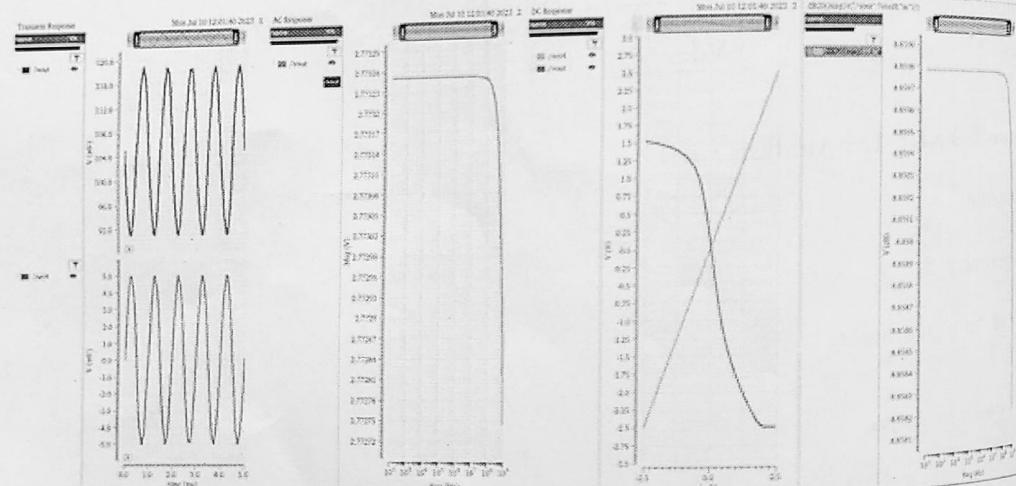


## AC analysis:

Frequency: Start 100 Stop: 1G

Sweep type: Logarithmic, Points per decade: 20, Outputs → to be plotted → select on design, click on input and output wires (net)

Apply → Netlist and Run



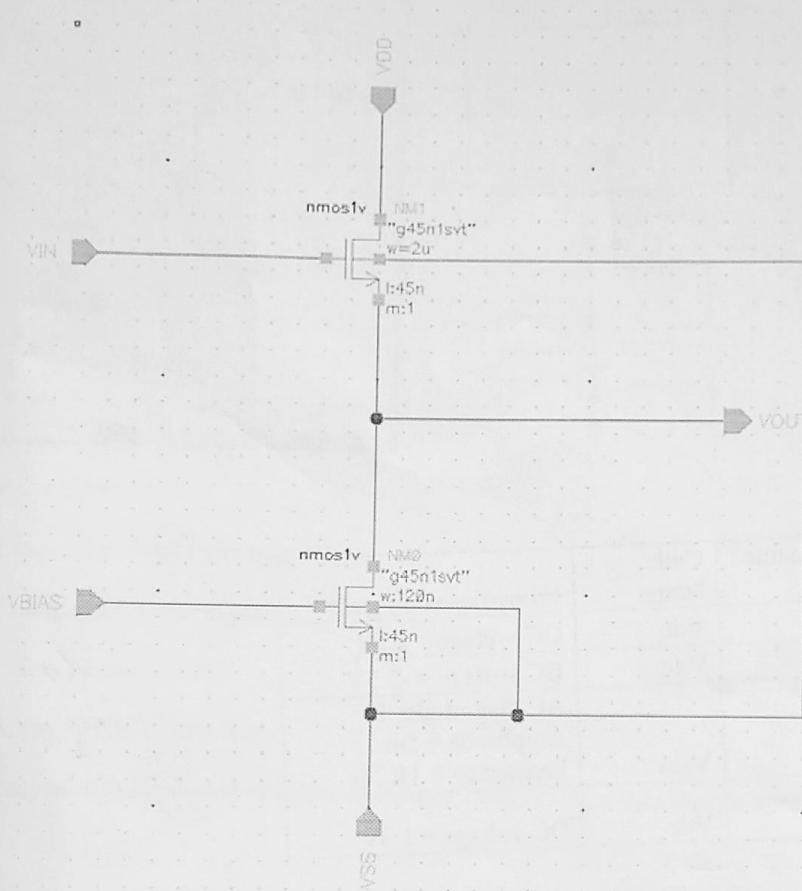
Converting gain to decibel:

Select the ac response, go to tools → calculator → under all functions select dB20, options wave and new sub-window needs to be selected → Evaluate

Expected gain: 8.85dB

## EXPERIMENT NO. 5- Common Drain amplifier- Transient, DC and AC analysis

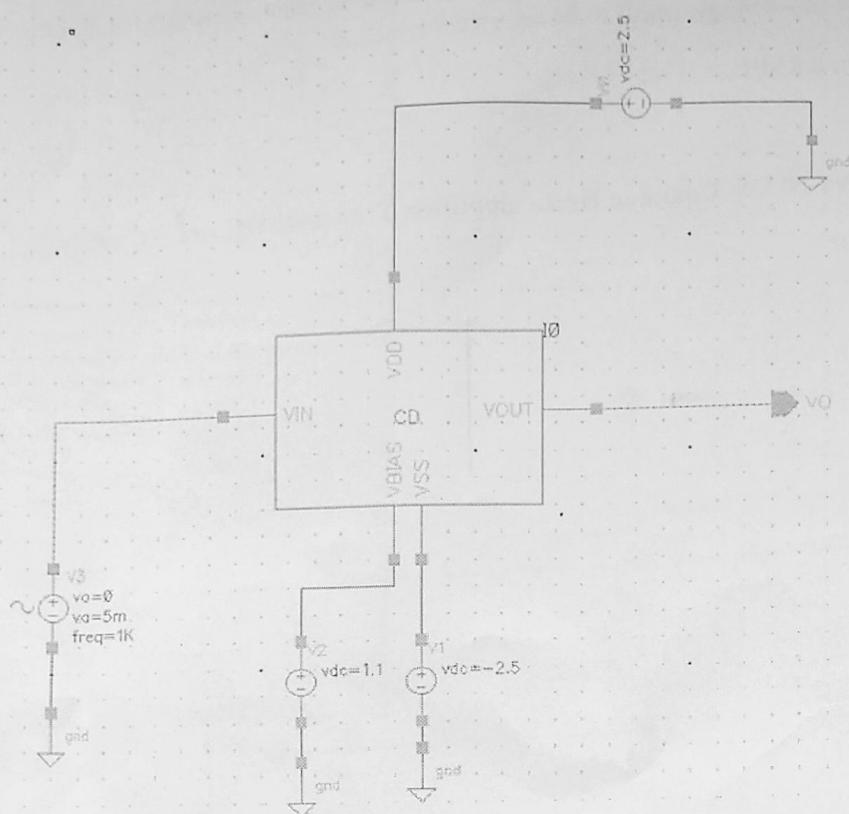
SCHEMATIC:



Note: aspect ratios can be changed to check the impact on gain

**Check and save and create symbol**

## TEST BENCH:



Library name	Pin name	Cell Name	Properties/comments
analogLib	vdd	Vdc	DC voltage = 2.5V
analogLib	vss	Vdc	DC voltage = -2.5V
analogLib	vin	Vsin	AC magnitude=1 Amplitude = 5m Frequency = 1K Hz
analogLib	vbias	Vdc	DC voltage = 1.1V

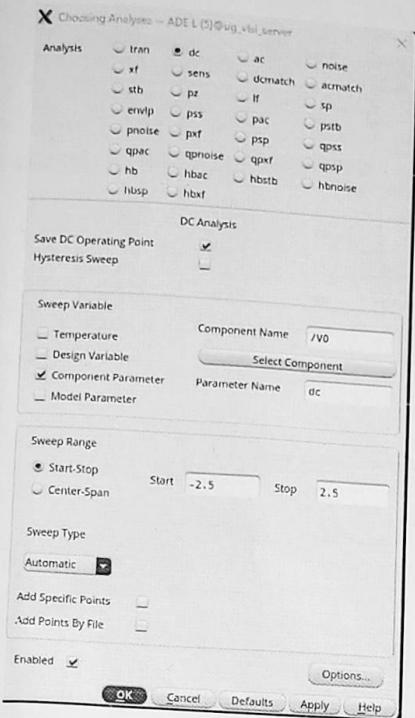
**Launch → ADE L → Analysis :**

Transient:

Stop time = 5m

Check on moderate

## DC analysis:



## AC analysis:

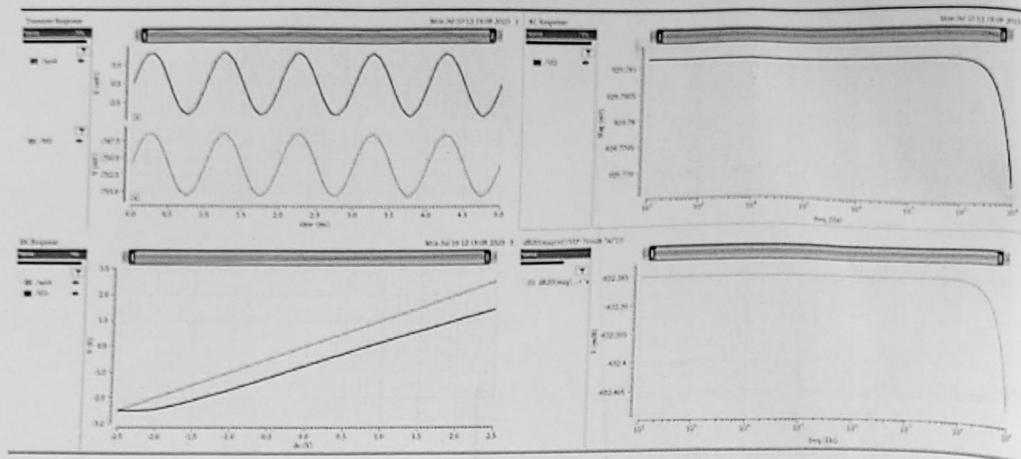
Frequency: Start 100 Stop: 1G

Sweep type: Logarithmic

Points per decade: 20

Apply → Netlist and Run

Outputs → to be plotted → select on design, click on input and output wires (net)

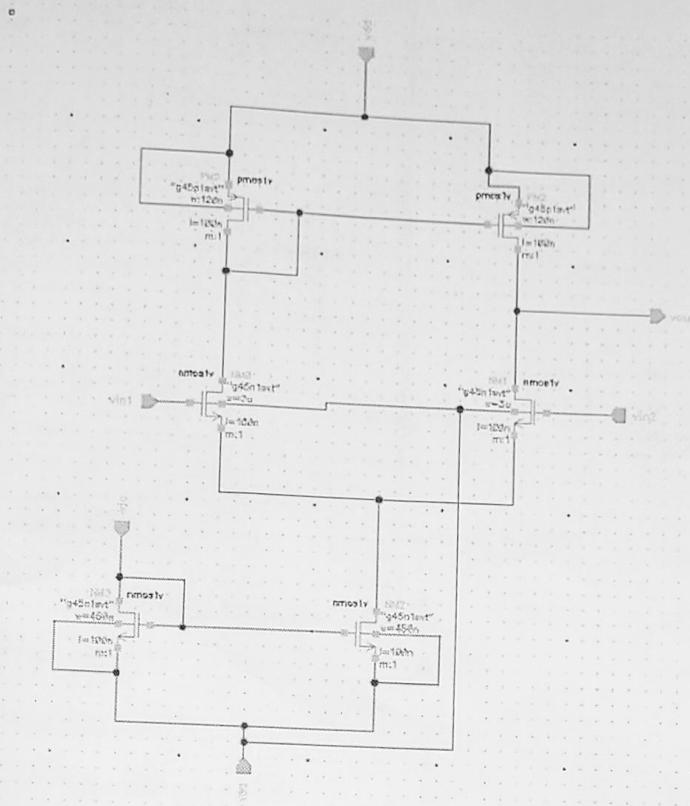


Results: Note down the gain

Expected gain with the given aspect ratio in the schematic =  $-0.633\text{dB}$  (Vout of 929.7mV, i.e. gain of 0.929)

## EXPERIMENT NO. 6- Differential amplifier- Transient, DC and AC analysis

SCHEMATIC:



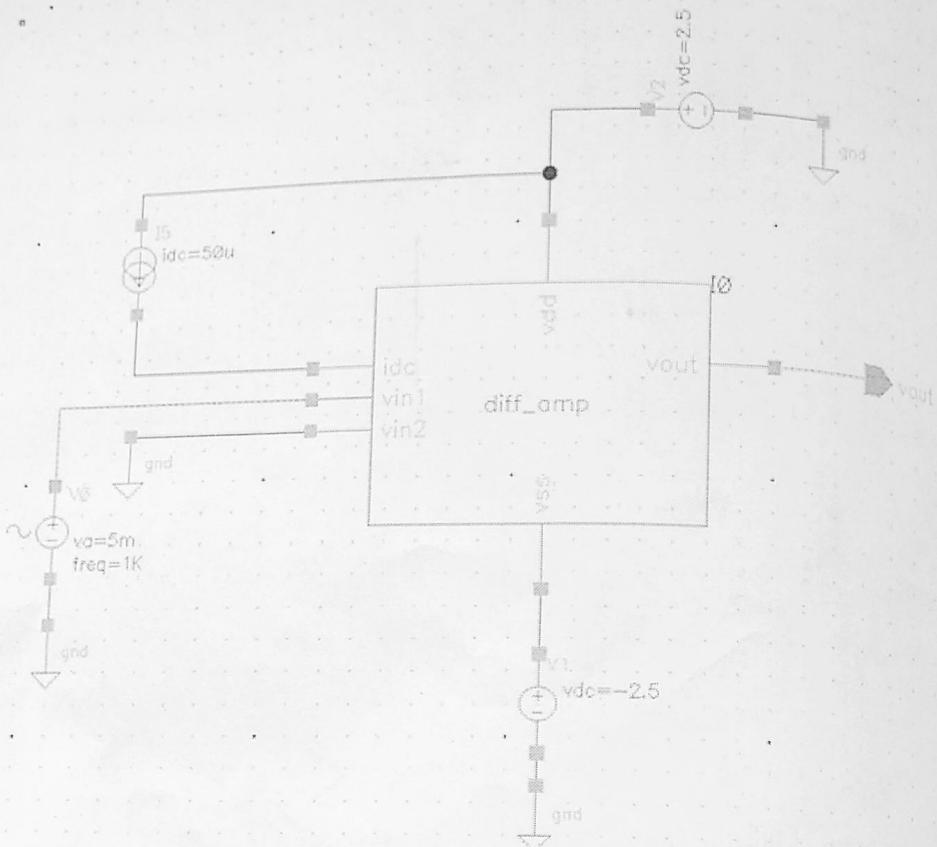
Library name	Position and	Cell Name	Properties/comments
gdk045	Top 2 pmos	pmos1v	W=120n, L=100n
gdk045	Middle 2 nmos	nmos1v	W=3u, L=100n
gdk045	Bottom 2 nmos	nmos1v	W=450n, L=100n

Note that aspect ratios of the MOSFETs can be changed for better gain

**Check and save and create symbol**

## TEST BENCH:

Differential mode:



Library name	Pin name	Cell Name	Properties/comments
analogLib	vdd	Vdc	DC voltage = 2.5V
analogLib	vss	Vdc	DC voltage = -2.5V
analogLib	Vin1	Vsin	AC magnitude=1 Amplitude = 5m Frequency = 1K Hz
analogLib	Idc	idc	DC current = 50u A

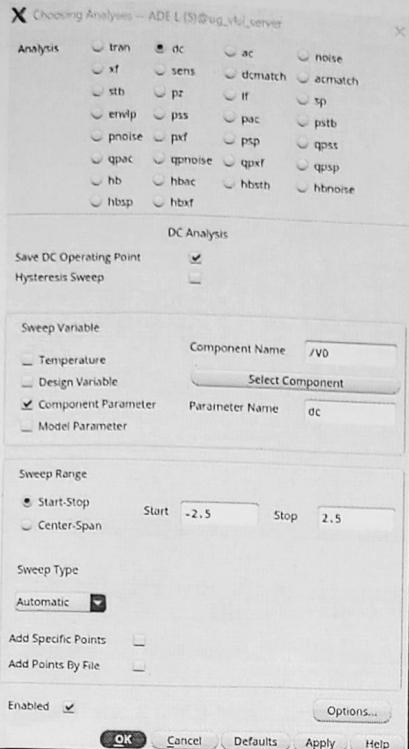
Launch → ADE L → Analysis :

Transient:

Stop time = 5m

Check on moderate

## DC analysis:



## AC analysis:

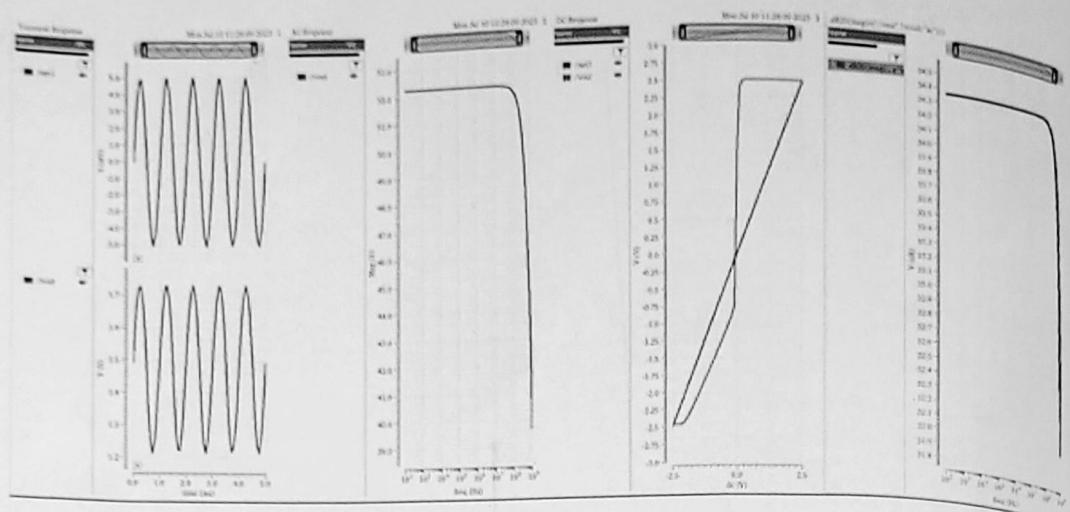
Frequency: Start 100 Stop: 1G

Sweep type: Logarithmic

Points per decade: 20

Apply → Netlist and Run

Outputs → to be plotted → select on design, click on input and output wires (net)

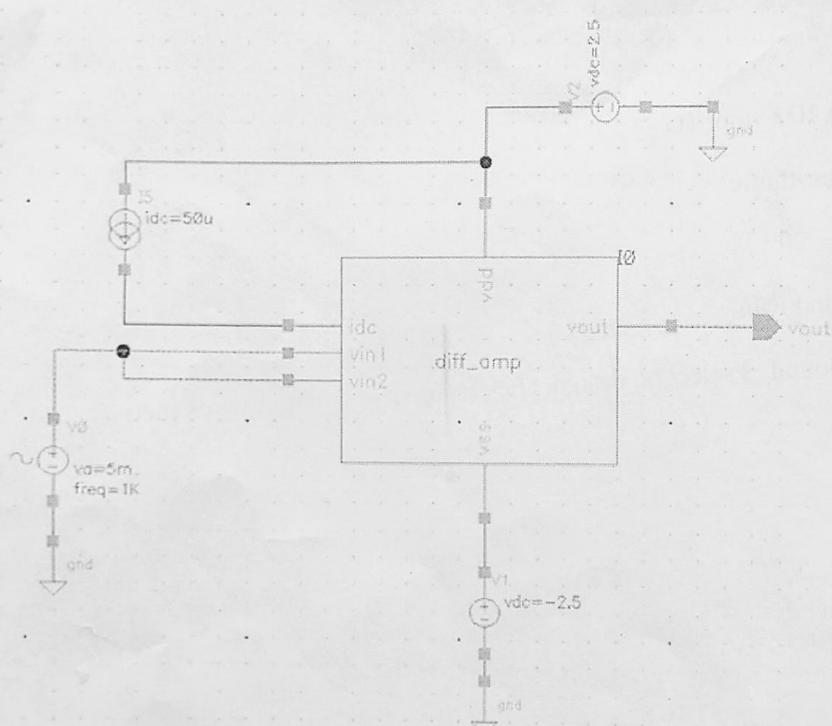


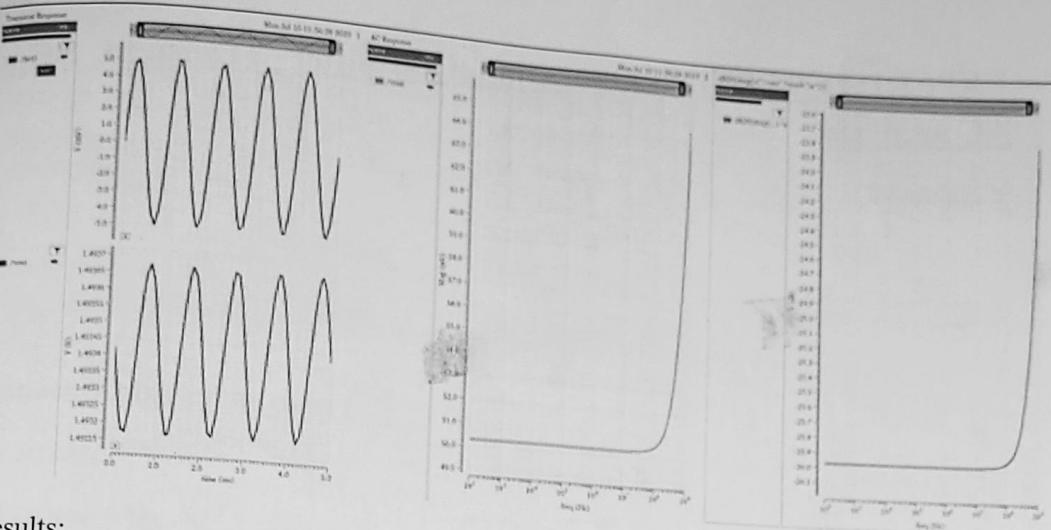
Results:

Note down the differential gain

Expected gain with the given aspect ratio in the schematic ( $A_d$ ) = 34.3dB

**Common mode:**





## Results:

Note down the common mode gain

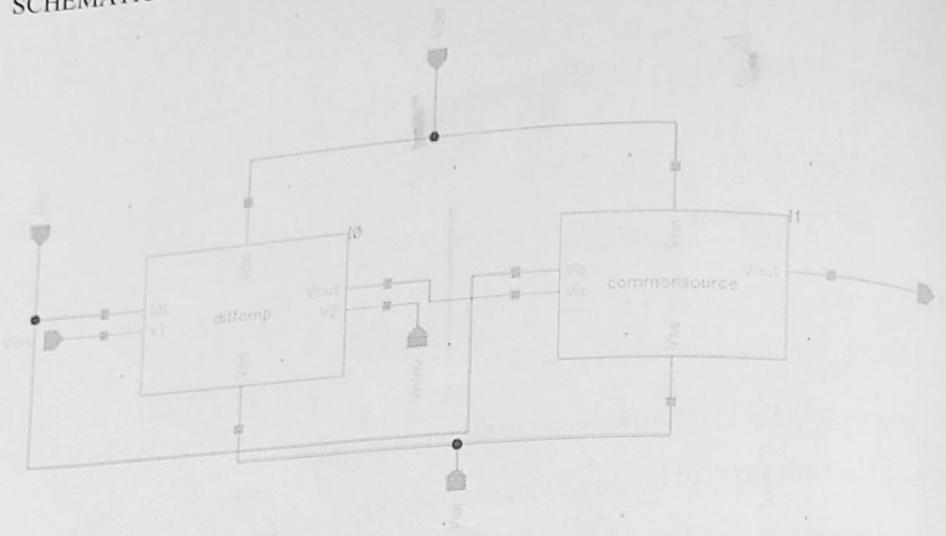
Expected gain with the given aspect ratio in the schematic ( $A_c$ ) = -25.67dB

$$CMRR = 20 \log(Ad/Ac) = 20 \log Ad - 20 \log(Ac) = 60\text{dB}$$

Change the aspect ratios and re-run

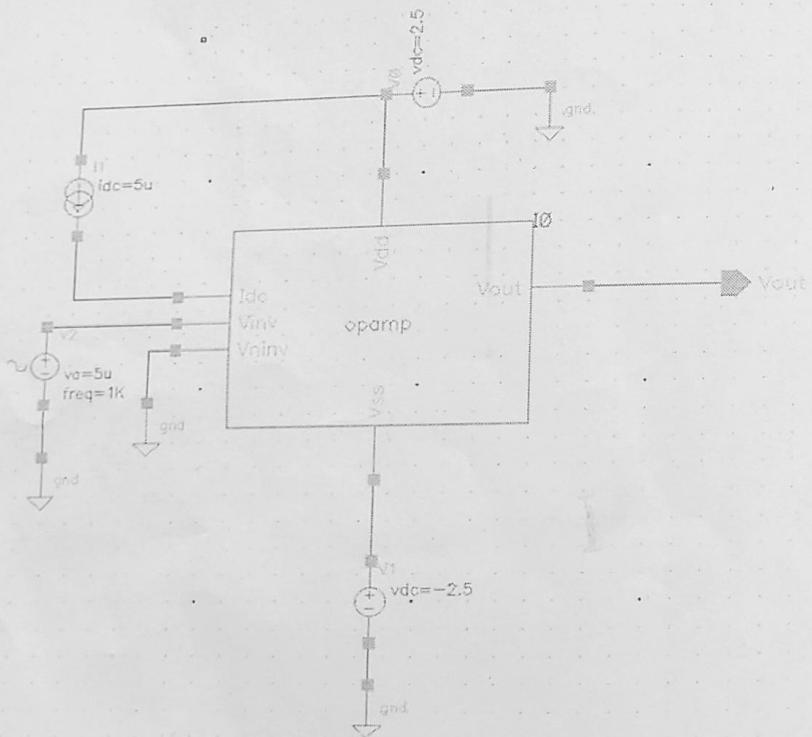
# EXPERIMENT NO. 7- Operational amplifier- Transient, DC and AC analysis

SCHEMATIC:



Check and save and create symbol

TEST BENCH:



Library name	Pin name	Cell Name	Properties/comments
analogLib	vdd	Vdc	DC voltage = 2.5V
analogLib	vss	Vdc	DC voltage = -2.5V
analogLib	Vin1	Vsin	AC magnitude=1 Amplitude = 5u Frequency = 1K Hz
analogLib	Idc	idc	DC current = 5u A

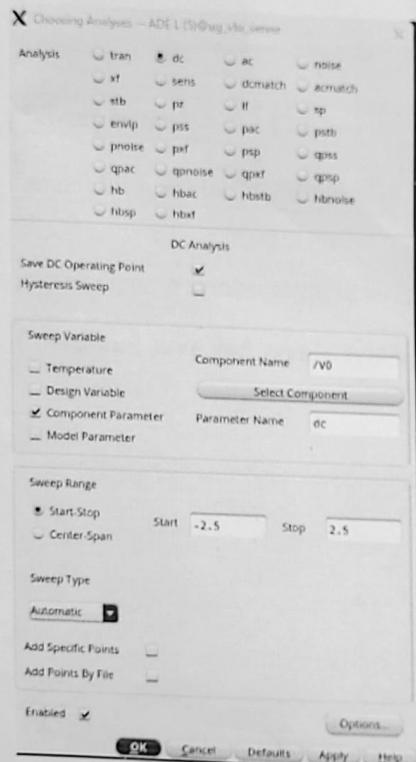
## Launch → ADE L → Analysis :

Transient:

Stop time = 5m

Check on moderate

DC analysis:



AC analysis:

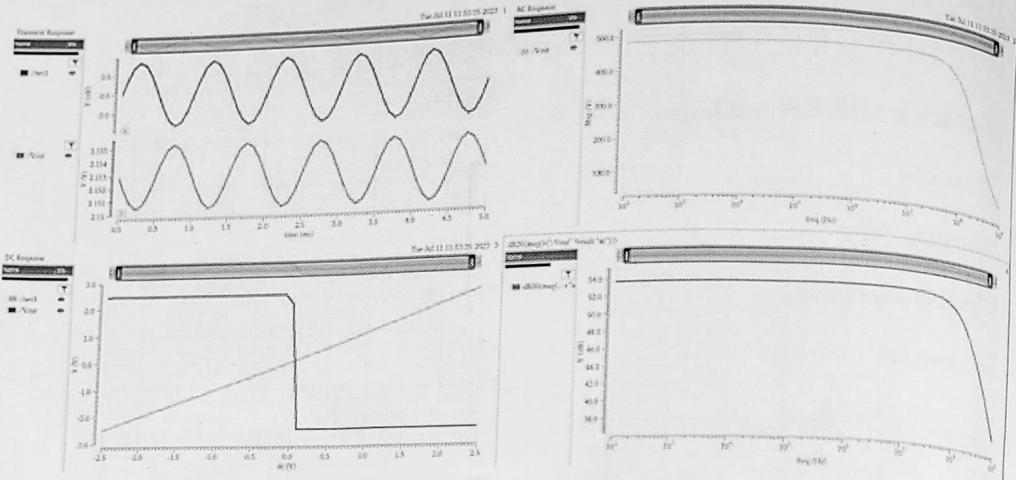
Frequency: Start 100 Stop: 1G

Sweep type: Logarithmic

Points per decade: 20

Outputs → to be plotted → select on design, click on input and output wires (net)

Apply → Netlist and Run



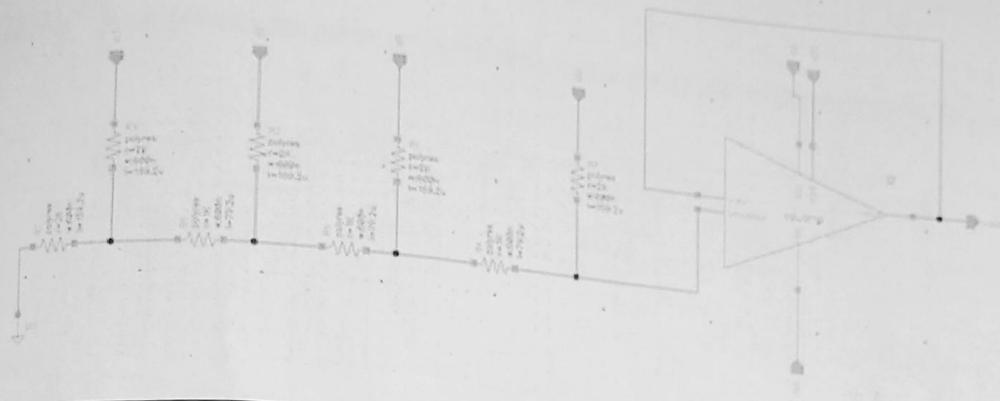
Results:

Expected gain with the given aspect ratio in the schematic = 53.69dB

Bandwidth=988.1E6 (988.1 MHz)

# EXPERIMENT NO. 8- R2R DAC- Transient analysis

SCHEMATIC:

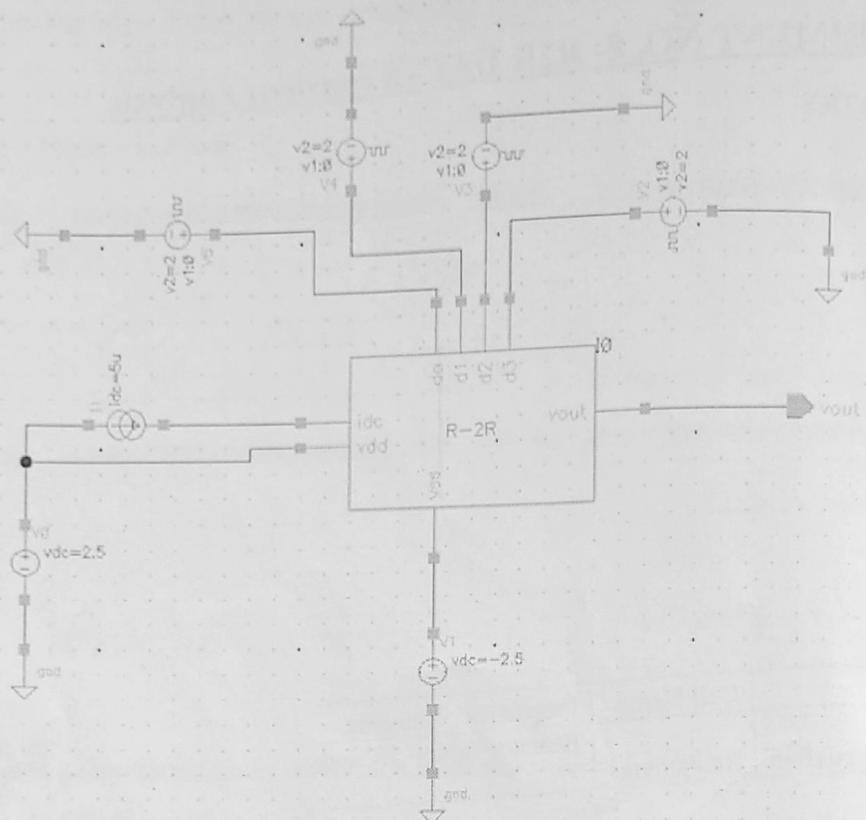


Library name	Cell Name	Properties/comments
analogLib/gpdk045	Res/polyres	Resistor value= 1K and 2K

Import Opamp symbol created in Experiment 7

**Check and save and create symbol**

TEST BENCH:



Library name	Pin name	Cell Name	Properties/comments
analogLib	D0	Vpulse	V1=0, V2=2 V, ton (pulse width)=5ns, period T=10ns
analogLib	D1	Vpulse	V1=0, V2=2 V, ton (pulse width)=10ns, period T= 20ns
analogLib	D2	Vpulse	V1=0, V2=2 V, ton (pulse width)=20ns, period T= 40ns
analogLib	D3	Vpulse	V1=0, V2=2 V, ton (pulse width)=40ns, period T= 80ns
analogLib	vdd	Vdc	DC voltage = 2.5V
analogLib	vss	Vdc	DC voltage = -2.5V
analogLib	Idc	idc	DC current = 5u A

## Launch → ADE L → Analysis :

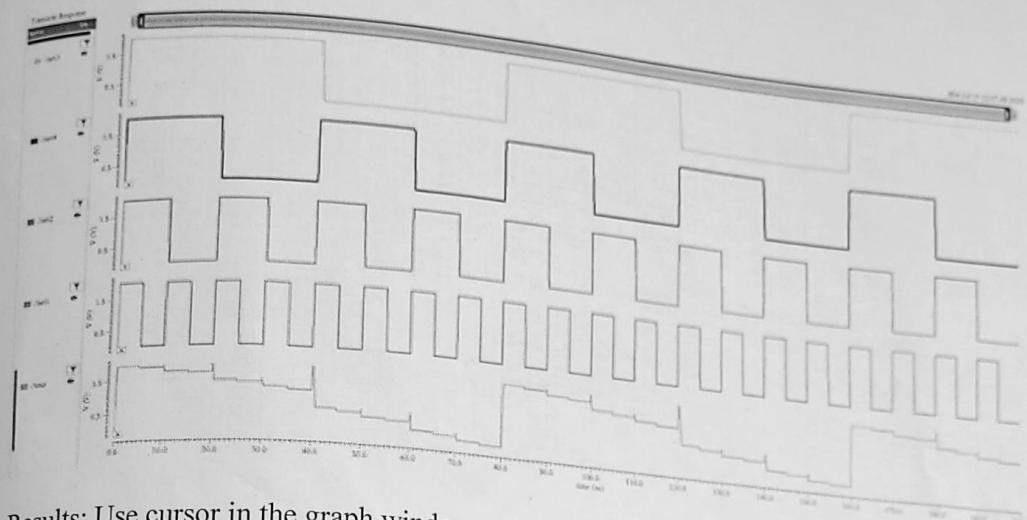
Transient:

Stop time = 200n

Check on moderate

Outputs → to be plotted → select on design, click on input and output wires (net)

Apply → Netlist and Run



Results: Use cursor in the graph window, note down analog values corresponding to each digital combination in the form of a table. Verify the practical values with theoretical formula:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

Where  $V_{out}$  is analog output voltage, D is decimal equivalent of digital input and N is number of bits at the input or resolution of DAC,  $V_{ref}$  is the reference voltage.