NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
CYCLE TEST-2

Subject Code/ Name: CSPC34/ Computer Organization **Date: 6/ 11/ 2023**
Marks: 20 **Time: 11 AM – 12 PM**

Answer all the Questions

1. Neatly draw the Datapath diagram for the `beq` instruction. Use a pencil and ruler. (5)

2. Calculate (3.41796875*10^-3 + 6.34765625 * 10^-5) by hand, assuming each of the values is stored in the 16-bit half-precision format described ~~in Exercise 3.27~~ (and also described in the text). Assume 1 guard, 1 round bit, and 1 sticky bit, and round to the nearest even. Show all the steps, and write your answer in both the 16-bit floating point format and in decimal. (4)

3. Refer to the following sequence of instructions, and assume that it is executed on a 5-stage pipelined datapath: (2+2)

```
add r5,r2,r1
lw r3,4(r5)
lw r2,0(r2)
or r3,r5,r3
sw r3,0(r5)
```

   a. Draw the pipeline diagram for the above code using `nops`, assuming that there is no forwarding or hazard detection.
   b. If the processor has forwarding, but we forgot to implement the hazard detection unit, what happens when this code executes?

4. Discuss briefly about the Intel FDIV bug. (2)

5. What is the condition that the hazard detection unit in a pipelined processor checks and explain that briefly? (2)

6. With an example illustrate the purpose of using biased notation in the IEEE 754 format. (3)