NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
CYCLE TEST –II

Subject Code/ Name: CSPC34/ Computer Organization **Date: 30/ 11/ 2022**
Marks: 20 **Time: 4 – 5 PM**

Answer all the Questions

1. Perform binary FP multiplication for the numbers 1.05625 x 10^2 and 0.4375 by hand assuming each of the values are stored in the 16-bit half precision format. Use 1 guard, 1 round and 1 sticky bit and round to the nearest even. Show all the steps. (4)
2. With a neat table, show the different steps in the multiplication of 5 and 8. (3)
3. Discuss briefly the different steps in transforming a C program to an executable in main memory. (2)
4. Draw neatly the data path diagram for the MIPS store instruction. Use a pencil and ruler. (4)
5. Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 3 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 4 GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 30% class A, 30% class B, 20% class C, and 20% class D, which implementation is faster? (4)
    1. What is the global CPI for each implementation?
    2. Find the clock cycles required in both cases.
6. Draw the multi-clock cycle diagram for the following instruction sequence with and without the forwarding circuit. (3)

```
or r1, r2, r3
or r2, r1, r4
or r1, r1,r2
```

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END SEMESTER EXAMINATION SUMER REDO 2023

Subject Code/ Name: CSPC34/ Computer Organization **Date:20 / 07/ 2023**
Marks: 40 **Time: ~~2:30 AM–4:30 PM~~** 11:00 AM – 1:00 PM

Answer all the questions

1.

a. Consider the following table: (4)

Processor	Clock rate	# of instructions	Time
A	2 GHz	20 x 10^9	7s
B	1.5 GHz	30 x 10^9	10s
C	3 GHz	90 x 10^9	9s

What is the IPC (Instructions per cycle) of each processor? Which processor has the highest performance?

b. List out the eight great ideas of computer architects. (2)

c. Write short notes on the logical operations in the MIPS ISA. (2)

2.

a. Using a table, calculate 9 divided by 5. You should show the contents of each register on each step. Assume both inputs are unsigned 5-bit integers. (4)

b. Calculate $3.984375 \times 10^{-1} + (3.4375 \times 10^{-1} + 1.771 \times 10^{3})$ by hand, assuming each of the values are stored in the 16-bit half precision. Assume 1 guard, 1 round bit, and 1 sticky bit, and round to the nearest even. Show all the steps, and write your answer in both the 16-bit floating point format and in decimal. (4)

3.

a. Draw the data path diagram for the MIPS `sw` instruction. No need to draw the control unit. You could indicate with inward and out-ward arrows the signals each of the resource which is using it. (4)

b. Consider the following sequence of instructions, and assume that it is executed on a 5- stage pipelined datapath. Draw the pipeline diagram for the execution of these instructions. Explain. (4)

```
add r5,r2,r1
lw r3,4(r5)
lw r2,0(r2)
or r3,r5,r3
sw r3,0(r5)
```

4

a. For a direct mapped cache design with 32-bit address, the following bits of the address are used to access the cache. (1+1+3)

Tag: bits 31-9, index: bits 8-4, offset: bits 3-0

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CYCLE TEST -I

Subject Code/ Name: CSPC34/ Computer Organization **Date:21 / 09/ 2022**
Marks: 20 **Time: 11:00AM–12:00 PM**

Answer all the Questions

1. List out and discuss briefly the eight great ideas invented by computer architects. (3)
2. Translate the following C code to MIPS. Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively. Assume that the elements of the arrays A and B are 4-byte words: (4)

```
while (f==g) A[f] = B[f] + h
```

3. For the register values shown above, what is the value of $t2 for the following sequence of instructions? Assume $t0 as holding the value 0xABCDEFAA (2)

```
srl $t2, $t0, 4
andi $t2, $t2, 0xEEEF
```

4. Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 3.5 GHz and CPIs of 1, 2, *<last digit of your roll_no>*, and 3, and P2 with a clock rate of 3 GHz and CPIs of 1, *<second largest digit of your full roll_no.>*, 3, and 2.
   Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 20% class A, 30% class B, 40% class C, and 10% class D, which implementation is faster? (4)
   i. What is the global CPI for each implementation?
   ii. Find the clock cycles required in both cases.
5. What are Pseudoinstructions? Why are they used? Give two examples. (2)
6. Provide the type, assembly language instruction, and binary representation of the instruction described by the MIPS fields: op=0x43, rs=4, rt = 3, constant = 0x55. Explain your answer. (2)
7. Distinguish between server computers and super computers. (2)
8. What are the different kinds of branch instructions in the MIPS ISA? (1)

		A	B	G	P
1	30	1	2	2	3
0.2			2	3	2

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REDO SUMMER 2023
CYCLE TEST -2

Subject Code/ Name: CSPC34/ Computer Organization **Date:18 / 07/ 2023**
Marks: 20 **Time :2:30 – 3:30 PM**

Answer all the Questions

1. Draw the datapath diagram for the lw instruction. (no need to draw the control unit. Just draw the control signals that are needed by the resource) (5)
2. ~~What is an edge-triggered clocking methodology?~~ (2)
3. What are the different stages in pipelining? What do they perform at those stages? (3)
4. What is a control hazard? How will you handle that? Give an example. (3)
5. Consider the following sequence of instructions, and assume that it is executed on a 5- stage pipelined datapath. Draw the pipeline diagram for the execution of these instructions. Explain. (5)

```
add r5,r2,r1
lw r3,4(r5)
lw r2,0(r2)
or r3,r5,r3
sw r3,0(r5)
```

6. ~~What is the sequence of steps during the execution of an unconditional branch instruction?~~ (2)

$(1.05625 \times 10^1) \times (0.4375)$ 1/2 precision (4)
Multiply, use G, S, R. 16 bits