DEPARTEMNT OF COMPUTER SCIENCE AND ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI-15.
CSPC61 – Embedded Systems Architecture
VI Semester - Section A / Cycle Test 1

Answer ALL Questions

Date: 12.02.2025
Max:Marks: 20

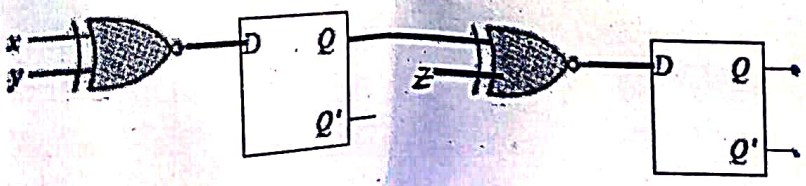
1. Consider the triangle shaped revenue model. Suppose that the product is entered into the market at time 0, with the peak revenue of S units occur at time W, and the product life is 2W. However the launch of the product gets delayed by a time D. For W=13 weeks and D=1 week, what will be the percentage revenue loss due to the delayed launch of the product? (2)

2. Consider the six stage pipeline with stage delays of 35,40,28,42,30 and 38 ns respectively. Is it required to process 5000 data items in the pipeline .What will be the time required to process the data items? (2)

3. Draw the block diagram of a handheld Global Positioning System Receiver. Discuss the function of the various blocks. What type of embedded processor they use? (3)

4. Enumerate the similarities and differences between the Microcontroller and Digital Signal Processor. (3)

5. Determine the configuration bits for the following circuit implementation in a FPGA with I/O. (4)



6. Write a code to compare two registers R0, R1. If R0 < R1, then move R0 to R2. Otherwise move R1 to R2 with and without conditional execution. Also list the advantage of conditional execution. (6)