NATIONAL INSTITUTE OF TECHNOLOGY TIRUCHIRAPPALLI
End Semester Exam – JULY, 2023 SESSION

Department	: Department of Computer Science and Engineering	
Date & Time of End semester	: 06/12/2023 10:00 am to 01:00 pm	Venue: CSE301
Sub Code & Title	: CSPC33 Digital Systems Design	Max. Marks: 80
Faculty Name	: R. Leela Velusamy	

Note to Student: Detailed answer is expected

Answer all questions

1) a) What is the largest binary number that can be expressed with 14 bits? What are the equivalent Decimal, Octal, and hexadecimal numbers? (4)

b) The following decimal numbers are shown in sign-magnitude form: +9,286 and +801. Convert them to signed-10's-complement form and perform the following operations:
(i) (-9,286) + (+801) (ii) (-9,286) + (-801) (4)

c) Implement the Boolean function F = xy + x'y' + y'z with (a) NAND and inverter gates (b) with OR and inverter gates (4)

d) Implement the following four Boolean expressions with three half adders:
D = A ⊕ B ⊕ C E = A'BC + AB'C F = ABC' + (A' + B')C G = ABC (4)

2) a) Draw and explain a BCD adder (4)

b) Derive the Boolean expressions to compare two 4 bit numbers A and B (4)

c) Construct a 5-to-32-line decoder with four 3-to-8 line decoders with enable and a 2-to 4-line decoder. Use block diagrams for the components. (4)

d) Specify the truth table of an octal-to-binary priority encoder. Provide an output V to indicate that at least one of the inputs is present. The input with the highest subscript number has the highest priority. What will be the value of the four outputs if inputs D2 and D6 are 1 at the same time?(4)

3) a) Write the characteristic tables, excitation tables, and characteristic equations for the following flip-flops: T and JK. (6)

b) Draw using NAND gates a SR latch with control input and explain its working using a function table. (5)

c) Derive the (i) state table (ii) state diagram (iii) excitation equations for the circuit in Figure1

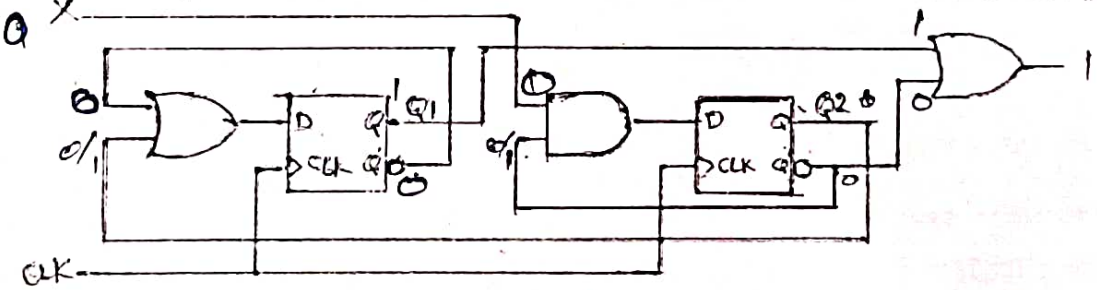

Figure1 (5)

4) a) Design a sequential circuit with two D flip-flops A and B, and one input x. When x = 0, the state of the circuit remains the same. When x =1, the circuit goes through the state transitions from 00 to 11, to 01, to 10, back to 00, and repeats. (6)

b) Draw and explain a 4 bit serial in and parallel out shift register using D flip flops (5)

c) Develop the state diagram for a Mealy state machine that detects the pattern 010. Design a sequential circuit for the Mealy machine using JK flip flops (5)

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5) a) Draw and explain a BCD ripple counter. (6)

b) Draw an equivalent state diagram for the Verilog code given below: (4)

```
module Moore Model (
output [1: 0]    y_out,
input            x_in, clock, reset
);
reg [1: 0]       state;
parameter        S0 = 2'b00, S1 = 2'b01, S2 = 2'b10, S3 = 2'b11;
always @ (posedge clock, negedge reset)
if (reset == 0) state <= S0; // Initialize to state S0
else case (state)
S0: if (~x_in) state <= S1; else state <= S0;
S1: if (x_in) state <= S2; else state <= S3;
S2: if (~x_in) state <= S3; else state <= S2;
S3: if (~x_in) state <= S0; else state <= S3;
endcase
assign y_out = state; // Output of flip-flops
endmodule
```

c) Design a counter with JK flip-flops for the following binary repeated sequence: 0, 1, 3, 7, 4, 6. Show what happens when binary states 010 and 101 are the starting states (6)

*****Best Wishes*****

BC $J_B = A \oplus C$ $J_C = B'$

B' $K_B = C'$ $K_C = 0$