NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
END SEMESTER EXAMINATION DECEMBER 2023

Subject Code/ Name: CSPC34/ Computer Organization **Date:4 / 12/ 2023**
Marks: 50 **Time: 10:00 AM–1:00 PM**

Answer all the questions

1.

a. Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2. (4)

a) Which processor has the highest performance expressed in instructions per second?
b) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
c) We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

b. Write the MIPS code for the following instruction. Assume that i, k and the base address of S are stored in the registers $s1, $s2 and $s3 (3)

```
for (i=0; i < 10; i++)
{
    k++;
    S[i] = S[i] +k;
}
```

c. What is pseudo-direct addressing in MIPS? Give an example. (3)

2.

a. With a neat table show the how the multiplication of the decimal numbers 32 and 3 is done in a computer. Use 6-bit binary digits for both the numbers. (4)

b. Calculate the sum of 2.6125x 10^1 and 4.150390625x 10^-1 by hand, assuming A and B are stored in the 16-bit half precision. Assume 1 guard, 1 round bit, and 1 sticky bit, and round to the nearest even. Show all the steps. (4)

c. Discuss briefly about the Intel FDIV bug. (2)

3.

a. Draw the datapath diagram of the `lw` instruction. (5)

b. Consider the following sequence of instructions: (3)

```
or r1,r2,r3
or r2,r1,r4
or r1,r1,r2
```

Also, assume the following cycle times for each of the options related to forwarding:

Without Forwarding	With Full Forwarding	With ALU-ALU Forwarding Only
250ps	300ps	290ps

What is the total execution time of this instruction sequence without forwarding and with full forwarding? What is the speedup achieved by adding full forwarding to a pipeline that had no forwarding? Explain

c. What is the condition that the hazard detection unit in a pipelined processor checks and explain that briefly? (2)

4.

a. Consider the following sequence of instructions, and assume that it is executed on a 5- stage pipelined datapath: (2+2)

```
add r5,r2,r1
lw r3,4(r5)
lw r2,0(r2)
or r3,r5,r3
sw r3,0(r5)
```

i. If the processor has forwarding, but we forgot to implement the hazard detection unit, what happens when this code executes?

ii. If there is forwarding, for the first five cycles during the execution of this code, specify which signals are asserted in each cycle by hazard detection and forwarding units.

b. What is dynamic branch prediction? How is it advantageous? (3)

c. What are the different steps used in the implementation of the jump instruction? (3)

5.

a. For a direct mapped cache design with 32-bit address, the following bits of the address are used to access the cache. (1+3)

Tag: bits 31-9, index: bits 8-4, offset: bits 3-0

i. How many lines does the cache have?

ii. If starting from power on, the following **byte addressed cache references** are recorded:

0,4,16,140,230,160,1024,30,16,160,3100,180,2180

What is the hit ratio? Show all the steps.

b. 'Increasing associativity requires more comparators and more tag bits per cache block' - explain with a simple example. (2)

c. What is the minimum number of parity bits required to protect a 128-bit word using the SEC code? (2)

d. Consider a SEC code that protects 8-bit words with 4 parity bits. If we read the value 0x375, is there an error? If so, correct the error. (2)