DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY
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CYCLE TEST-2
CSPC51 – COMPUTER ARCHITECTURE

Branch/Semester/Sec : CSE/V/A Time: 10:30 PM to 11.30 PM
Date : 15.10.2024 Max Marks: 20

Answer All Questions

1. a. State the advantages of OOO pipelines over In-order pipelines.

b. Assume a five-stage single-pipeline microarchitecture (fetch, decode, execute, memory, write-back) and the code in the given Figure 1. All ops are one cycle except LW and SW, which are 1 + 2 cycles, and branches, which are 1 + 1 cycles. There is no forwarding. Show the phases of each instruction per clock cycle for one iteration of the loop.

```
Loop: LW    R3,0(R0)
      LW    R1,0(R3)
      ADDI  R1,R1,#1
      SUB   R4,R3,R2
      SW    R1,0(R3)
      BNZ   R4, Loop
```

Figure 1

a. How many clock cycles per loop iteration are lost to branch overhead?

b. Assume a static branch predictor, capable of recognizing a backwards branch in the Decode stage. Now how many clock cycles are wasted on branch overhead?

c. Assume a dynamic branch predictor. How many cycles are lost on a correct prediction?

[1+6=7]

2. a. Discuss the Tomasulo's algorithms & its necessity. Use the hardware configuration and show the disadvantage of it.

b. Suppose the Following instruction sequence is being executed where the system which is able to issue instructions in order but can perform out of order execution, which consists of 3 load units, 3 adder units and 2 multiplier units. The floating point adder unit takes 2 clock cycles, floating point multiplier takes 10 clock cycles and divide operation takes 40 clock cycles. If we use Tomsula's algorithm along with dynamic branch prediction, then find at what cycle the final value of F10 will be available and state the state of the functional units when the DIVD instruction is in execution. Also picturise the states of the reservation station.

```
LD    F6 34+ R2
LD    F2 45+ R3
MULTD F0 F2 F4
SUBD  F8 F6 F2
DIVD  F10 F0 F6
ADDD  F6 F8 F2
```

[2+5=7]

3. Consider the usage of critical word first and early restart on L2 cache misses. Assume a 1 MB L2 cache with 64 byte blocks and a refill path that is 16 bytes wide. Assume that the L2 can be written with 16 bytes every 4 processor cycles, the time to receive the first 16-byte block from the memory controller is 120 cycles, each additional 16-byte block from main memory requires 16 cycles, and data can be bypassed directly into the read port of the L2 cache. Ignore any cycles to transfer the miss request to the L2 cache and the requested data to the L1 cache.

How many cycles would it take to service an L2 cache miss with and without critical word first and early restart?

Do you think critical word first and early restart would be more important for L1 caches or L2 caches, and what factors would contribute to their relative importance?

[3]

4. Now you are designing a write buffer between a write-through L1 cache and a write-back L2 cache. The L2 cache write data bus is 16 B wide and can perform a write to an independent cache address every 4 processor cycles.

What should be the size of each write buffer entry?

What speedup could be expected in the steady state by using a merging write buffer instead of a non-merging buffer when zeroing memory by the execution of 64-bit stores if all other instructions could be issued in parallel with the stores and the blocks are present in the L2 cache?

[3]