National Institute of Technology, Tiruchirappalli

Department of Computer Science and Engineering

Compensatory CYCLE TEST

Computer Architecture

Course/ Branch : B.Tech/ CSE Course Code : CSPC51

Duration : 1 Hour Max Marks : 20

Answer All Questions

1. What are the 4 different types of predictors? Elaborate on their performance in terms of average misprediction rate.
   [4]
2. Assume that in the 5-stage pipeline the longest stage requires 0.8 ns, and the pipeline register delay is 0.1 ns. What is the clock cycle time of the 5-stage pipeline? If the 10-stage pipeline splits all stages in half, what is the cycle time of the 10-stage machine?
   [2]
3. What do you understand by Hardware Based Speculation?
   [2]
4. Disscuss the cache memory optimization techniques in view of reducing the access time.
5. Assume a five-stage single-pipeline microarchitecture (fetch, decode, execute, memory, write-back) and the code is as follows:

```
Loop:  LW    R3,0(R0)
       LW    R1,0(R3)
       ADDI  R1,R1,#1
       SUB   R4,R3,R2
       SW    R1,0(R3)
       BNZ   R4, Loop
```

All ops are one cycle except LW and SW, which are 1 + 2 cycles, and branches, which are 1 + 1 cycles. There is no forwarding. Show the phases of each instruction per clock cycle for one iteration of the loop. How many clock cycles per loop iteration are lost to branch overhead?
[5]

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