EE671: Assignment3

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1 Overview of the experiment

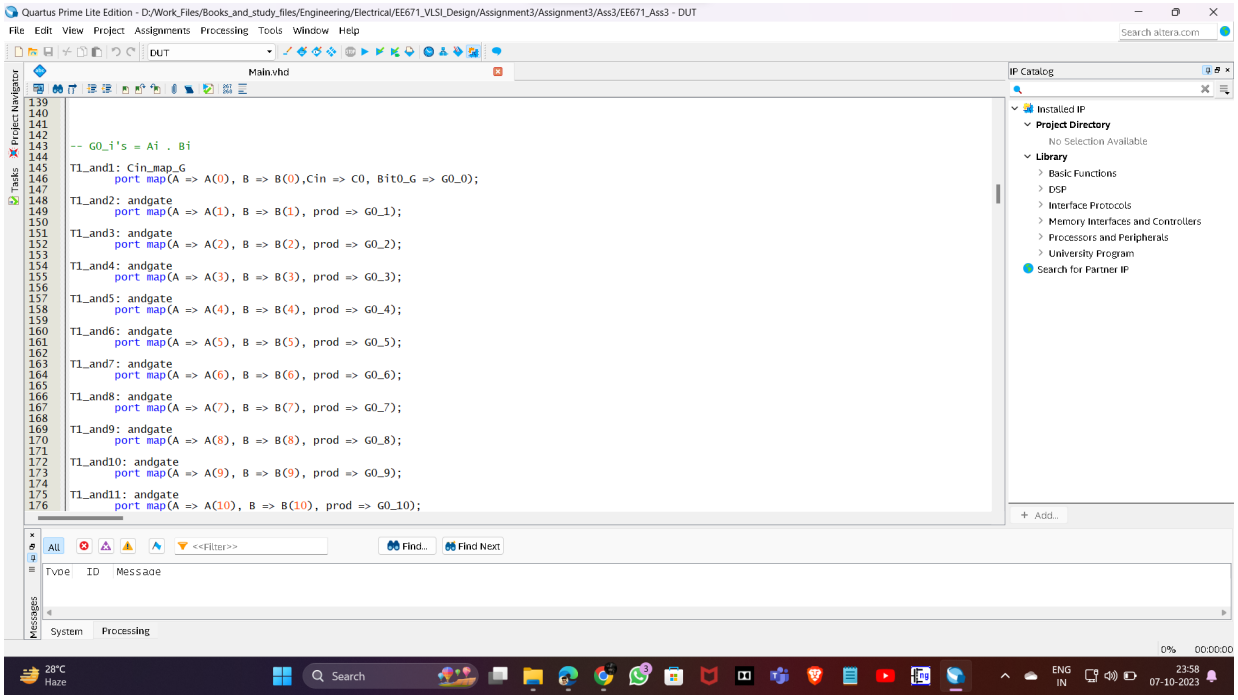
Describing a 32 bit Brent Kung adder in VHDL and simulating it using a test bench. description uses stdlogic types for various signals.

2 design

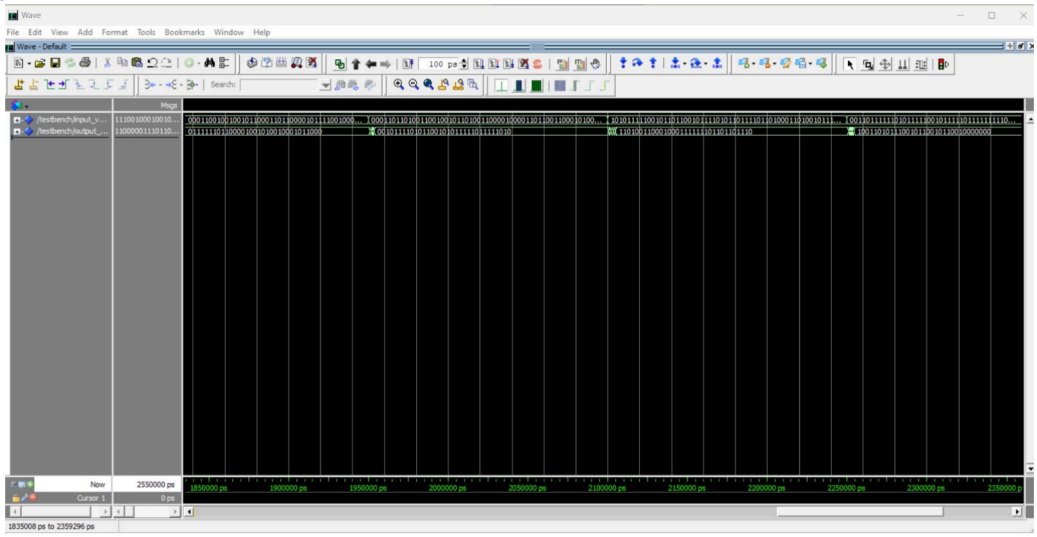
Here, we are given sample code in which we have to modify delay according to our roll numbers. These logic functions are used to determine G, P, final sum and carry outputs.

AND operation delay - 344ps
A+B.C operation delay - 444ps
XOR operation delay - 688ps
A.B+C.(A+B) operation delay - 688ps

```
-- A, B are available

C0 <= Cin;

-------- timestep 1

--P0_i's = Ai + Bi

T1_xor1: xorgate
       port map(A => A(0), B => B(0), uneq => P0_0);

T1_xor2: xorgate
       port map(A => A(1), B => B(1), uneq => P0_1);

T1_xor3: xorgate
       port map(A => A(2), B => B(2), uneq => P0_2);

T1_xor4: xorgate
       port map(A => A(3), B => B(3), uneq => P0_3);

T1_xor5: xorgate
       port map(A => A(4), B => B(4), uneq => P0_4);

T1_xor6: xorgate
       port map(A => A(5), B => B(5), uneq => P0_5);

T1_xor7: xorgate
       port map(A => A(6), B => B(6), uneq => P0_6);

T1_xor8: xorgate
       port map(A => A(7), B => B(7), uneq => P0_7);

T1_xor9: xorgate
       port map(A => A(8), B => B(8), uneq => P0_8);

T1_xor10: xorgate
       port map(A => A(9), B => B(9), uneq => P0_9);
```



Here, I am attaching code snippets of time stamp 1 and 2 showing G0,G1,P0 and P1.



This is my RTL simulation and test cases image. In files section there is Test-bench.vhd, Main.vhd , Gates.vhd and DUT.vhd files