Assignment 4 VLSI

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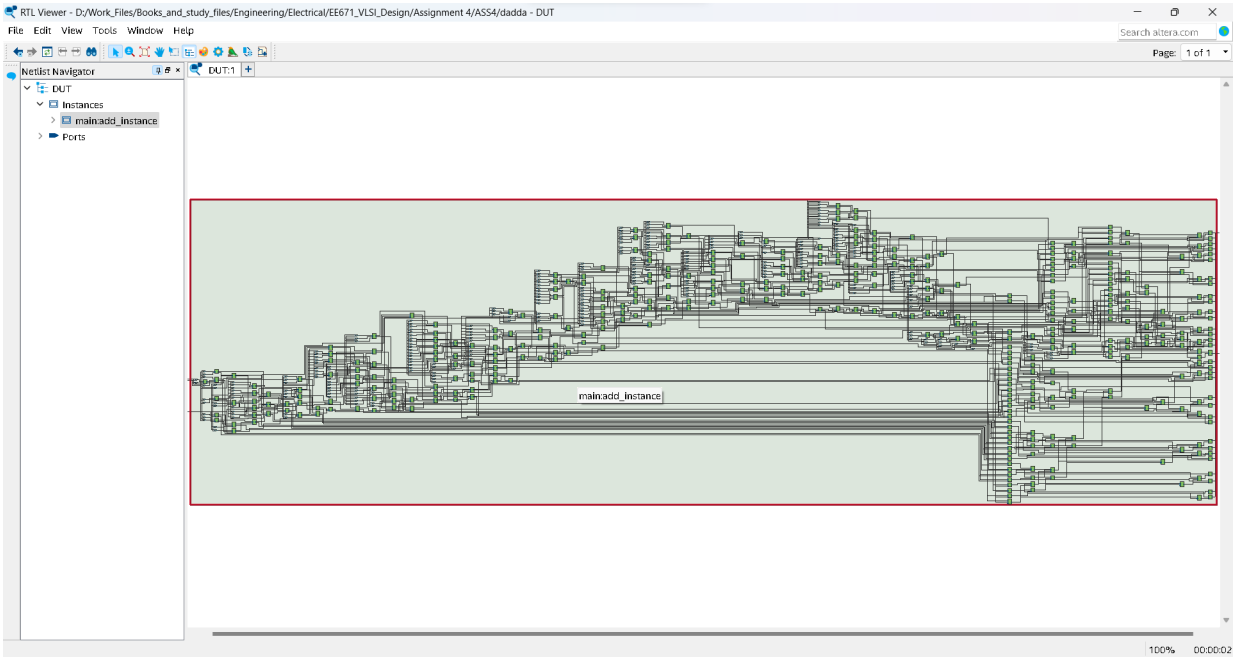
November 2023

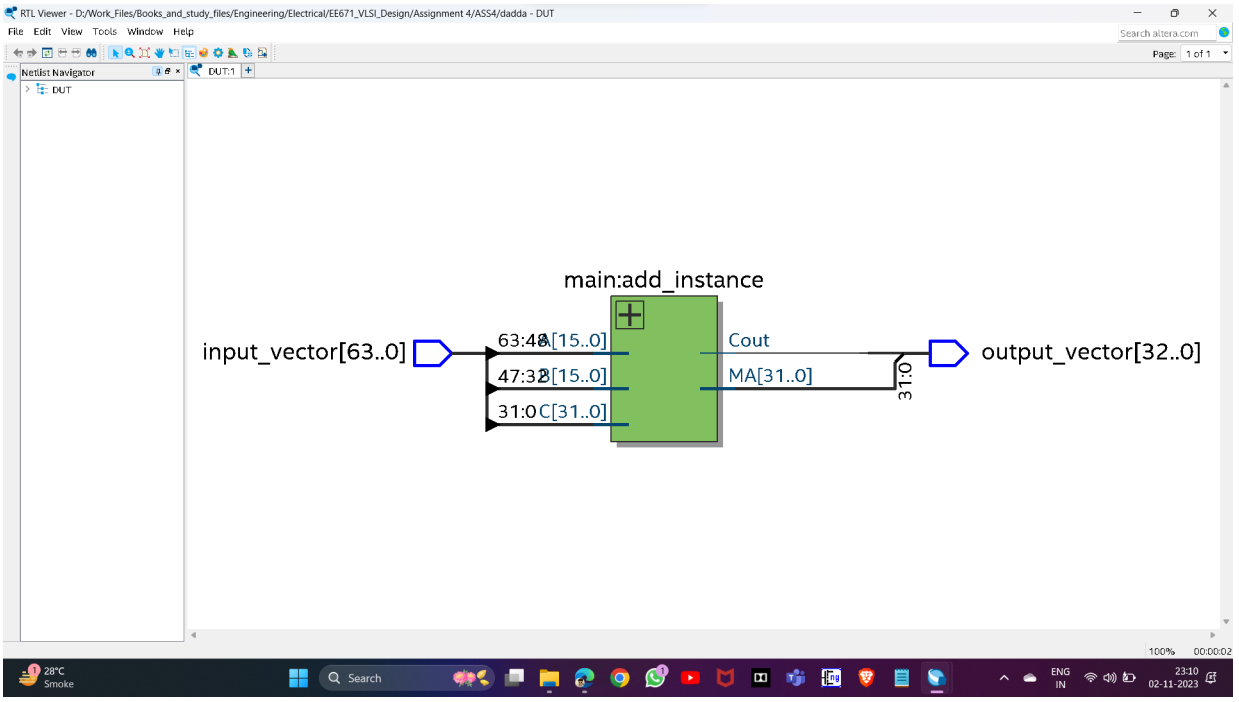
1 Introduction

Multiply-Accumulate circuit using Dadda reduction scheme

We were given two 16-bit input and one 32-bit input for multiplication of the two 16-bit integer followed by addition with the 32-bit integer using the DADDA reduction scheme. Firstly, the two 16-bit input were multiplied using the old conventional method and we got the partial product. We add or place the 32-bit number in the top and assume all the numbers as 32-bit integer. Finally, we have 17rows of 32-bit numbers. According to the algorithm we have to convert the 17 rows into 13 rows using appropriate wires, half adders and full adders. After that we have to convert it into 9 reduction layers followed by 6 reduction and finally into 2 reduction layers. After that we have to use a Bent-Kung adder designed in the last assignment to add the last two reduction layer which gives the final output.

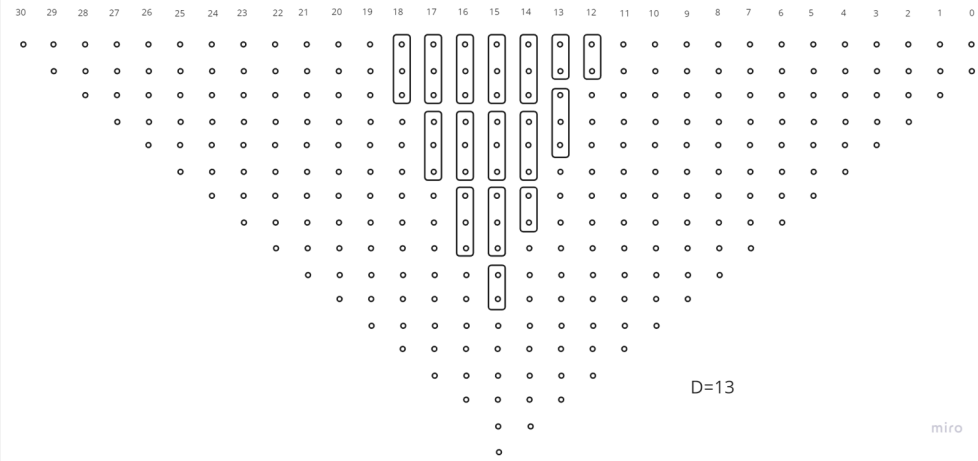


Here is the detailed RTL viewer of the MAC circuit.

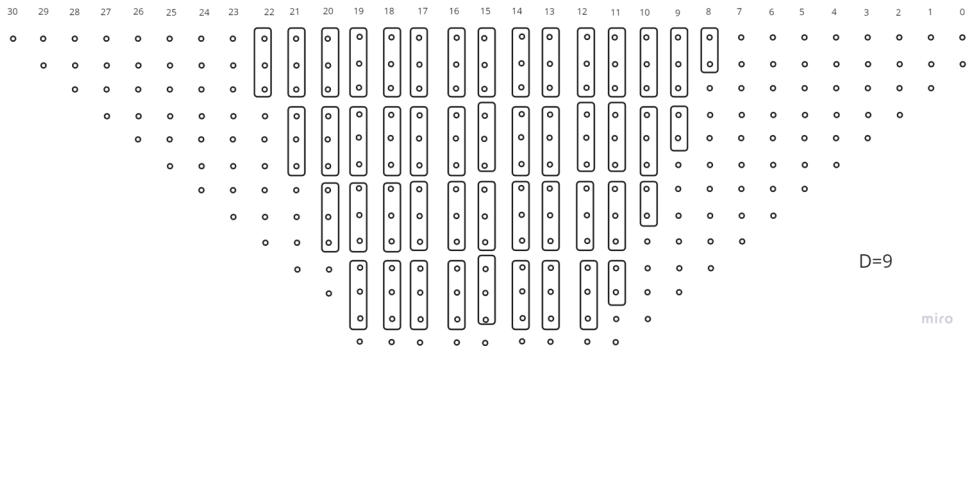


The dot diagram of different reduction layers is mentioned here: -

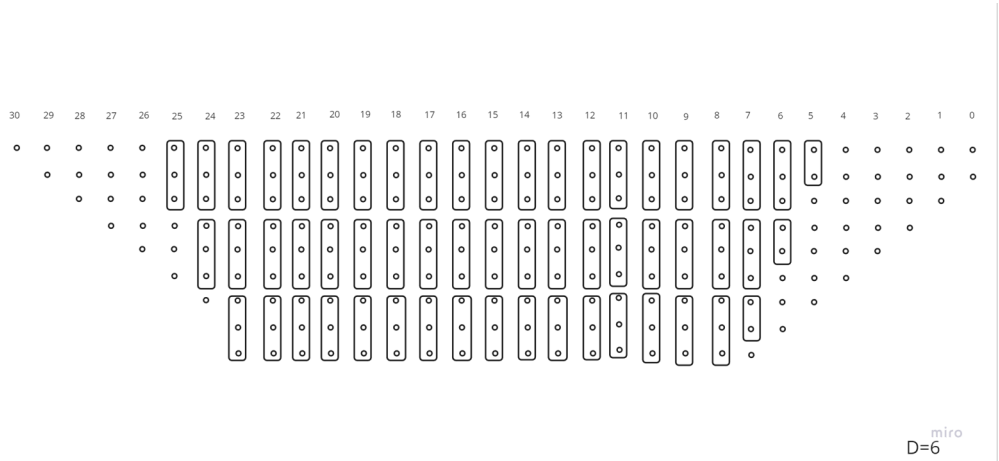
13 REDUCTIONS: -



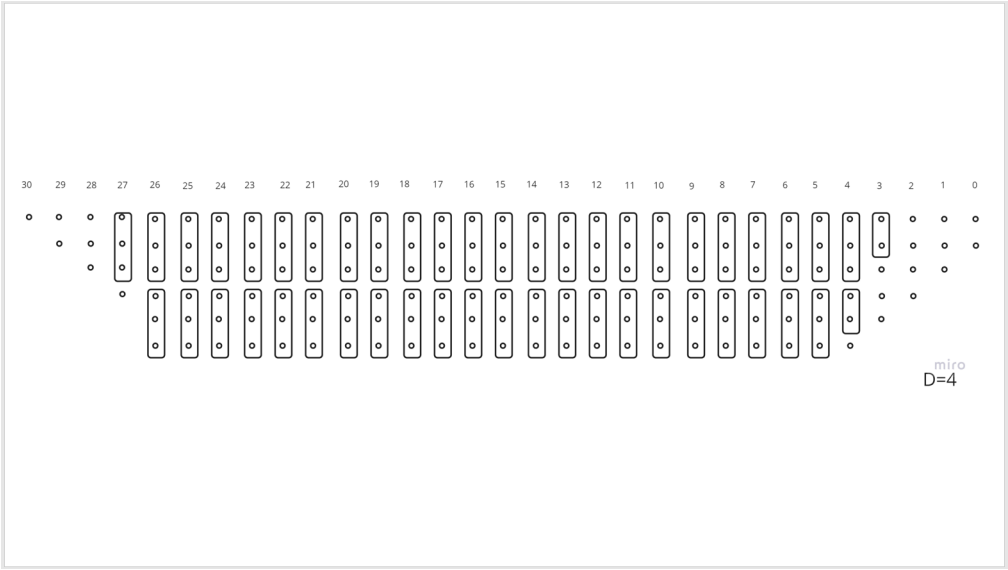
9 REDUCTIONS: -

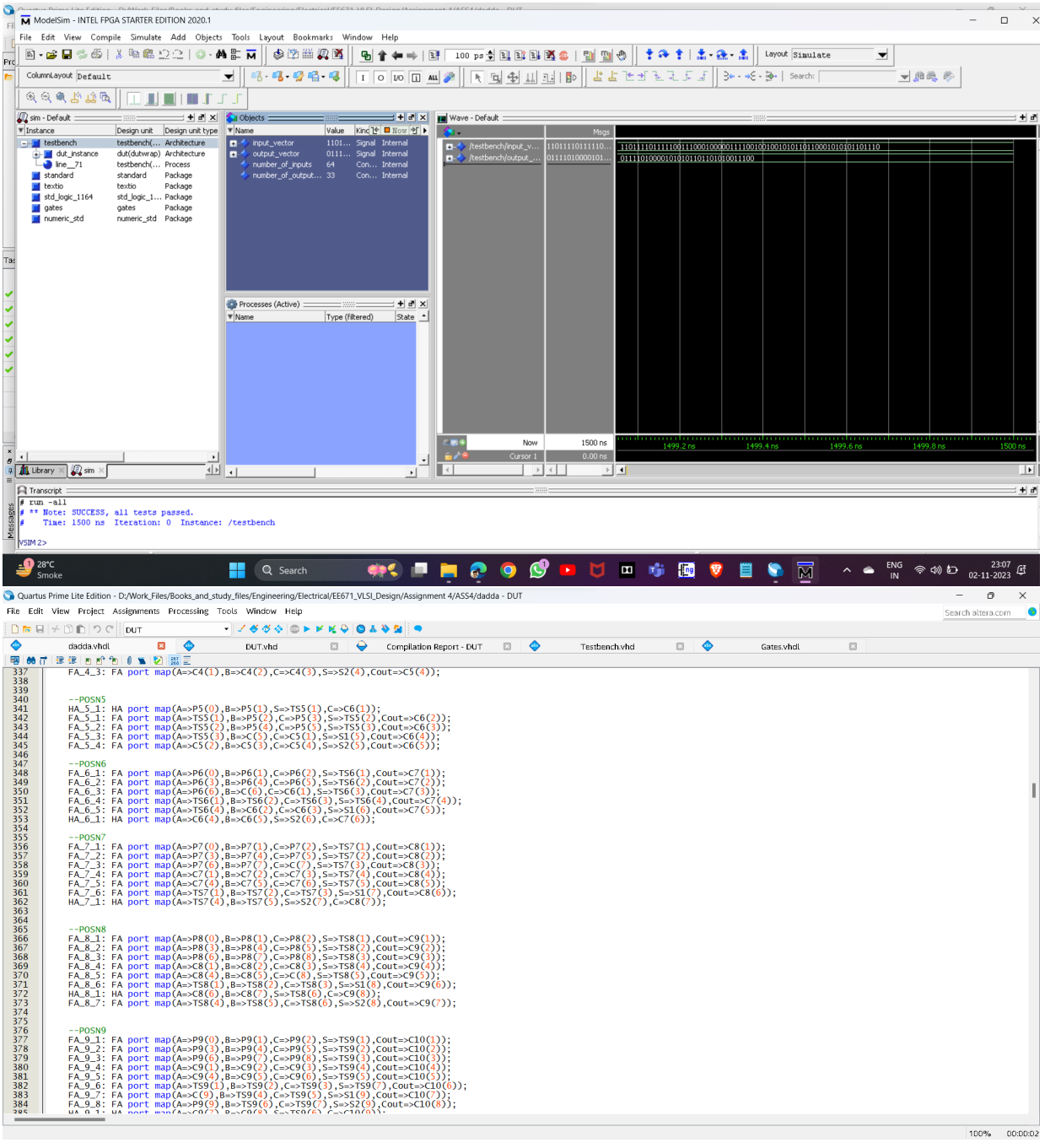


6 REDUCTIONS: -



4 REDUCTIONS: -



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    FA_4_3: FA port map(A=>C4(1),B=>C4(2),C=>C4(3),S=>S2(4),Cout=>C5(4));

    --POSN5
    HA_5_1: HA port map(A=>P5(0),B=>P5(1),S=>TS5(1),C=>C6(1));
    FA_5_1: FA port map(A=>TS5(1),B=>P5(2),C=>P5(3),S=>TS5(2),Cout=>C6(2));
    FA_5_2: FA port map(A=>TS5(2),B=>P5(4),C=>P5(5),S=>TS5(3),Cout=>C6(3));
    FA_5_3: FA port map(A=>TS5(3),B=>C(5),C=>C5(1),S=>S1(5),Cout=>C6(4));
    FA_5_4: FA port map(A=>C5(2),B=>C5(3),C=>C5(4),S=>S2(5),Cout=>C6(5));

    --POSN6
    FA_6_1: FA port map(A=>P6(0),B=>P6(1),C=>P6(2),S=>TS6(1),Cout=>C7(1));
    FA_6_2: FA port map(A=>P6(3),B=>P6(4),C=>P6(5),S=>TS6(2),Cout=>C7(2));
    FA_6_3: FA port map(A=>P6(6),B=>C(6),C=>C6(1),S=>TS6(3),Cout=>C7(3));
    FA_6_4: FA port map(A=>TS6(1),B=>TS6(2),C=>TS6(3),S=>TS6(4),Cout=>C7(4));
    FA_6_5: FA port map(A=>TS6(4),B=>C6(2),C=>C6(3),S=>S1(6),Cout=>C7(5));
    HA_6_1: HA port map(A=>C6(4),B=>C6(5),S=>S2(6),C=>C7(6));

    --POSN7
    FA_7_1: FA port map(A=>P7(0),B=>P7(1),C=>P7(2),S=>TS7(1),Cout=>C8(1));
    FA_7_2: FA port map(A=>P7(3),B=>P7(4),C=>P7(5),S=>TS7(2),Cout=>C8(2));
    FA_7_3: FA port map(A=>P7(6),B=>P7(7),C=>C(7),S=>TS7(3),Cout=>C8(3));
    FA_7_4: FA port map(A=>C7(1),B=>C7(2),C=>C7(3),S=>TS7(4),Cout=>C8(4));
    FA_7_5: FA port map(A=>C7(4),B=>C7(5),C=>C7(6),S=>TS7(5),Cout=>C8(5));
    FA_7_6: FA port map(A=>TS7(1),B=>TS7(2),C=>TS7(3),S=>S1(7),Cout=>C8(6));
    HA_7_1: HA port map(A=>TS7(4),B=>TS7(5),S=>S2(7),C=>C8(7));


    --POSN8
    FA_8_1: FA port map(A=>P8(0),B=>P8(1),C=>P8(2),S=>TS8(1),Cout=>C9(1));
    FA_8_2: FA port map(A=>P8(3),B=>P8(4),C=>P8(5),S=>TS8(2),Cout=>C9(2));
    FA_8_3: FA port map(A=>P8(6),B=>P8(7),C=>P8(8),S=>TS8(3),Cout=>C9(3));
    FA_8_4: FA port map(A=>C8(1),B=>C8(2),C=>C8(3),S=>TS8(4),Cout=>C9(4));
    FA_8_5: FA port map(A=>C8(4),B=>C8(5),C=>C(8),S=>TS8(5),Cout=>C9(5));
    FA_8_6: FA port map(A=>TS8(1),B=>TS8(2),C=>TS8(3),S=>S1(8),Cout=>C9(6));
    HA_8_1: HA port map(A=>C8(6),B=>C8(7),S=>TS8(6),C=>C9(8));
    FA_8_7: FA port map(A=>TS8(4),B=>TS8(5),C=>TS8(6),S=>S2(8),Cout=>C9(7));


    --POSN9
    FA_9_1: FA port map(A=>P9(0),B=>P9(1),C=>P9(2),S=>TS9(1),Cout=>C10(1));
    FA_9_2: FA port map(A=>P9(3),B=>P9(4),C=>P9(5),S=>TS9(2),Cout=>C10(2));
    FA_9_3: FA port map(A=>P9(6),B=>P9(7),C=>P9(8),S=>TS9(3),Cout=>C10(3));
    FA_9_4: FA port map(A=>C9(1),B=>C9(2),C=>C9(3),S=>TS9(4),Cout=>C10(4));
    FA_9_5: FA port map(A=>C9(4),B=>C9(5),C=>C9(6),S=>TS9(5),Cout=>C10(5));
    FA_9_6: FA port map(A=>TS9(1),B=>TS9(2),C=>TS9(3),S=>TS9(7),Cout=>C10(6));
    FA_9_7: FA port map(A=>C(9),B=>TS9(4),C=>TS9(5),S=>S1(9),Cout=>C10(7));
    FA_9_8: FA port map(A=>P9(9),B=>TS9(6),C=>TS9(7),S=>S2(9),Cout=>C10(8));
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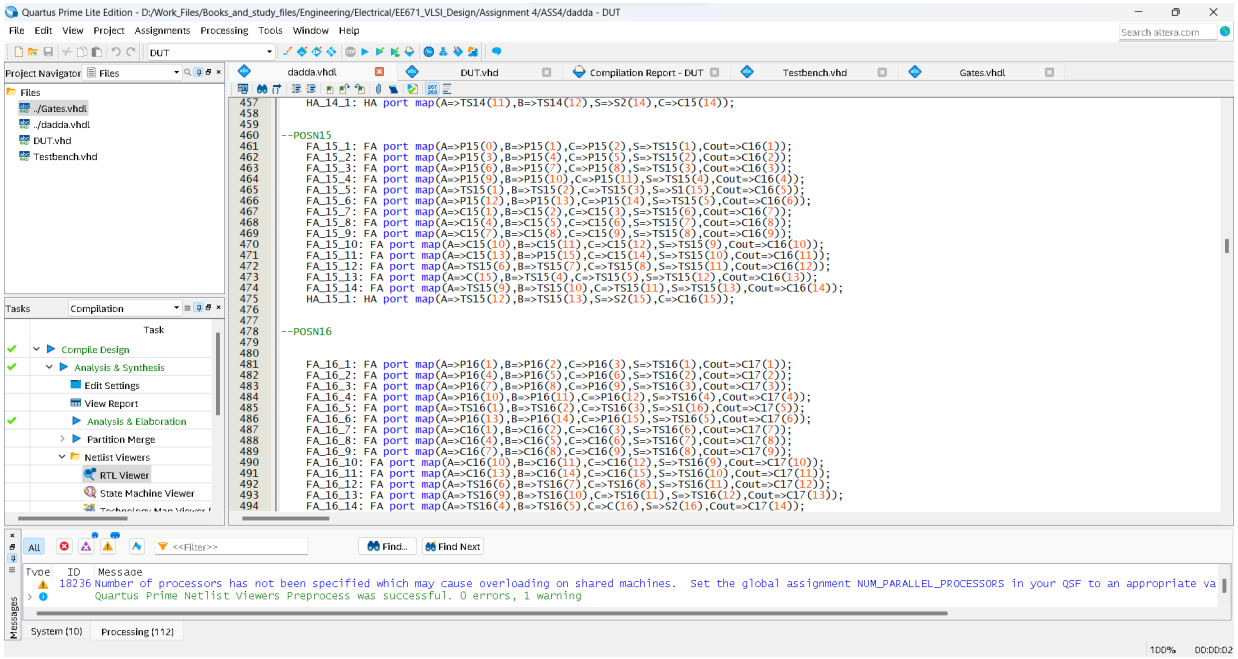
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Testbench.vhd
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Compilation Report - DUT
Testbench.vhd
Gates.vhdl
457 HA_14_1: HA port map(A=>TS14(11),B=>TS14(12),S=>S2(14),C=>C15(14));
459
460 --POSN15
461 FA_15_1: FA port map(A=>P15(0),B=>P15(1),C=>P15(2),S=>TS15(1),Cout=>C16(1));
462 FA_15_2: FA port map(A=>P15(3),B=>P15(4),C=>P15(5),S=>TS15(2),Cout=>C16(2));
463 FA_15_3: FA port map(A=>P15(6),B=>P15(7),C=>P15(8),S=>TS15(3),Cout=>C16(3));
464 FA_15_4: FA port map(A=>P15(9),B=>P15(10),C=>P15(11),S=>TS15(4),Cout=>C16(4));
465 FA_15_5: FA port map(A=>TS15(1),B=>TS15(2),C=>TS15(3),S=>S1(15),Cout=>C16(5));
466 FA_15_6: FA port map(A=>P15(12),B=>P15(13),C=>P15(14),S=>TS15(5),Cout=>C16(6));
467 FA_15_7: FA port map(A=>C15(1),B=>C15(2),C=>C15(3),S=>TS15(6),Cout=>C16(7));
468 FA_15_8: FA port map(A=>C15(4),B=>C15(5),C=>C15(6),S=>TS15(7),Cout=>C16(8));
469 FA_15_9: FA port map(A=>C15(7),B=>C15(8),C=>C15(9),S=>TS15(8),Cout=>C16(9));
470 FA_15_10: FA port map(A=>C15(10),B=>C15(11),C=>C15(12),S=>TS15(9),Cout=>C16(10));
471 FA_15_11: FA port map(A=>C15(13),B=>P15(15),C=>C15(14),S=>TS15(10),Cout=>C16(11));
472 FA_15_12: FA port map(A=>TS15(6),B=>TS15(7),C=>TS15(8),S=>TS15(11),Cout=>C16(12));
473 FA_15_13: FA port map(A=>C(15),B=>TS15(4),C=>TS15(5),S=>TS15(12),Cout=>C16(13));
474 FA_15_14: FA port map(A=>TS15(9),B=>TS15(10),C=>TS15(11),S=>TS15(13),Cout=>C16(14));
475 HA_15_1: HA port map(A=>TS15(12),B=>TS15(13),S=>S2(15),C=>C16(15));
476
477
478 --POSN16
479
480
481 FA_16_1: FA port map(A=>P16(1),B=>P16(2),C=>P16(3),S=>TS16(1),Cout=>C17(1));
482 FA_16_2: FA port map(A=>P16(4),B=>P16(5),C=>P16(6),S=>TS16(2),Cout=>C17(2));
483 FA_16_3: FA port map(A=>P16(7),B=>P16(8),C=>P16(9),S=>TS16(3),Cout=>C17(3));
484 FA_16_4: FA port map(A=>P16(10),B=>P16(11),C=>P16(12),S=>TS16(4),Cout=>C17(4));
485 FA_16_5: FA port map(A=>TS16(1),B=>TS16(2),C=>TS16(3),S=>S1(16),Cout=>C17(5));
486 FA_16_6: FA port map(A=>P16(13),B=>P16(14),C=>P16(15),S=>TS16(5),Cout=>C17(6));
487 FA_16_7: FA port map(A=>C16(1),B=>C16(2),C=>C16(3),S=>TS16(6),Cout=>C17(7));
488 FA_16_8: FA port map(A=>C16(4),B=>C16(5),C=>C16(6),S=>TS16(7),Cout=>C17(8));
489 FA_16_9: FA port map(A=>C16(7),B=>C16(8),C=>C16(9),S=>TS16(8),Cout=>C17(9));
490 FA_16_10: FA port map(A=>C16(10),B=>C16(11),C=>C16(12),S=>TS16(9),Cout=>C17(10));
491 FA_16_11: FA port map(A=>C16(13),B=>C16(14),C=>C16(15),S=>TS16(10),Cout=>C17(11));
492 FA_16_12: FA port map(A=>TS16(6),B=>TS16(7),C=>TS16(8),S=>TS16(11),Cout=>C17(12));
493 FA_16_13: FA port map(A=>TS16(9),B=>TS16(10),C=>TS16(11),S=>TS16(12),Cout=>C17(13));
494 FA_16_14: FA port map(A=>TS16(4),B=>TS16(5),C=>C(16),S=>S2(16),Cout=>C17(14));
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