VLSI Design

Final Project Report

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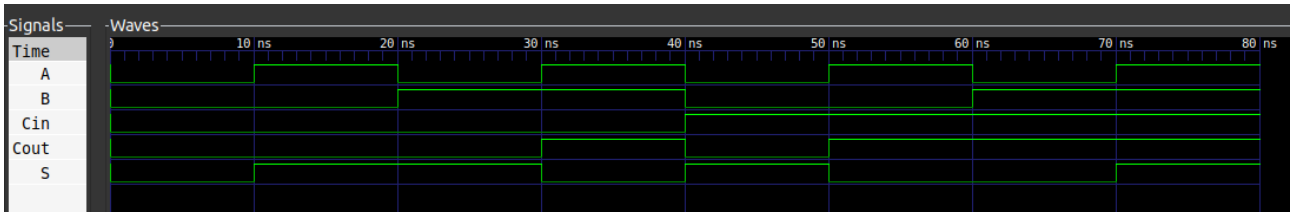
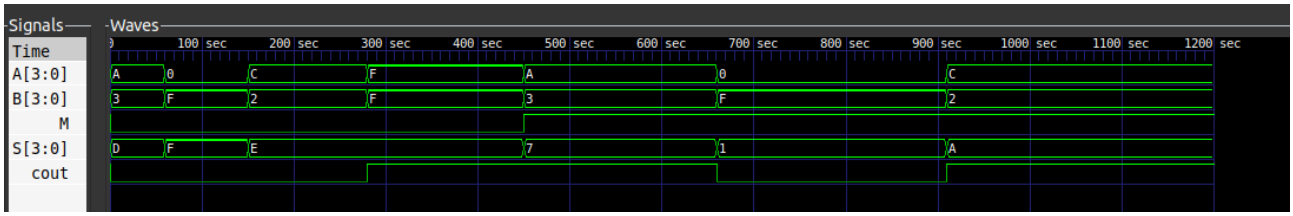
1)Verilog

Results from Verilog codes are shown below:

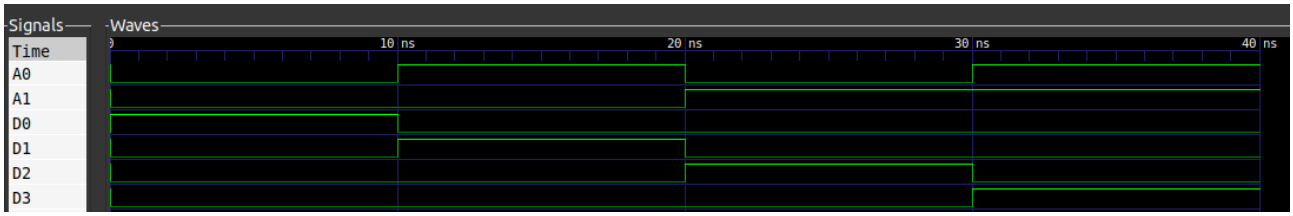
i)Full Adder:



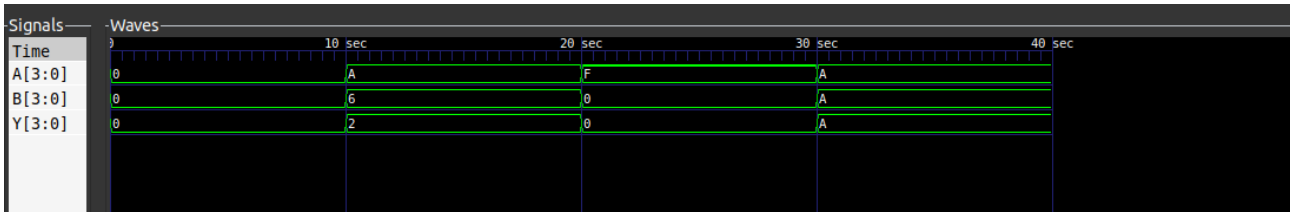
ii) Four Bit Adder/Subtractor:



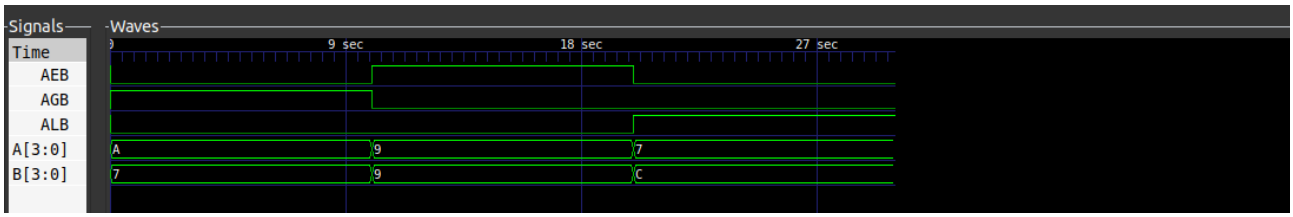
iii) Twotofour Decoder:



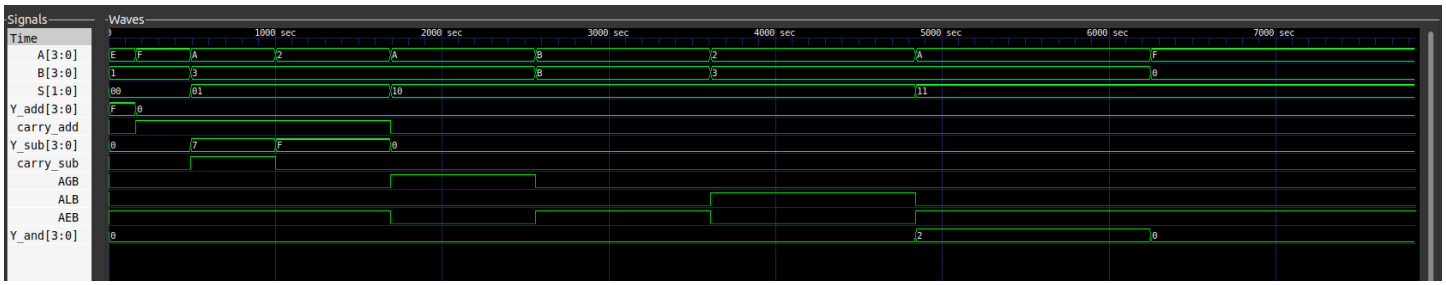
iv) AndBlock:



v) Comparator:



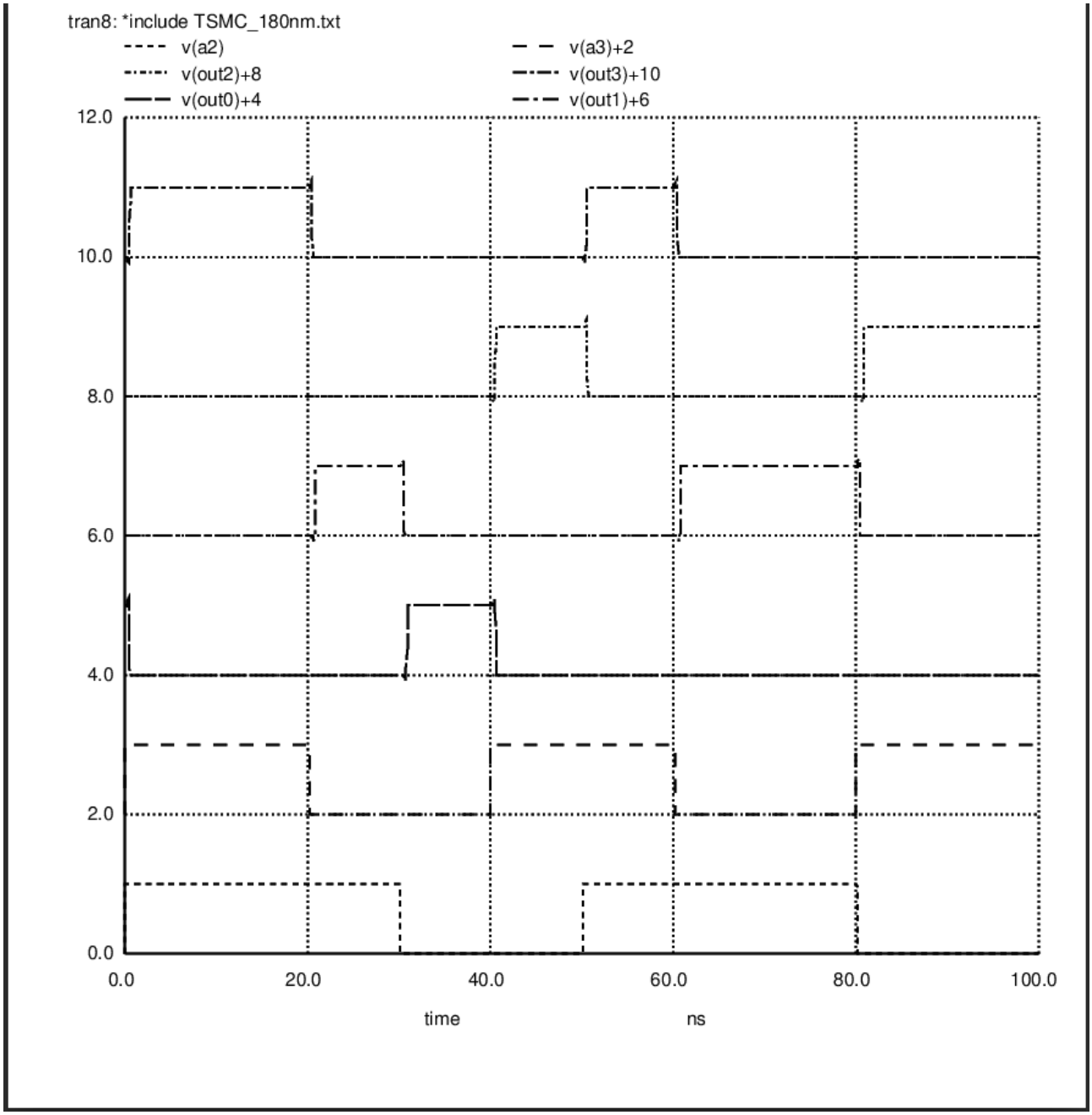
vi) Alu :



2)NG SPICE

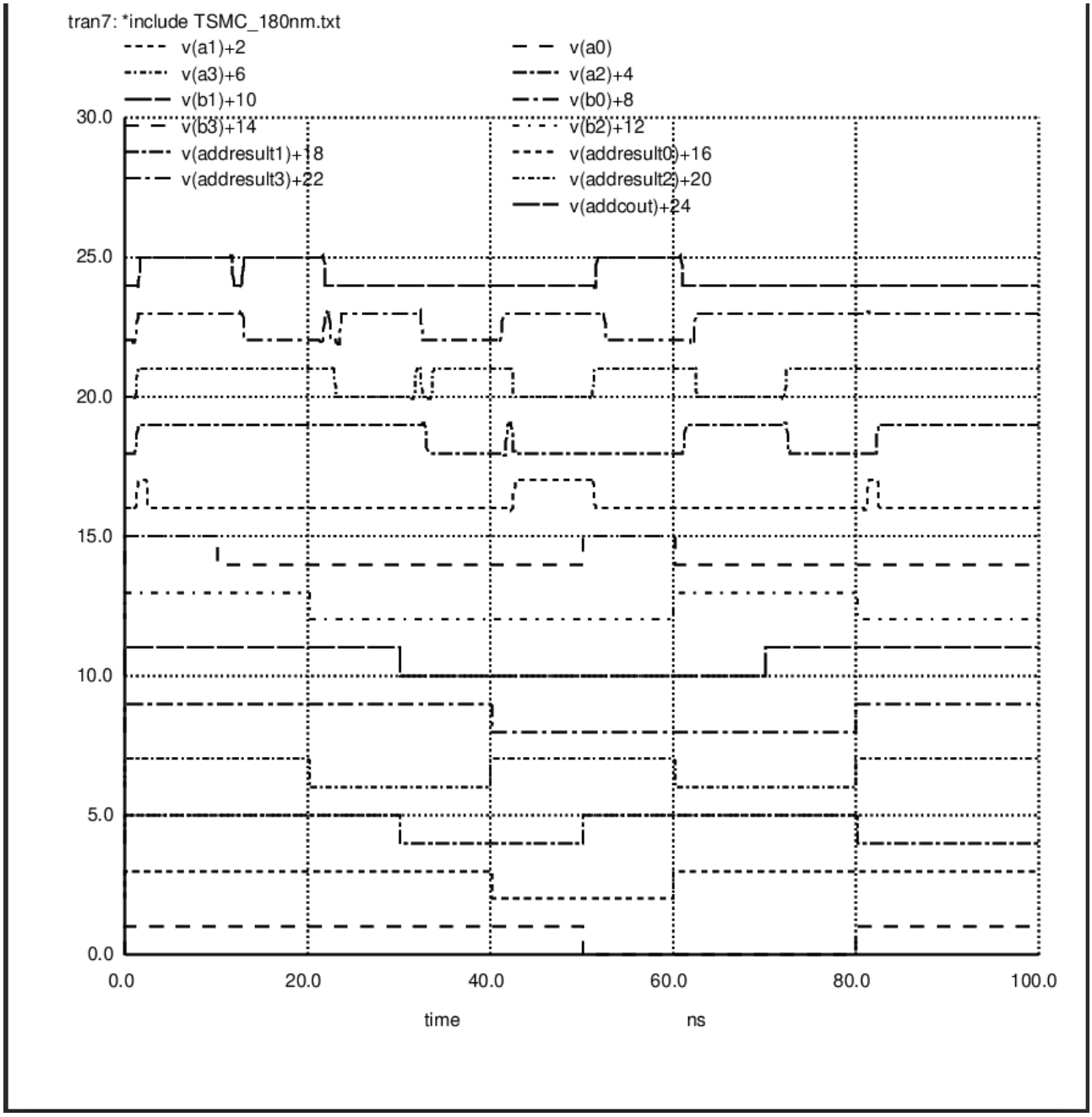
The results from Ng spice simulations are shown below

i) Two to fourdecoder:

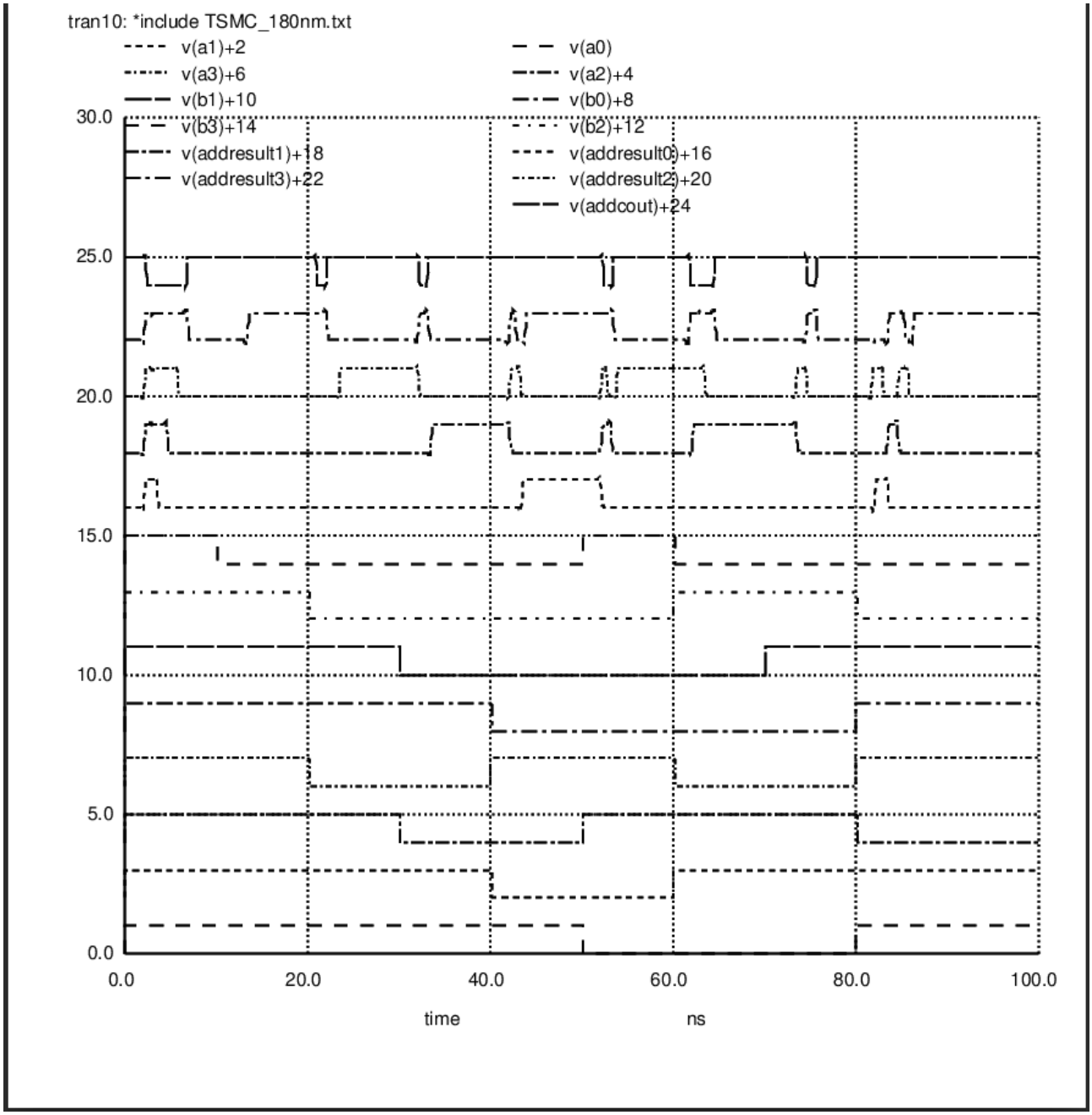


The below are the results from main Alucircuit when each operation is done seperately

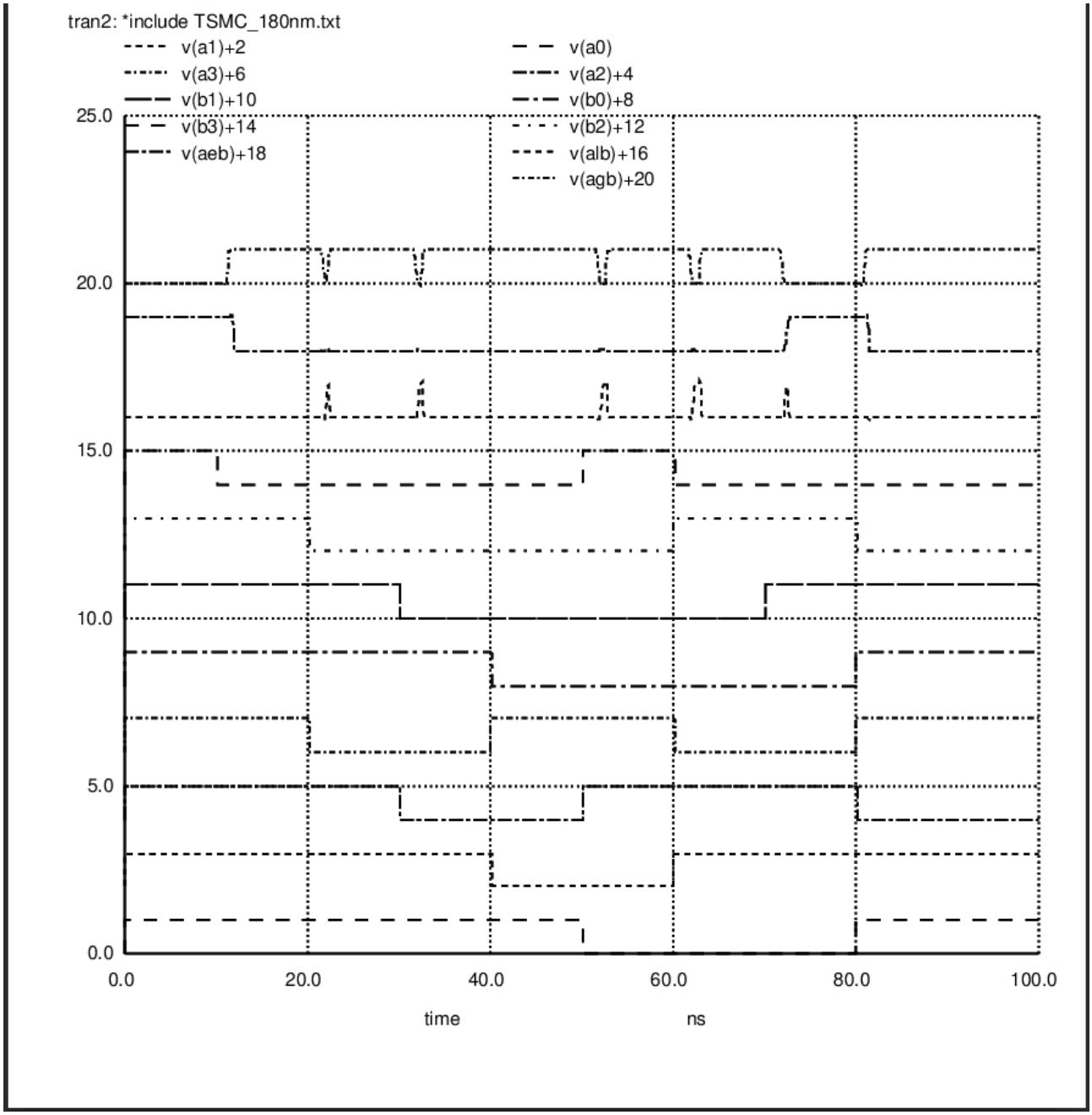
ii) Adder Block:



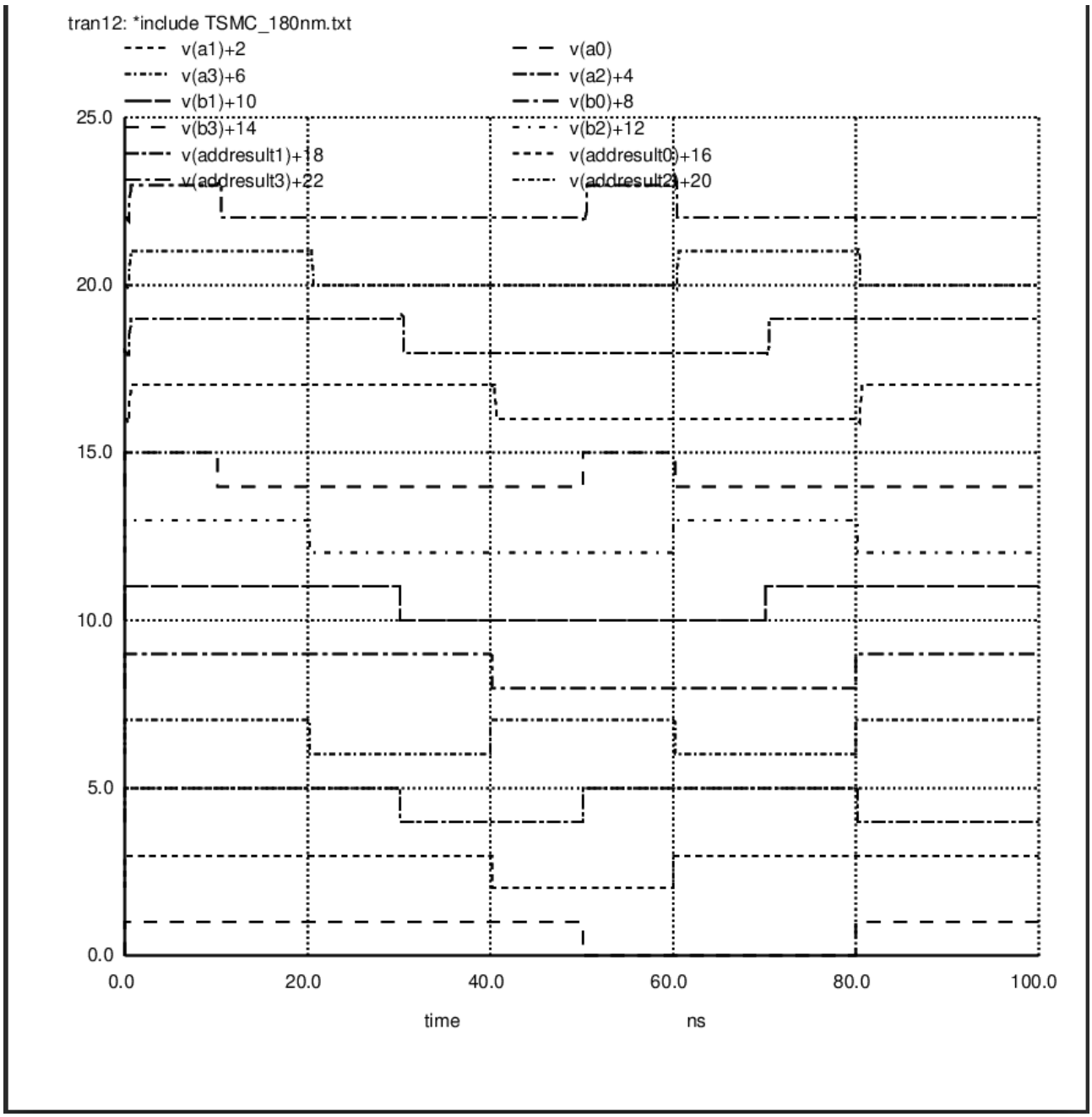
iii)Subtractor



iii)Comparator:



iv)Andblock:


tran12: *include TSMC_180nm.txt
v(a1)+2
v(a0)
v(a3)+6
v(a2)+4
v(b1)+10
v(b0)+8
v(b3)+14
v(b2)+12
v(addresult1)+18
v(addresult0)+16
v(addresult3)+22
v(addresult2)+20
25.0
20.0
15.0
10.0
5.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ns

3) MAGIC