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DOCUMENTATIONCACHE PROJECT LEVEL-2

In this I have taken a 2-Level cache: L1 and L2.

Mapping for both the caches is taken as input. While block size for both caches remain the same, the no. Of cache lines in L1 is half that of L2 as required. Writing is done in both caches simultaneously. Replacement strategy remains the same as in case of the Single level cache. While reading opertaion is done on L1 first. In case there is a miss, we move to L2-cache. If there is a miss in L1 and hit in L2 then we also need to write the address to L1 from L2. If there is a hit in L1 we will not search in L2. Some important variables defined:

current_data= Initiallized to "-1". Keeps track of data in L2 when there is miss in L1. **check_level=**checks the current Level of cache being worked upon.

c_rows=no. Of rows in the cache(cache lines)

c_cols=no. Of columns in the cache(block size)

cache_array[][]=contents of cache memory

tag_set[],tag_bits[],tag_array[]=keeps track of the tags for different mappings
associate_counter=keeps track of the cache filled in associate mapping
set_counter[]=keeps track of cache lines filled in each set

num set=number of sets

lines_in_each_set=Value of n (in case of n-way set or set size)

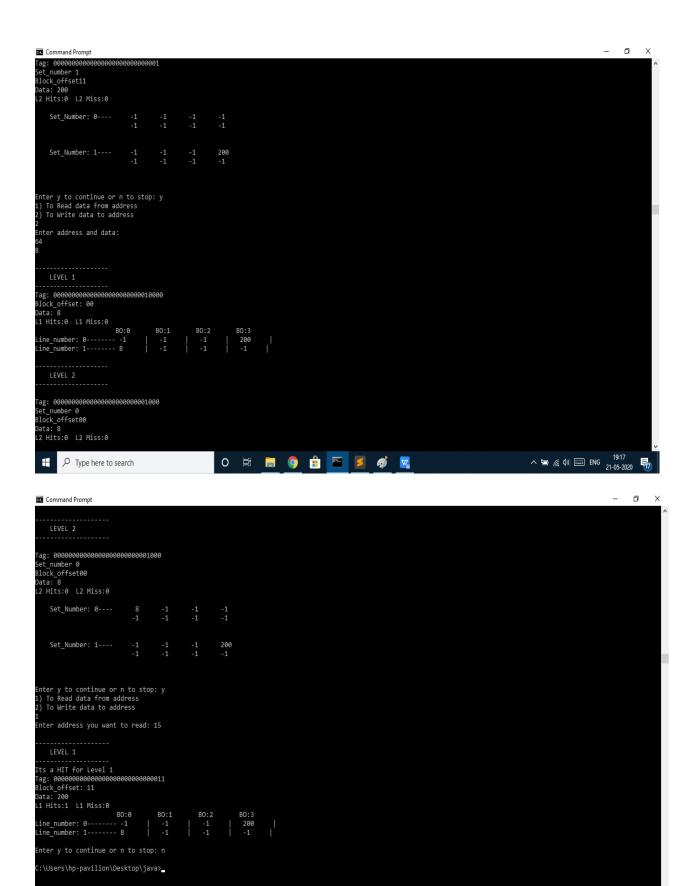
num_hits=number of hits;

num_miss=number of misses;

This is a screenshot of my cache project."-1" represents no data in the cell of the block. BO is Block_offset. There is Associative mapping in L1 and n-way-set-Associative in L2(with n=2).

The machine word length is 32 bits. The No. Of cache lines is 4 and Block Size is 4.

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