Assignment - 1

Statement: Given that the sequence of instructions to be executed processor, Design a 5 – stage (Instruction Fetch; Decode; Execute; Memory Access; Write Back) multi-cycle RISC processor that can execute following instructions.

Step 1: Draw the detailed architecture-level diagram of the processor, depicting all the blocks (e.g. register file, instruction memory, ALU, PC, and combinational functional blocks, etc.).

Step 2: Create Verilog behavioral models for each architectural block separately.

Step 3: Build the top-level structural model of the processor by instantiating and interconnecting the individual architectural blocks.

Step 4: Initialize the instruction memory with the following instructions:

0000 BEQ reg1, reg2, 7
0004 ORI reg5, reg4, 10

Initialize the register file with the following data
reg1 = 26677D reg2 = 2667DA
reg4 = 55F3

Initialize PC with 0000 address. All the registers are 32 bits wide. Each element in memory is 8-bit wide and memory has 50 locations.