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LAB 02 : BEHAVIORAL SIMULATION

LAB REPORT

TASK ASSIGNED:

1. Read the scenario given and draw a truth table to identify the resultant output state (3 LED's state whether it is Red or Amber or Green) depending on the each possible input combination (3 generator's state whether it is ON or OFF).
2. Using a Karnaugh map, get the simplified Boolean expression for the logic in the given scenario.
3. Code the circuit in VHDL and design it in Xilinx Vivado software.
4. Obtain the schematic diagram for the circuit.
5. Construct a test bench code to simulate the coded circuit.
6. Using the simulation timeline, verify the circuit comparing to real scenario's functionality.

TRUTH TABLE FOR THE GIVEN SCENARIO:

m	A	B	C	Y_1 (Green)	Y_2 (Amber)	Y_3 (Red)
0	0	0	0	0	0	1
1	0	0	1	0	0	1
2	0	1	0	0	0	1
3	0	1	1	0	1	0
4	1	0	0	0	0	1
5	1	0	1	0	1	0
6	1	1	0	0	1	0
7	1	1	1	1	0	0

MIN-TERM CANONICAL SUM OF PRODUCTS WITH SHORTHAND NOTATION:

1. $Y_1 = \sum_{(A,B,C)}(7)$
2. $Y_2 = \sum_{(A,B,C)}(3, 5, 6)$
3. $Y_3 = \sum_{(A,B,C)}(0, 1, 2, 4)$

SIMPLIFIED EXPRESSIONS FOR Green, Amber & Red:

1. Y_1 = ABC
2. Y_2 = (ABC') + (A'BC) + (AB'C)
3. Y_3 = (A'B') + (AB'C') + (A'BC')

AB / C	00	01	11	10
0	0	0	0	0
1	0	0	1	0

K-MAP FOR Y_1 (Green)

$$Y_1 = ABC$$

AB / C	00	01	11	10
0	0	0	1	0
1	0	1	0	1

K-MAP FOR Y_2 (Amber)

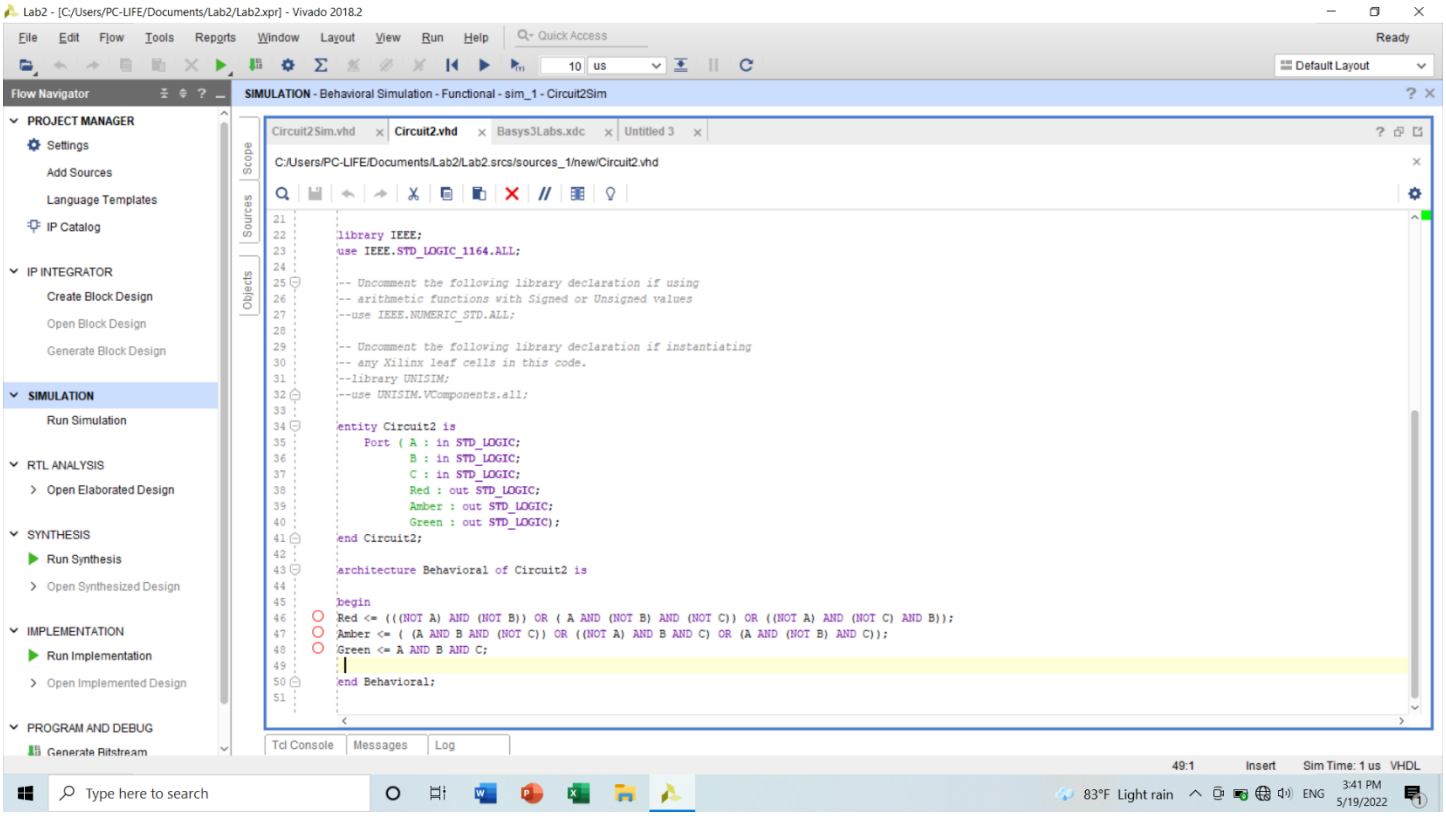
$$Y_2 = (ABC') + (A'BC) + (AB'C)$$

AB / C	00	01	11	10
0	1	1	0	1
1	1	0	0	0

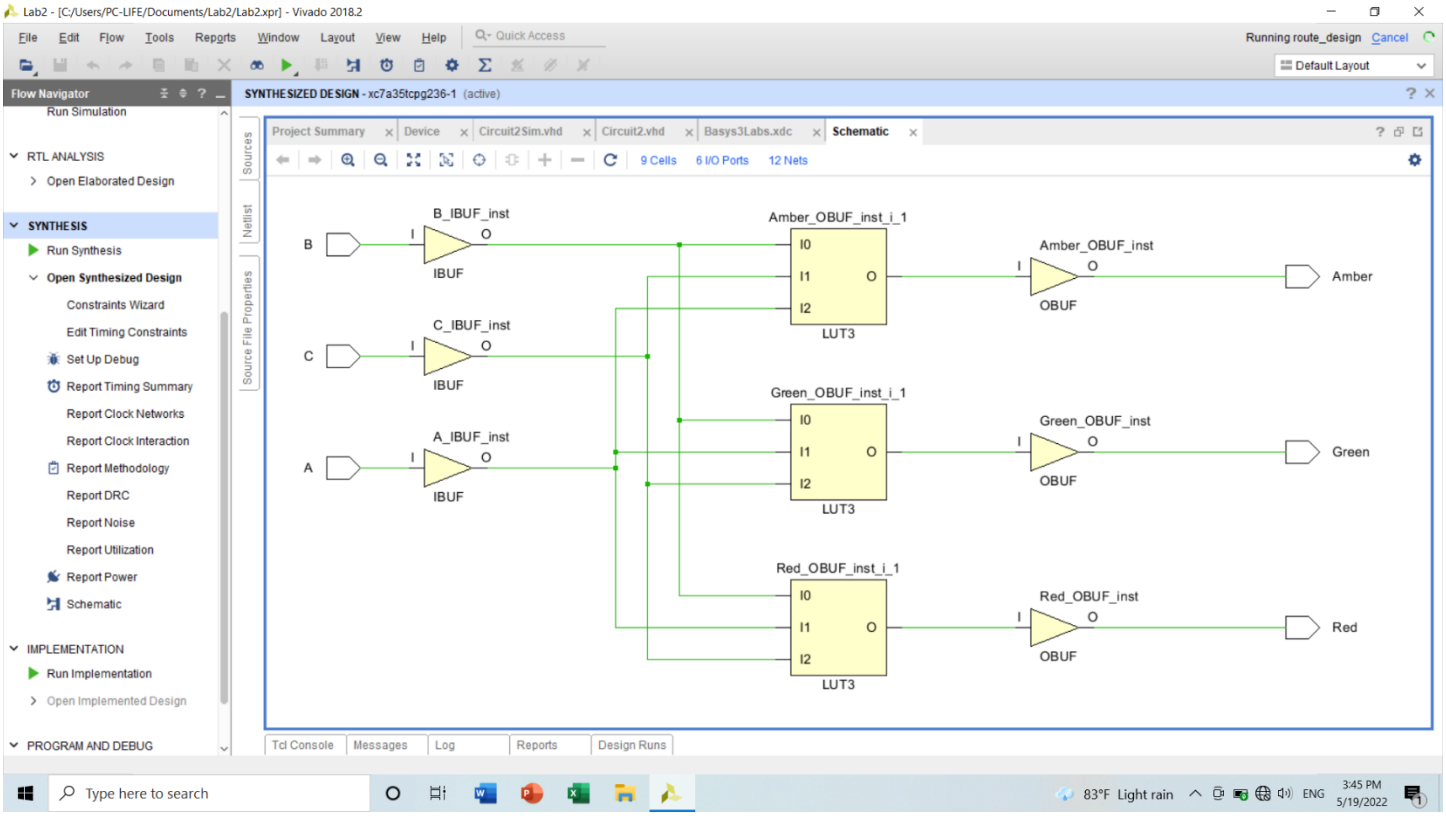
K-MAP FOR Y_3 (Red)

$$Y_3 = (A'B') + (AB'C') + (A'BC')$$

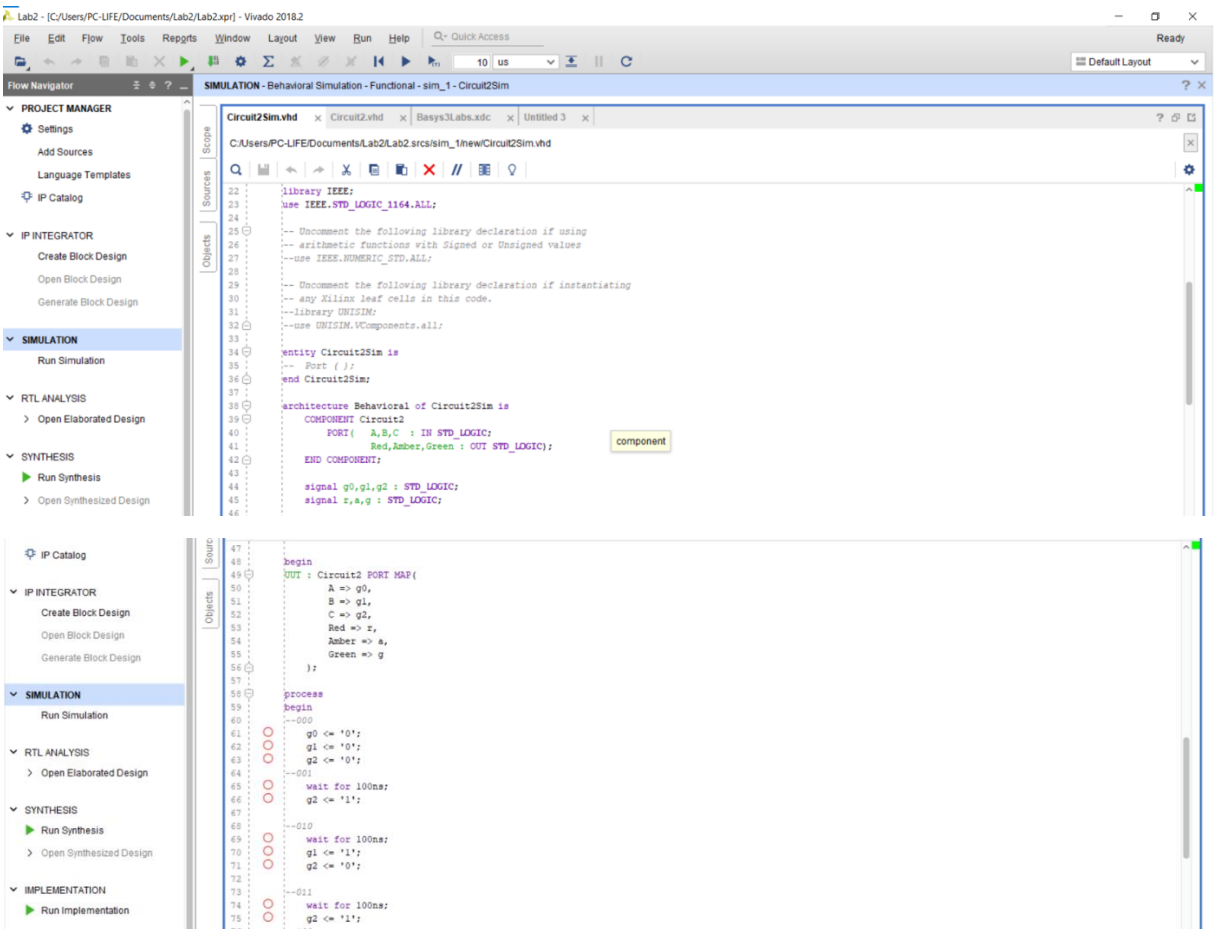
FULL VHDL DESIGN SOURCE CODE:

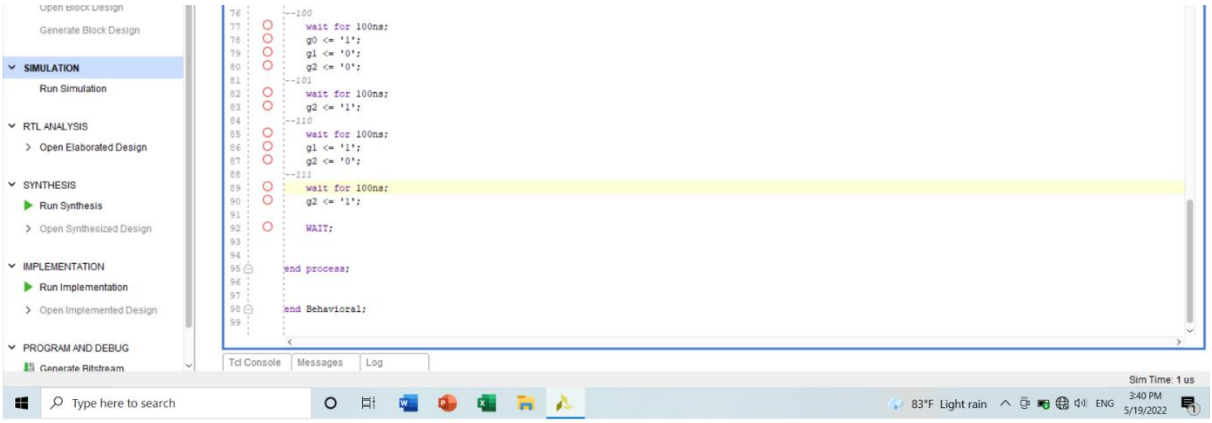


SCHEMATIC CIRCUIT FROM VIVADO:

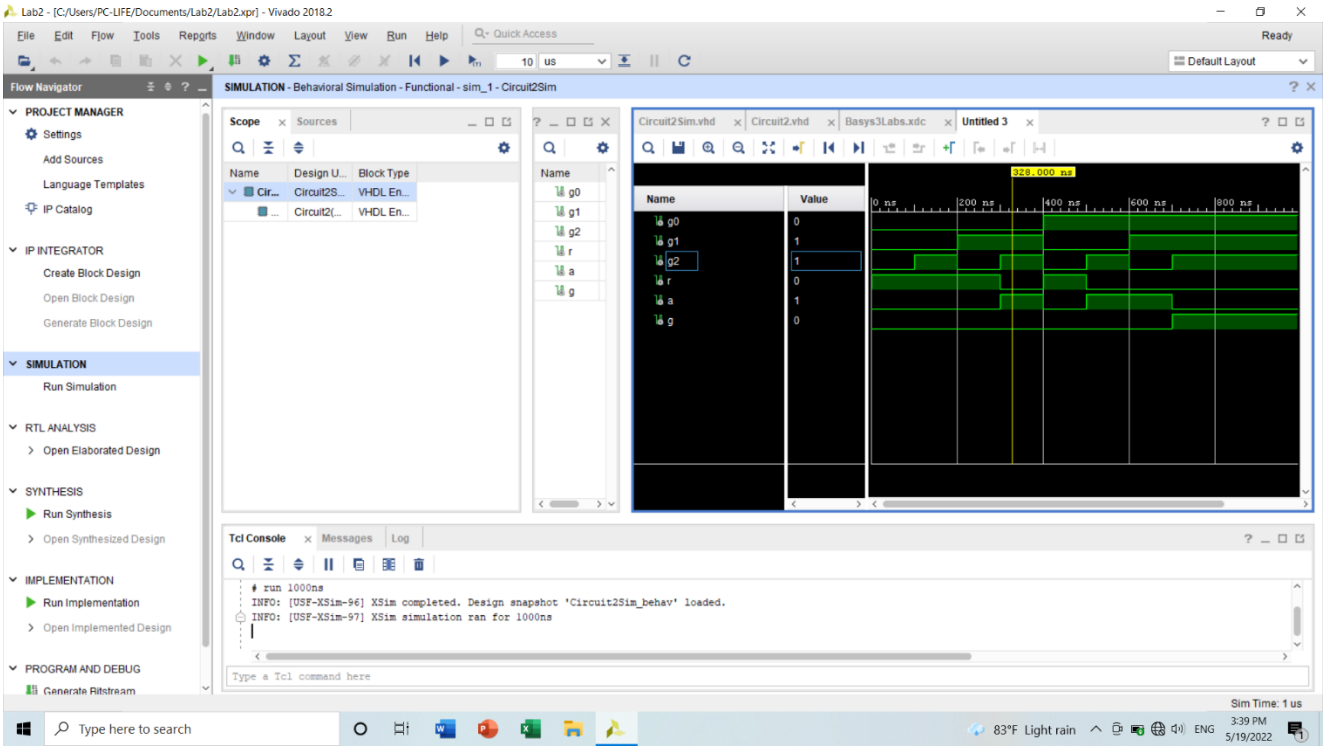


TEST BENCH CODE:





TIMING DIAGRAM FROM XSIM SHOWING ALL POSSIBLE INPUTS AND OUTPUTS:



CONCLUSIONS:

- **The output of a logic can be identified using a truth table considering all possible scenarios of inputs.**
- **The logic displayed in truth table can be converted into Boolean terms using the method of min-term canonical sum of products.**
- **Using a Karnaugh map, a Boolean expression can be further simplified for the ease of use.**
- **Schematic diagram can be obtained using Vivado software as per the design source. (Here it was coded in VHDL.)**
- **Vivado's behavioral simulation allows to verify the proper functionality of every RTL module in a design at anytime. (without needing to run synthesis or implementation)**
- **It runs a specified testbench module (where the logic inputs are mapped to simulation's variables and the simulation procedure is structured in a timely manner) and then displays the logic of the testbench's results in a waveform window.**