LAB 06: ARITHMETIC UNIT

TIMING DIAGRAM OF ARITHMETIC UNIT Lab6 - [C:/Users/PC-LIFE/Documents/Lab6/Lab6.xpr] - Vivado 2018.2 <u>File Edit Flow Tools Reports Window Layout View Run Help Q- Quick Access</u> Synthesis Complete □ ← → □ □ × ▶ ♯ ❖ Σ ½ ∅ ⅙ ▶ ㎞ 10 us v <u>∓</u> ∥ C E Default Layout SIMULATION - Behavioral Simulation - Functional - sim_1 - TB_AU AU.vhd x RCA_4.vhd x TB_AU.vhd x Untitled 14 x ? 🗆 🖸 Q H Q Q X + K N ± ± + F F F H √ M A[3:0] **1** [3] **1** [2] 0 la [1] **[0]** 0 **⊌** S[3:0] 7 / 8 / 9 / a / b / d / e / f 0 **1** [3] **l** [2] 0 16 [1] **[0]** RegSel Clk **⊿** Zero Carry Tcl Console Messages Log

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TEST BENCH OF ARITHMETIC UNIT

```
RegSel <= '1';
library IEEE;
                                                                                                                 wait for 20ns;
                                                       SIGNAL A ,S : STD LOGIC VECTOR(3 downto 0)
use IEEE.STD LOGIC 1164.ALL;
                                                        := "0000";
                                                                                                                 RegSel <= '0';
-- Uncomment the following library declaration
                                                                                                                 wait for 20ns;
                                                        SIGNAL RegSel, Clk, Zero, Carry:
if using
                                                        STD LOGIC:='0';
                                                                                                                 A <= "0010"; --200'3'32X
-- arithmetic functions with Signed or Unsigned
                                                                                                                 RegSel <= '1';
values
                                                        begin
                                                                                                                 wait for 20ns;
                                                       UUT: AU PORT MAP(
                                                                                                                 RegSel <= '0';
--use IEEE.NUMERIC_STD.ALL;
                                                                                                                 wait for 20ns;
                                                          A => A
-- Uncomment the following library declaration
                                                          S => S,
if instantiating
                                                                                                               --simulation for all other possible input combinations
                                                          RegSel => RegSel,
-- any Xilinx leaf cells in this code.
                                                          Clk => Clk,
                                                                                                                 A <= "0000":
--library UNISIM;
                                                          Zero => Zero,
                                                                                                                 wait for 20ns;
                                                          Carry => Carry);
--use UNISIM.VComponents.all;
                                                                                                                 RegSel <= '1';
                                                        process
                                                                                                                 wait for 20ns;
                                                        begin
                                                                                                                 RegSel <= '0';
entity TB AU is
                                                         Clk <= NOT(Clk);
                                                                                                                 wait for 20ns;
-- Port ();
                                                          wait for 2ns:
                                                                                                                 A <= "0001";
end TB AU;
                                                        end process;
                                                                                                                 wait for 20ns;
architecture Behavioral of TB AU is
                                                        process
                                                                                                                 RegSel <= '1';
component AU
                                                        begin
                                                                                                                 wait for 20ns;
Port (A: in STD LOGIC VECTOR (3 downto 0);
                                                          A <= "0010": --'2'00332X
                                                                                                                 RegSel <= '0';
      RegSel: in STD_LOGIC;
                                                          RegSel <= '1';
                                                                                                                 wait for 20ns;
      Clk: in STD_LOGIC;
                                                          wait for 20ns;
                                                                                                                 A <= "0010";
     S: out STD_LOGIC_VECTOR (3 downto 0);
                                                          RegSel <= '0';
                                                                                                                 wait for 20ns;
     Zero: out STD_LOGIC;
                                                          wait for 20ns;
                                                                                                                 RegSel <= '1';
      Carry: out STD LOGIC);
                                                          A <= "0000"; --2'0'0332X
                                                                                                                 wait for 20ns;
end component;
```

| RegSel <= '0'; | wait for 20ns; | RegSel <= '1'; |
|----------------|----------------|-----------------|
| wait for 20ns; | RegSel <= '0'; | wait for 20ns; |
| A <= "0011"; | wait for 20ns; | RegSel <= '0'; |
| wait for 20ns; | A <= "1000"; | wait for 20ns; |
| RegSel <= '1'; | wait for 20ns; | A <= "1101"; |
| wait for 20ns; | RegSel <= '1'; | wait for 20ns; |
| RegSel <= '0'; | wait for 20ns; | RegSel <= '1'; |
| wait for 20ns; | RegSel <= '0'; | wait for 20ns; |
| A <= "0100"; | wait for 20ns; | RegSel <= '0'; |
| wait for 20ns; | A <= "1001"; | wait for 20ns; |
| RegSel <= '1'; | wait for 20ns; | A <= "1110"; |
| wait for 20ns; | RegSel <= '1'; | wait for 20ns; |
| RegSel <= '0'; | wait for 20ns; | RegSel <= '1'; |
| wait for 20ns; | RegSel <= '0'; | wait for 20ns; |
| A <= "0101"; | wait for 20ns; | RegSel <= '0'; |
| wait for 20ns; | A <= "1010"; | wait for 20ns; |
| RegSel <= '1'; | wait for 20ns; | A <= "1111"; |
| wait for 20ns; | RegSel <= '1'; | RegSel <= '1'; |
| RegSel <= '0'; | wait for 20ns; | wait for 20ns; |
| wait for 20ns; | RegSel <= '0'; | RegSel <= '0'; |
| A <= "0110"; | wait for 20ns; | wait for 20ns; |
| wait for 20ns; | A <= "1011"; | wait; |
| RegSel <= '1'; | wait for 20ns; | end process; |
| wait for 20ns; | RegSel <= '1'; | end Behavioral; |
| RegSel <= '0'; | wait for 20ns; | |
| wait for 20ns; | RegSel <= '0'; | |
| A <= "0111"; | wait for 20ns; | |
| wait for 20ns; | A <= "1100"; | |
| RegSel <= '1'; | wait for 20ns; | |
| | | |