

LAB 02 : BEHAVIORAL SIMULATION

LAB REPORT

TASK ASSIGNED:

1. Read the scenario given and draw a truth table to identify the resultant output state (3 LED's state whether it is Red or Amber or Green) depending on the each possible input combination (3 generator's state whether it is ON or OFF).
2. Using a Karnaugh map, get the simplified Boolean expression for the logic in the given scenario.
3. Code the circuit in VHDL and design it in Xilinx Vivado software.
4. Obtain the schematic diagram for the circuit.
5. Construct a test bench code to simulate the coded circuit.
6. Using the simulation timeline, verify the circuit comparing to real scenario's functionality.

TRUTH TABLE FOR THE GIVEN SCENARIO:

m	A	B	C	Y ₁ (Green)	Y ₂ (Amber)	Y ₃ (Red)
0	0	0	0	0	0	1
1	0	0	1	0	0	1
2	0	1	0	0	0	1
3	0	1	1	0	1	0
4	1	0	0	0	0	1
5	1	0	1	0	1	0
6	1	1	0	0	1	0
7	1	1	1	1	0	0

MIN-TERM CANONICAL SUM OF PRODUCTS WITH SHORTHAND NOTATION:

1. $Y_1 = \sum_{(A,B,C)}(7)$
2. $Y_2 = \sum_{(A,B,C)}(3, 5, 6)$
3. $Y_3 = \sum_{(A,B,C)}(0, 1, 2, 4)$

SIMPLIFIED EXPRESSIONS FOR Green, Amber & Red:

1. $Y_1 = ABC$
2. $Y_2 = (ABC') + (A'BC) + (AB'C)$
3. $Y_3 = (A'B') + (AB'C') + (A'BC')$

AB \ C	00	01	11	10
0	0	0	0	0
1	0	0	1	0

K-MAP FOR Y_1 (Green)

$$Y_1 = ABC$$

AB \ C	00	01	11	10
0	0	0	1	0
1	0	1	0	1

K-MAP FOR Y_2 (Amber)

$$Y_2 = (ABC') + (A'BC) + (AB'C)$$

AB \ C	00	01	11	10
0	1	1	0	1
1	1	0	0	0

K-MAP FOR Y_3 (Red)

$$Y_3 = (A'B') + (AB'C') + (A'BC')$$

FULL VHDL DESIGN SOURCE CODE:

Lab2 - [C:/Users/PC-LIFE/Documents/Lab2/Lab2.xpr] - Vivado 2018.2

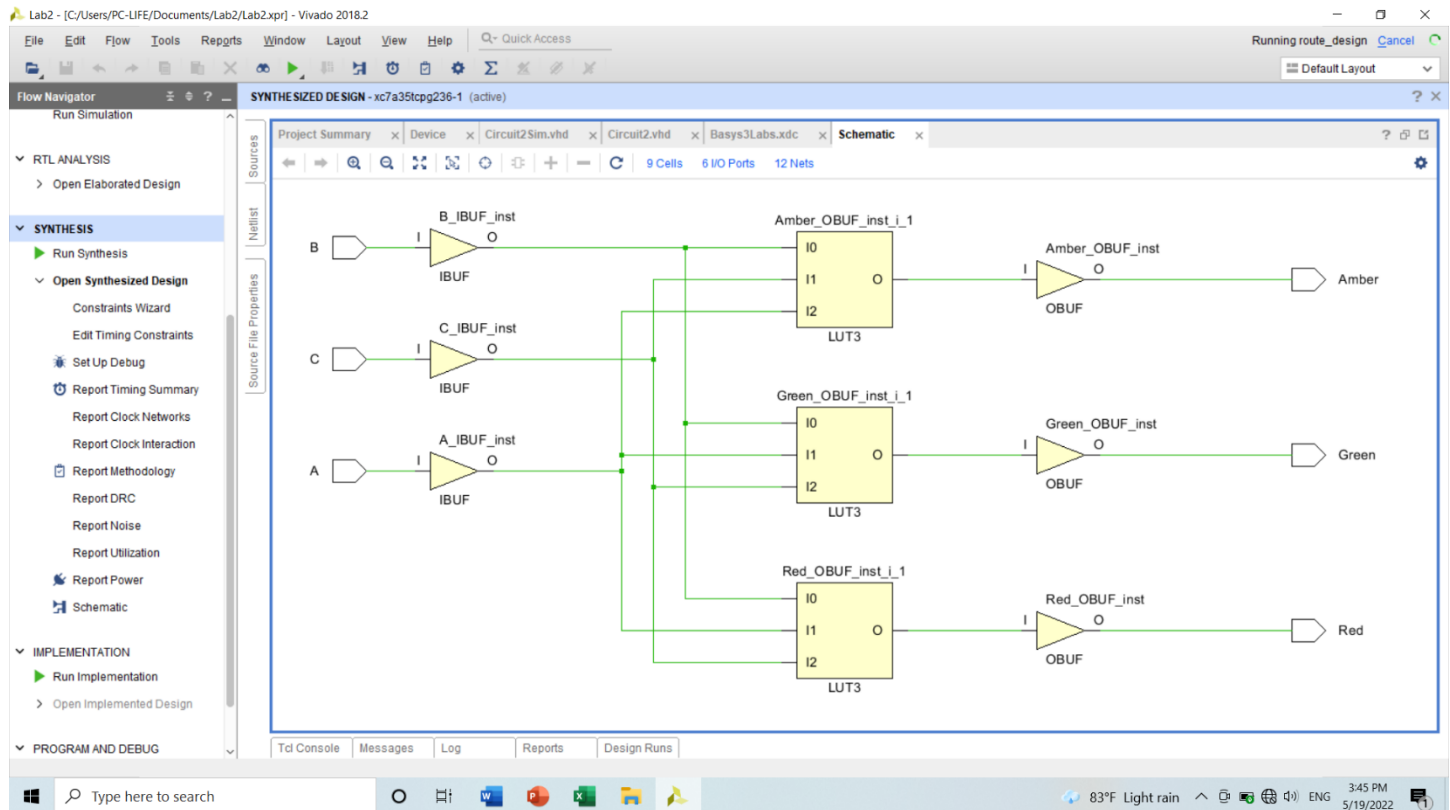
```

21 library IEEE;
22 use IEEE.STD_LOGIC_1164.ALL;
23
24 -- Uncomment the following library declaration if using
25 -- arithmetic functions with Signed or Unsigned values
26 --use IEEE.NUMERIC_STD.ALL;
27
28 -- Uncomment the following library declaration if instantiating
29 -- any Xilinx leaf cells in this code.
30 --library UNISIM;
31 --use UNISIM.VComponents.all;
32
33 entity Circuit2 is
34     Port (
35         A : in STD_LOGIC;
36         B : in STD_LOGIC;
37         C : in STD_LOGIC;
38         Red : out STD_LOGIC;
39         Amber : out STD_LOGIC;
40         Green : out STD_LOGIC;
41     );
42 end Circuit2;
43
44 architecture Behavioral of Circuit2 is
45 begin
46     Red <= ((NOT A) AND (NOT B)) OR (A AND (NOT B) AND (NOT C)) OR ((NOT A) AND (NOT C) AND B);
47     Amber <= (A AND B AND (NOT C)) OR ((NOT A) AND B AND C) OR (A AND (NOT B) AND C);
48     Green <= A AND B AND C;
49 end Behavioral;
50
51

```

49:1 Insert Sim Time: 1 us VHDL
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SCHEMATIC CIRCUIT FROM VIVADO:



TEST BENCH CODE:

```
Lab2 - [C:/Users/PC-LIFE/Documents/Lab2/Lab2.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help Quick Access
Running route_design Cancel
Default Layout

SYNTHESIZED DESIGN - xc7a35tpg236-1 (active)
Project Summary Device Circuit2Sim.vhd Circuit2.vhd Basys3Labs.xdc Schematic
9 Cells 6 I/O Ports 12 Nets

Sources
Netlist
Source File Properties

B IBUF B_IBUF_inst
C IBUF C_IBUF_inst
A IBUF A_IBUF_inst

Amber_OBUF_inst_i_1
Green_OBUF_inst_i_1
Red_OBUF_inst_i_1

Amber_OBUF_inst
Green_OBUF_inst
Red_OBUF_inst

Amber
Green
Red

Tcl Console Messages Log Reports Design Runs

Type here to search
83°F Light rain 3:45 PM 5/19/2022
```

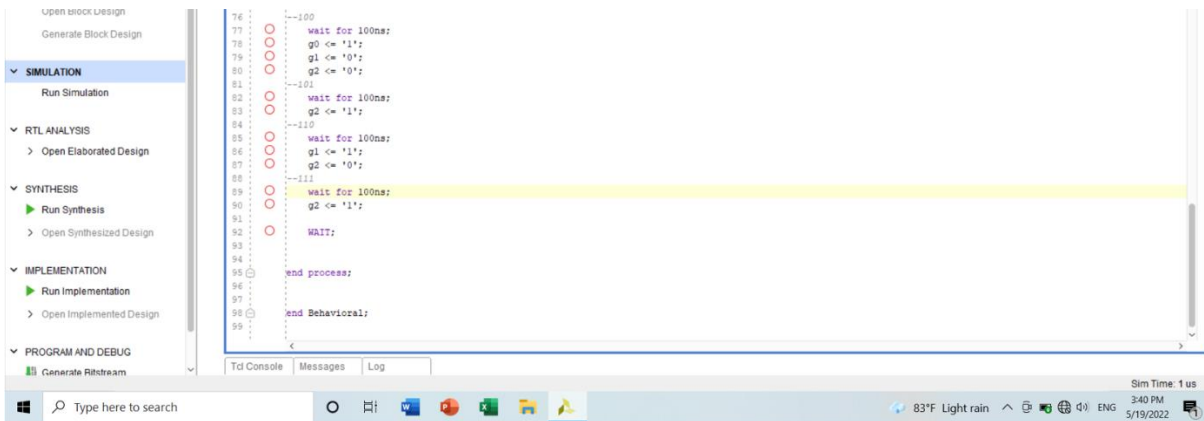


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Lab2 - [C:/Users/PC-LIFE/Documents/Lab2/Lab2.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Run Help Quick Access
Ready
Default Layout

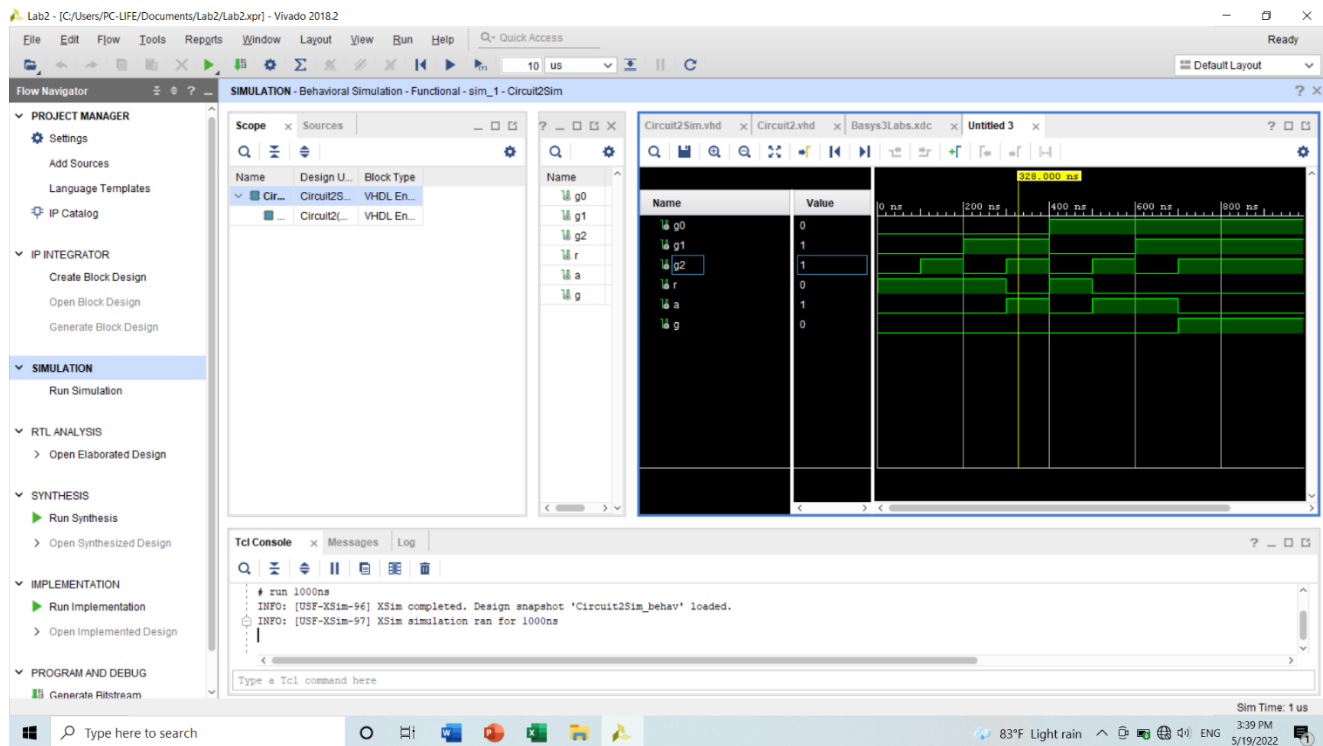
SIMULATION - Behavioral Simulation - Functional - sim_1 - Circuit2Sim
Project Manager Settings Add Sources Language Templates IP Catalog
IP INTEGRATOR Create Block Design Open Block Design Generate Block Design
SIMULATION Run Simulation
RTL ANALYSIS Open Elaborated Design
SYNTHESIS Run Synthesis Open Synthesized Design
IMPLEMENTATION Run Implementation

Circuit2Sim.vhd Circuit2.vhd Basys3Labs.xdc Untitled 3
C:/Users/PC-LIFE/Documents/Lab2/Lab2.srscs/sim_1/new/Circuit2Sim.vhd

22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Uncomment the following library declaration if using
26 -- arithmetic functions with Signed or Unsigned values
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity Circuit2Sim is
35     Port (
36     );
37 end Circuit2Sim;
38
39 architecture Behavioral of Circuit2Sim is
40     COMPONENT Circuit2
41     PORT(
42         A,B,C : IN STD_LOGIC;
43         Red,Amber,Green : OUT STD_LOGIC;
44     );
45     END COMPONENT;
46
47     signal g0,g1,g2 : STD_LOGIC;
48     signal i,a,g : STD_LOGIC;
49
50 begin
51     COUT : Circuit2 PORT MAP(
52         A => g0,
53         B => g1,
54         C => g2,
55         Red => i,
56         Amber => a,
57         Green => g
58     );
59
60 process
61 begin
62     --000
63     g0 <= '0';
64     g1 <= '0';
65     g2 <= '0';
66     wait for 100ns;
67     g2 <= '1';
68
69     --010
70     wait for 100ns;
71     g1 <= '1';
72     g2 <= '0';
73
74     --011
75     wait for 100ns;
76     g2 <= '1';
```



TIMING DIAGRAM FROM XSIM SHOWING ALL POSSIBLE INPUTS AND OUTPUTS:



CONCLUSIONS:

- The output of a logic can be identified using a truth table considering all possible scenarios of inputs.
- The logic displayed in truth table can be converted into Boolean terms using the method of min-term canonical sum of products.
- Using a Karnaugh map, a Boolean expression can be further simplified for the ease of use.
- Schematic diagram can be obtained using Vivado software as per the design source. (Here it was coded in VHDL.)
- Vivado's behavioral simulation allows to verify the proper functionality of every RTL module in a design at anytime. (without needing to run synthesis or implementation)
- It runs a specified testbench module (where the logic inputs are mapped to simulation's variables and the simulation procedure is structured in a timely manner) and then displays the logic of the testbench's results in a waveform window.