

COMBINATIONAL CIRCUITS

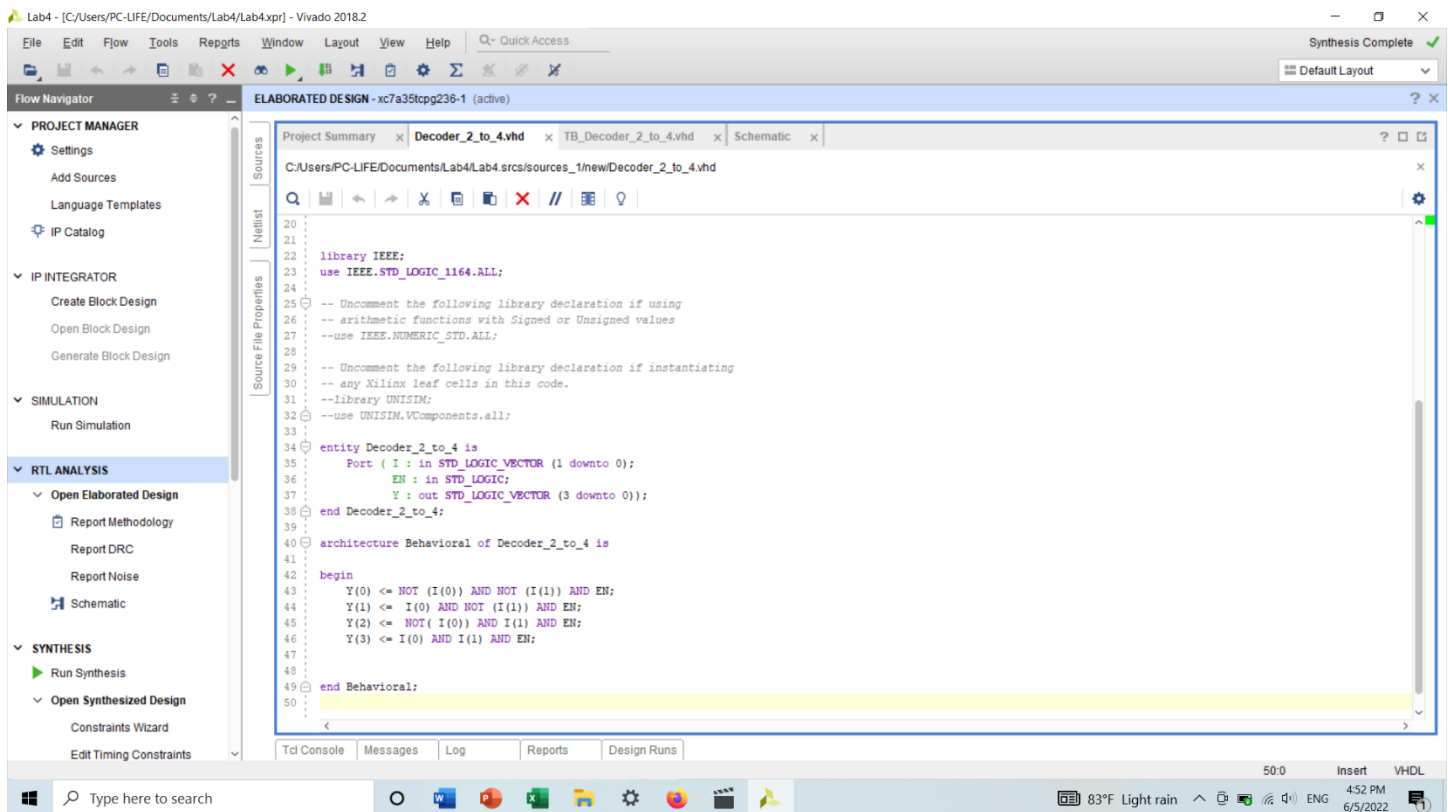
LAB 04 REPORT

Task Assigned:

1. Analyze the functionality of decoder and multiplexer.
2. Design and develop a 2 to 4 decoder in VHDL using Vivado software.
3. Design and develop 3 to 8 decoder using 2 of above 2 to 4 decoders.
4. Design and develop 8 to 1 multiplexer using the 3 to 8 decoder.
5. Verify the functionality of each of above 3 circuits via a simulation using input combinations as per the numbers in the index number

VHDL Source Codes

01.VHDL Code for 2 to 4 decoder



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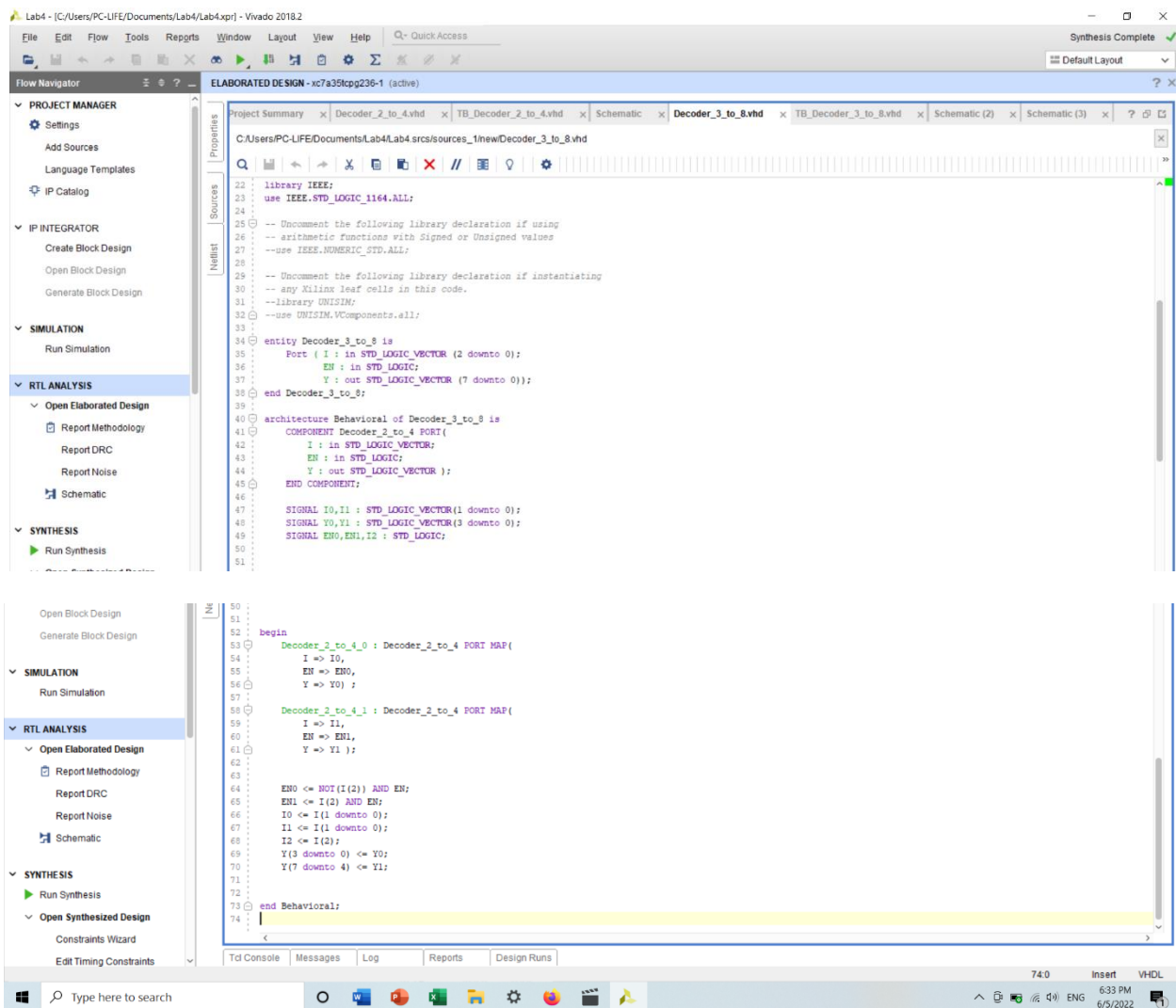
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IP INTEGRATOR
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C:/Users/PC-LIFE/Documents/Lab4/Lab4.srca/sources_1/new/Decoder_2_to_4.vhd
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22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Uncomment the following library declaration if using
26 -- arithmetic functions with Signed or Unsigned values
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity Decoder_2_to_4 is
35     Port ( I : in STD_LOGIC_VECTOR (1 downto 0);
36           EN : in STD_LOGIC;
37           Y : out STD_LOGIC_VECTOR (3 downto 0));
38 end Decoder_2_to_4;
39
40 architecture Behavioral of Decoder_2_to_4 is
41
42 begin
43     Y(0) <= NOT (I(0)) AND NOT (I(1)) AND EN;
44     Y(1) <= I(0) AND NOT (I(1)) AND EN;
45     Y(2) <= NOT (I(0)) AND I(1) AND EN;
46     Y(3) <= I(0) AND I(1) AND EN;
47
48
49 end Behavioral;
50

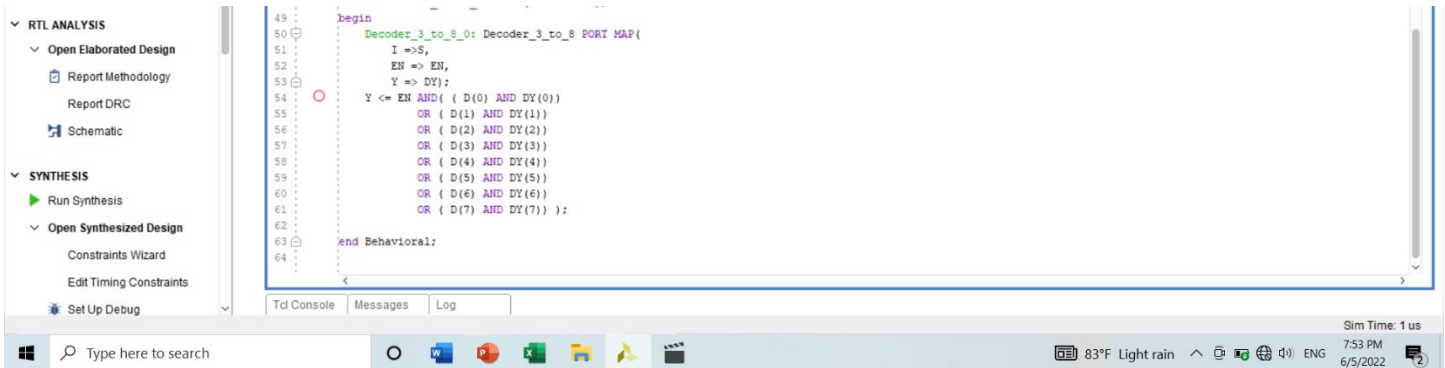
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02.VHDL Code for 3 to 8 decoder



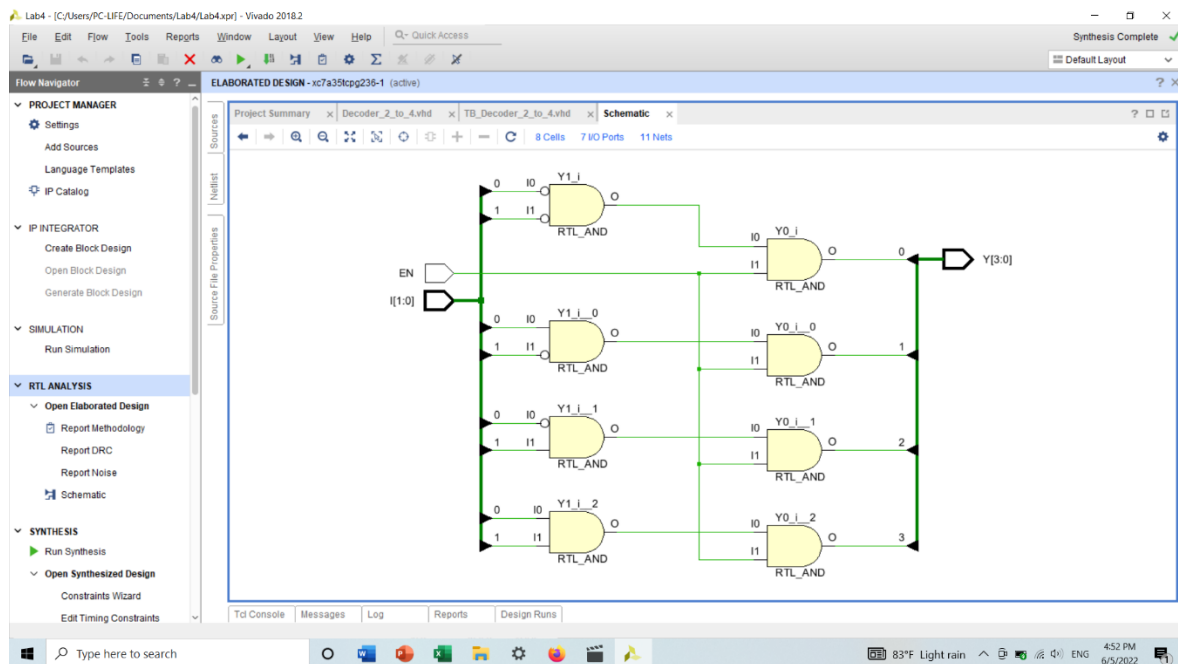
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Project Summary Decoder_2_to_4.vhd TB_Decoder_2_to_4.vhd Schematic Decoder_3_to_8.vhd TB_Decoder_3_to_8.vhd Schematic (2) Schematic (3)
C:/Users/PC-LIFE/Documents/Lab4/Lab4.srscs/sources_1/new/Decoder_3_to_8.vhd
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Uncomment the following library declaration if using
26 -- arithmetic functions with Signed or Unsigned values
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity Decoder_3_to_8 is
35     Port ( I : in STD_LOGIC_VECTOR (2 downto 0);
36           EN : in STD_LOGIC;
37           Y : out STD_LOGIC_VECTOR (7 downto 0));
38 end Decoder_3_to_8;
39
40 architecture Behavioral of Decoder_3_to_8 is
41     COMPONENT Decoder_2_to_4 PORT(
42         I : in STD_LOGIC_VECTOR;
43         EN : in STD_LOGIC;
44         Y : out STD_LOGIC_VECTOR );
45     END COMPONENT;
46
47     SIGNAL I0,I1 : STD_LOGIC_VECTOR(1 downto 0);
48     SIGNAL Y0,Y1 : STD_LOGIC_VECTOR(3 downto 0);
49     SIGNAL EN0,EN1,I2 : STD_LOGIC;
50
51 begin
52     Decoder_2_to_4_0 : Decoder_2_to_4 PORT MAP(
53         I => I0,
54         EN => EN0,
55         Y => Y0 );
56
57     Decoder_2_to_4_1 : Decoder_2_to_4 PORT MAP(
58         I => I1,
59         EN => EN1,
60         Y => Y1 );
61
62     EN0 <= NOT(I(2)) AND EN;
63     EN1 <= I(2) AND EN;
64     I0 <= I(1 downto 0);
65     I1 <= I(1 downto 0);
66     I2 <= I(2);
67     Y(3 downto 0) <= Y0;
68     Y(7 downto 4) <= Y1;
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70 end Behavioral;
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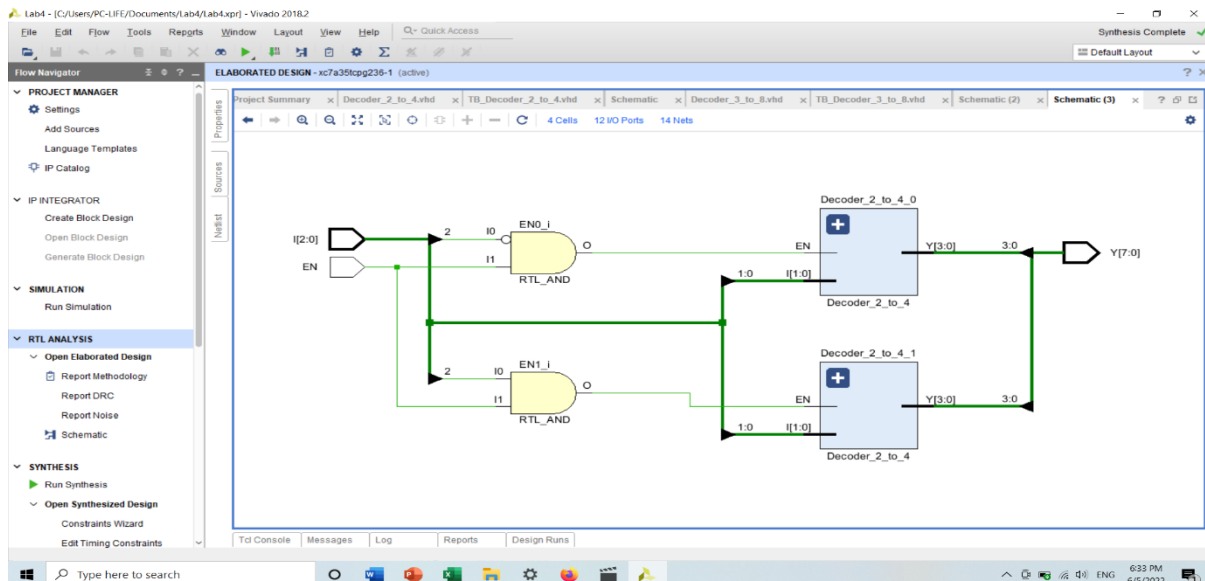


RTL Analysis Elaborated Design Schematics

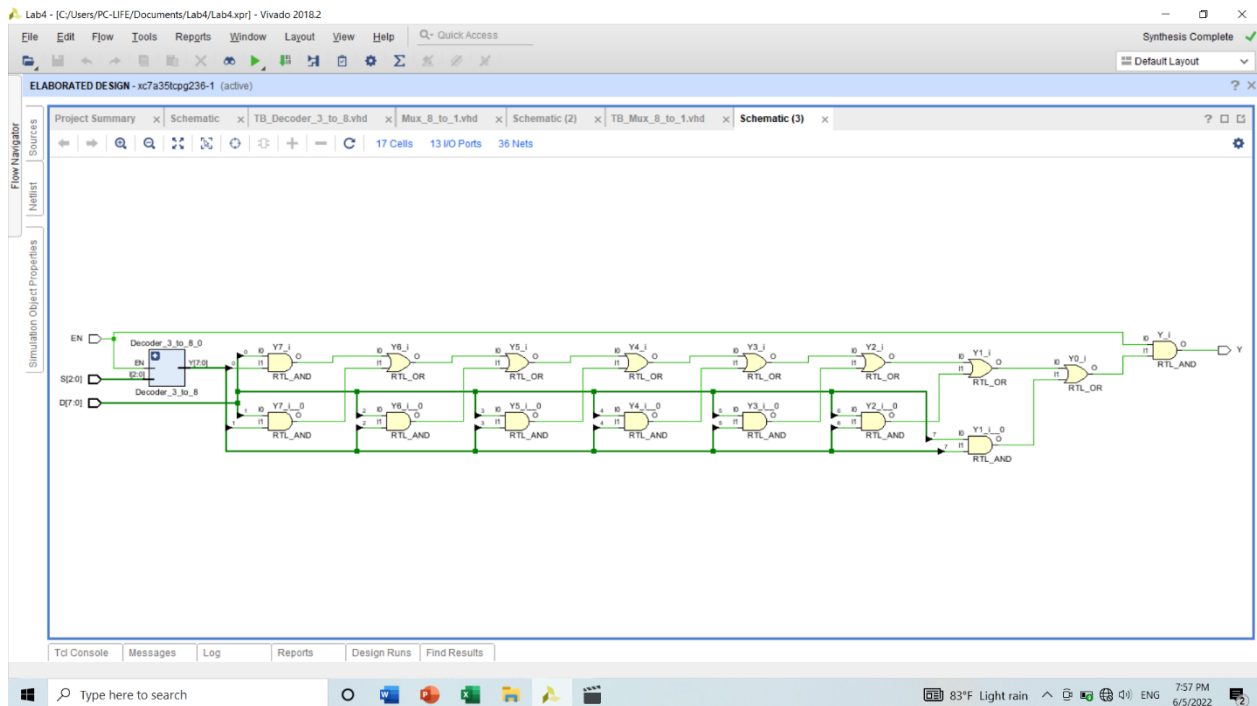
01.RTL Schematic for 2 to 4 Decoder



02.RTL Schematic for 3 to 8 Decoder

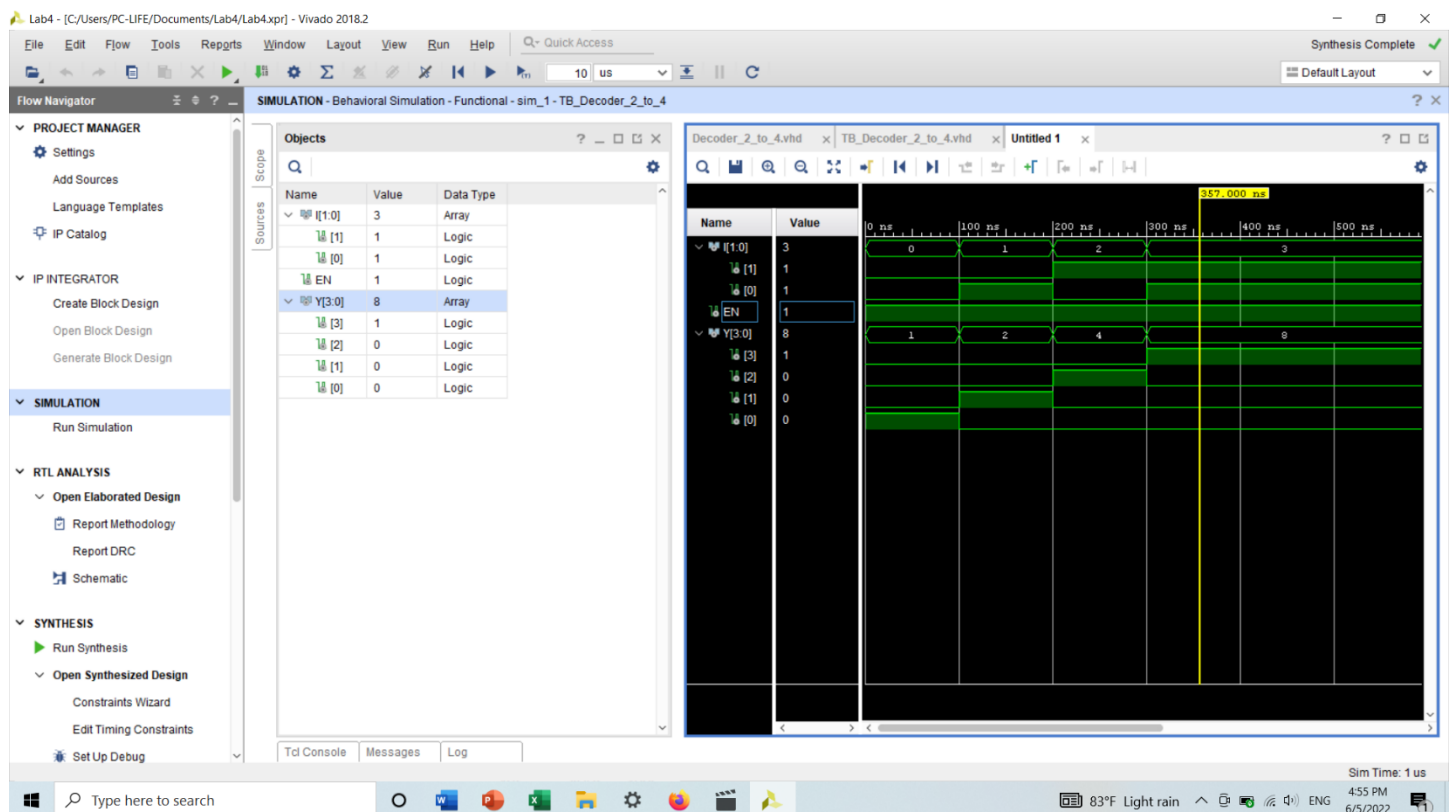


03.RTL Schematic for 8 to 1 Multiplexer

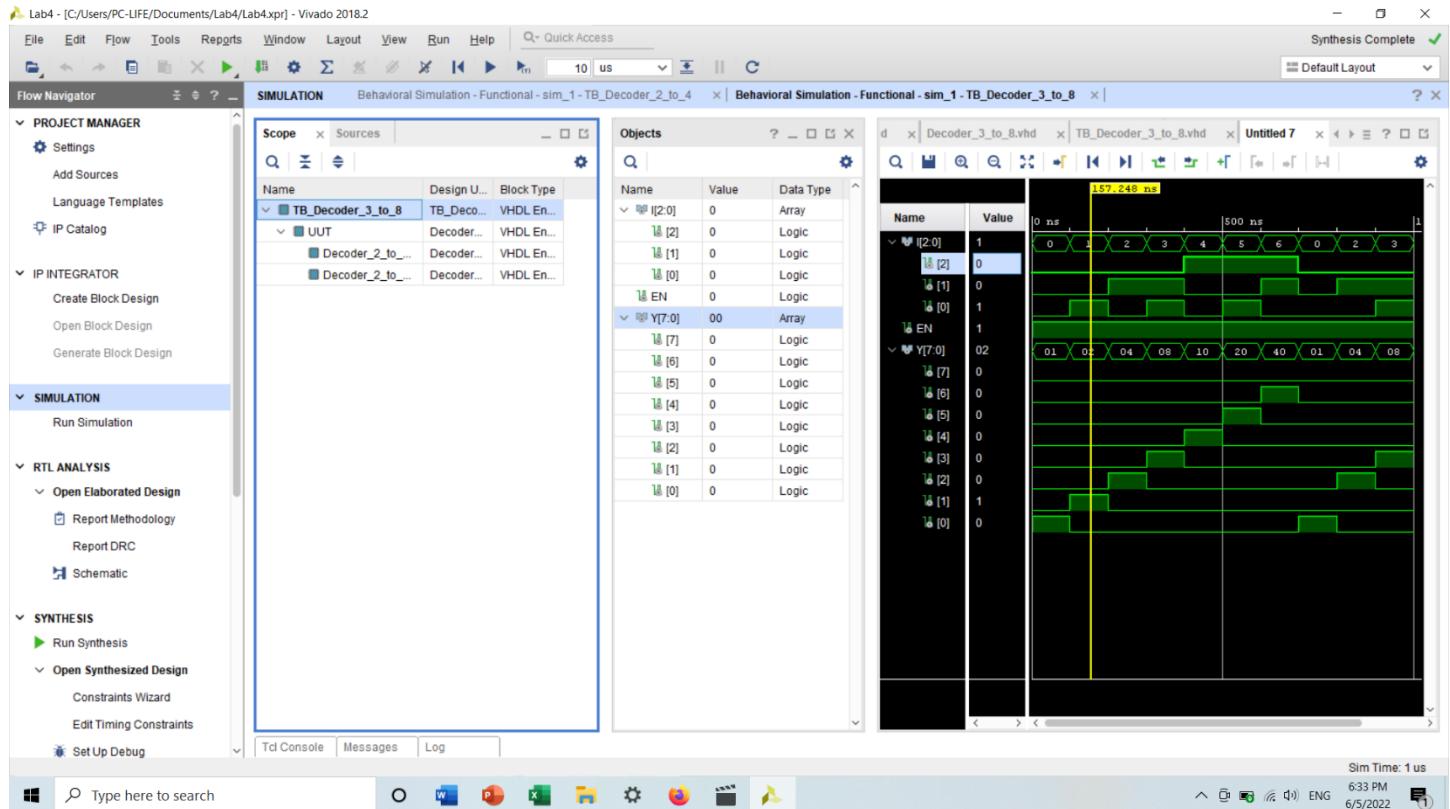


Timing Diagrams

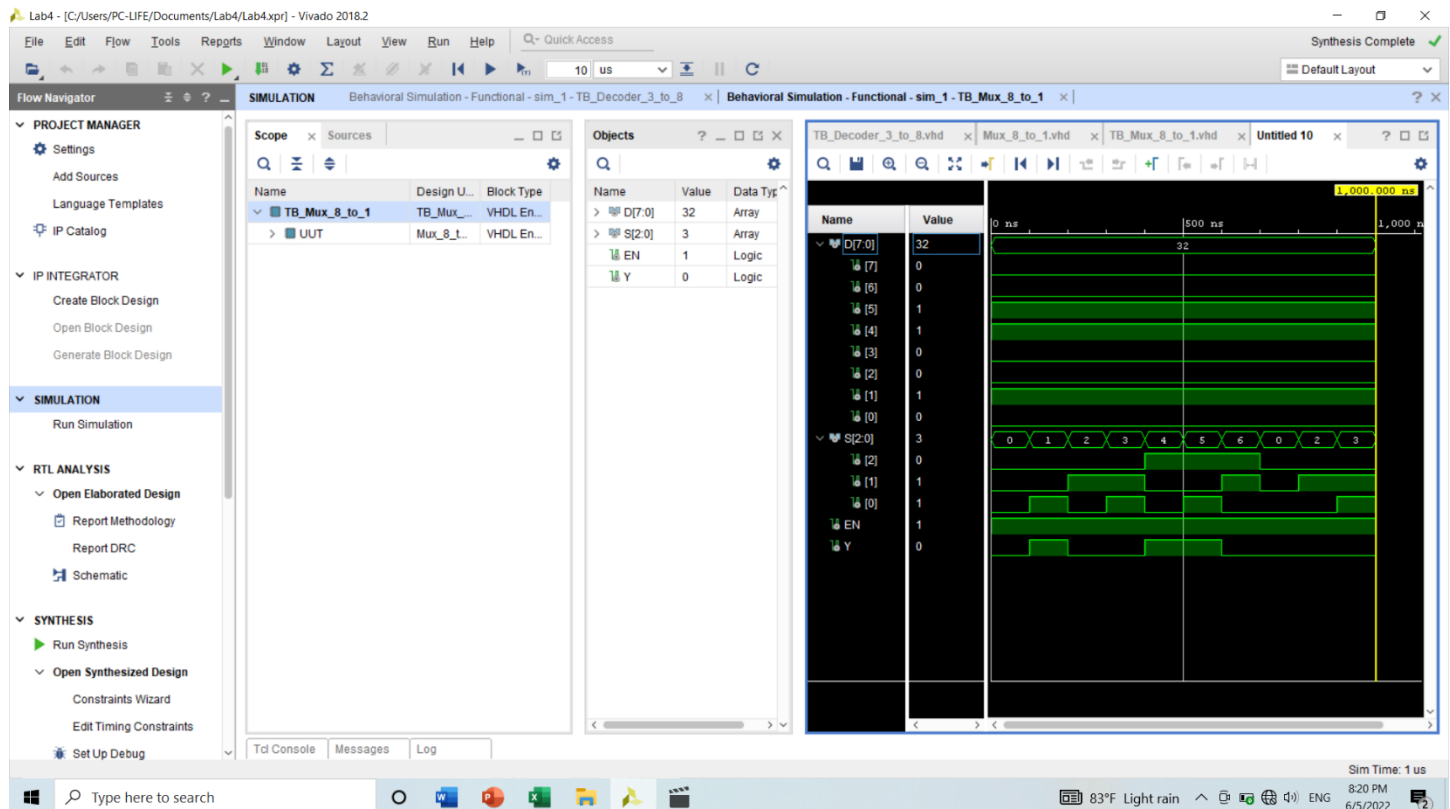
01.Timing Diagram for 2 to 4 decoder



02. Timing Diagram for 3 to 8 decoder

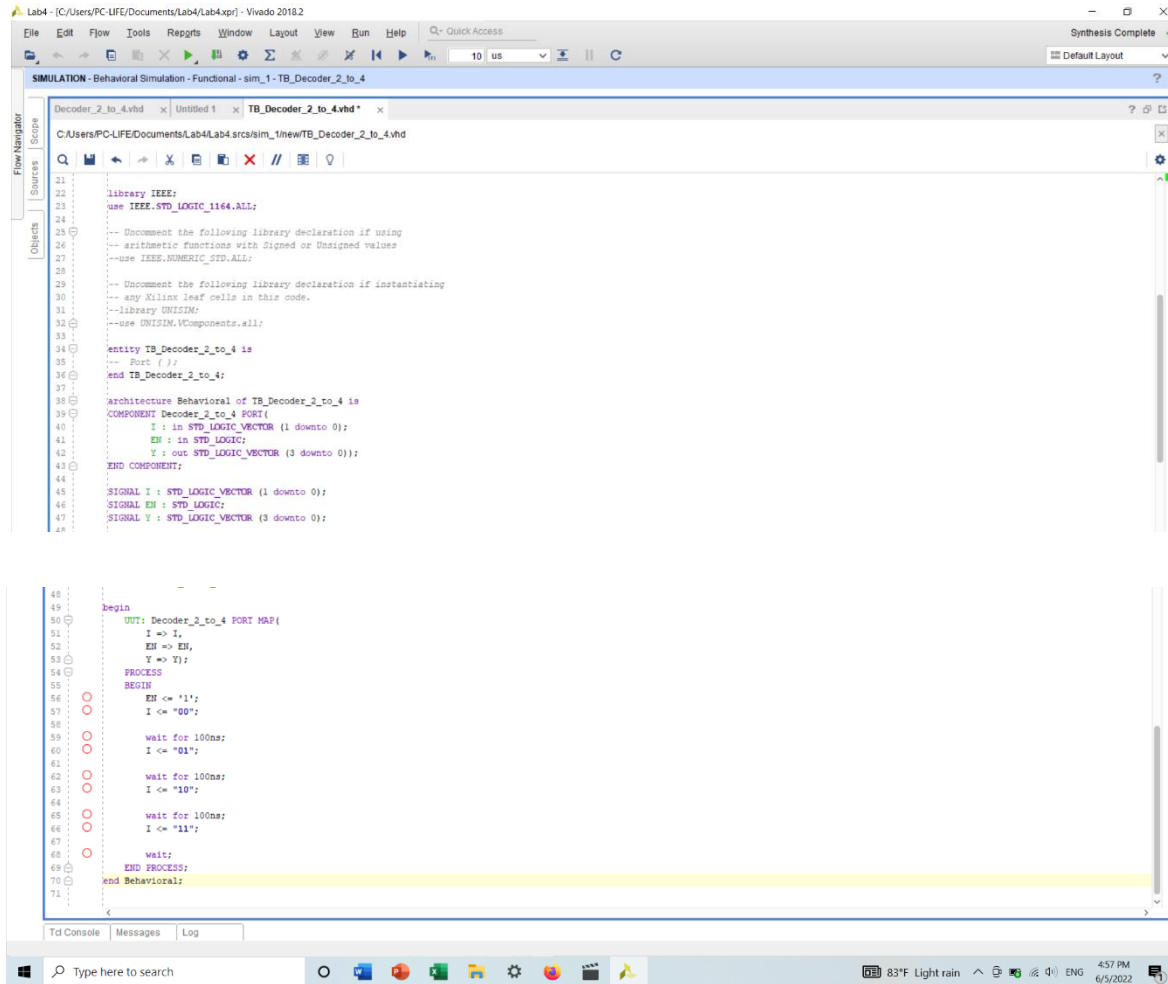


03. Timing Diagram for 8 to 1 multiplexer



Test Bench Codes

01. Test Bench code for 2 to 4 decoder's simulation



The screenshot displays the Vivado IDE interface for a project named 'Lab4'. The main editor window shows the test bench code for a 2-to-4 decoder simulation. The code is written in VHDL and includes the following sections:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Document the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Document the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_Decoder_2_to_4 is
    Port (
        --
    end TB_Decoder_2_to_4;

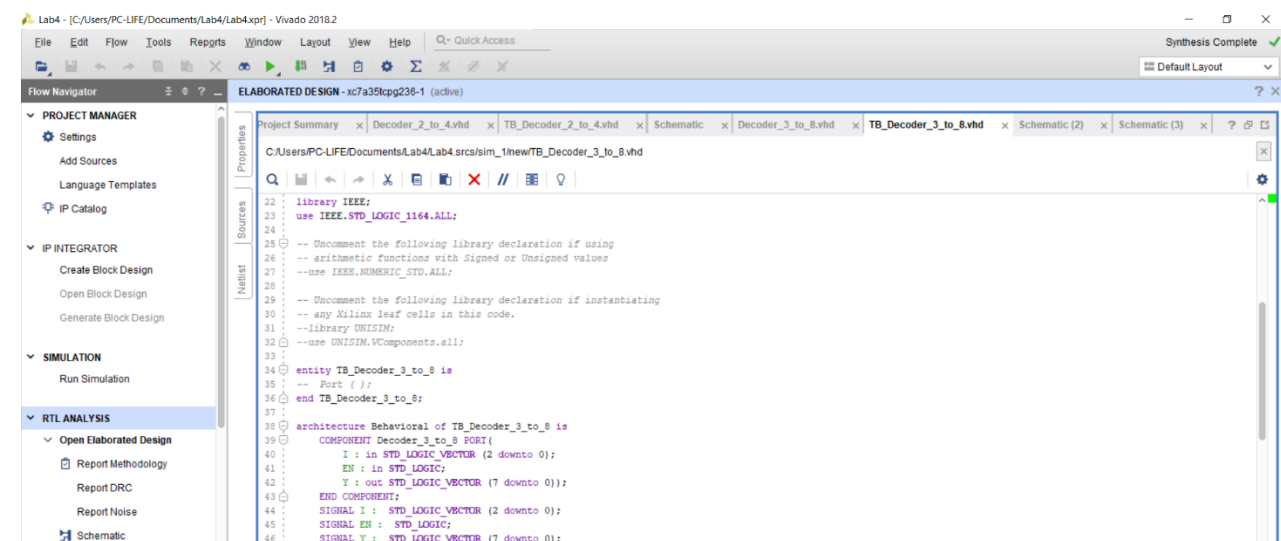
architecture Behavioral of TB_Decoder_2_to_4 is
    COMPONENT Decoder_2_to_4 PORT(
        I : in STD_LOGIC_VECTOR (1 downto 0);
        EN : in STD_LOGIC;
        Y : out STD_LOGIC_VECTOR (3 downto 0));
    END COMPONENT;

    SIGNAL I : STD_LOGIC_VECTOR (1 downto 0);
    SIGNAL EN : STD_LOGIC;
    SIGNAL Y : STD_LOGIC_VECTOR (3 downto 0);

begin
    --
    OUT: Decoder_2_to_4 PORT MAP(
        I => I,
        EN => EN,
        Y => Y);
    PROCESS
    BEGIN
        EN <= '1';
        I <= "00";
        wait for 100ns;
        I <= "01";
        wait for 100ns;
        I <= "10";
        wait for 100ns;
        I <= "11";
        wait;
    END PROCESS;
end Behavioral;
```

The code defines a test bench entity 'TB_Decoder_2_to_4' that instantiates the 'Decoder_2_to_4' component. It sets up signals for inputs 'I' and 'EN', and output 'Y'. The test process applies a sequence of input values to 'I' while 'EN' is high, and waits for 100ns between each input change. The test process is enclosed in a 'PROCESS' block and ends with 'END Behavioral;'.

02. Test Bench code for 3 to 8 decoder's simulation



The screenshot displays the Vivado IDE interface for a project named 'Lab4'. The main editor window shows the test bench code for a 3-to-8 decoder simulation. The code is written in VHDL and includes the following sections:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Document the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Document the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

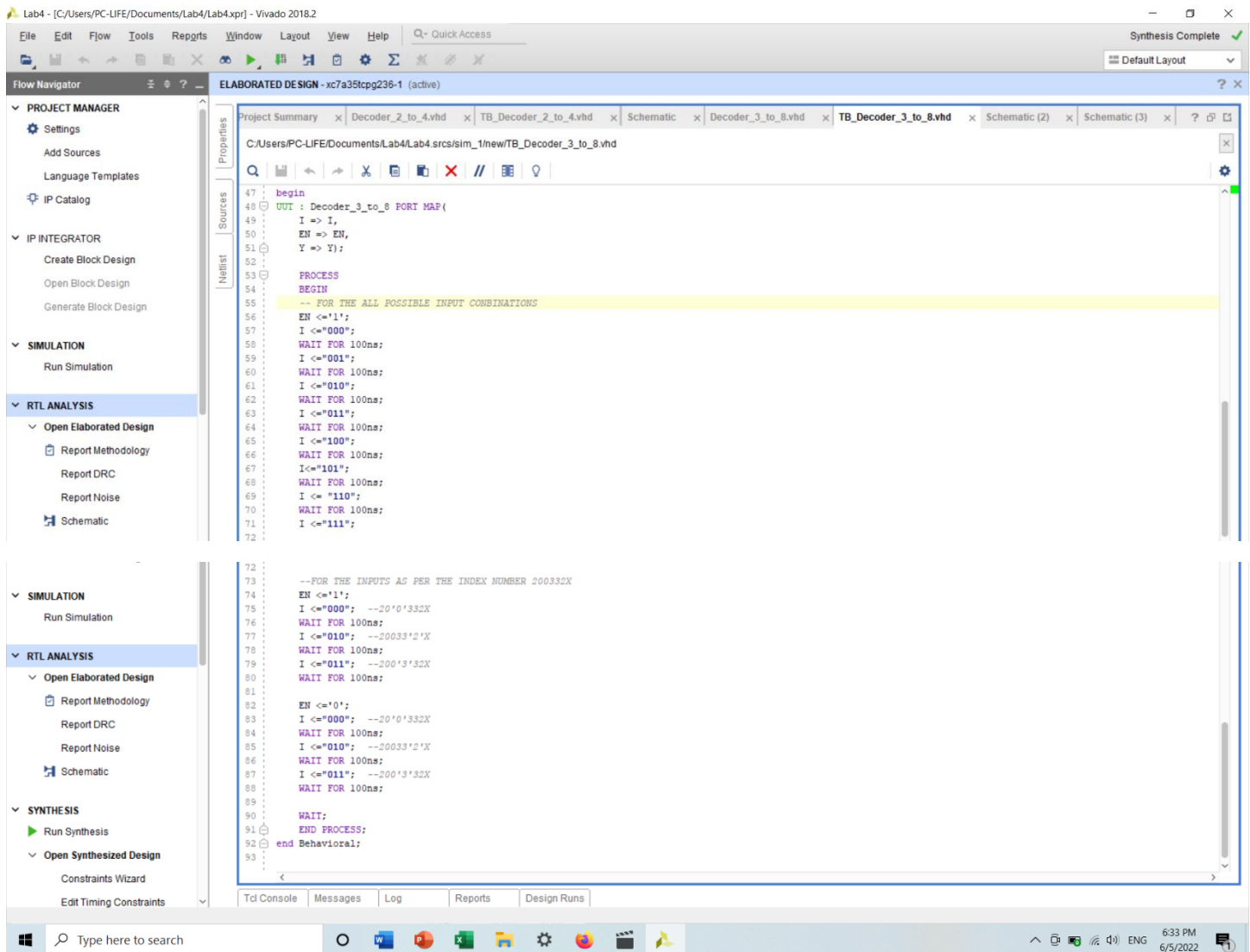
entity TB_Decoder_3_to_8 is
    Port (
        --
    end TB_Decoder_3_to_8;

architecture Behavioral of TB_Decoder_3_to_8 is
    COMPONENT Decoder_3_to_8 PORT(
        I : in STD_LOGIC_VECTOR (2 downto 0);
        EN : in STD_LOGIC;
        Y : out STD_LOGIC_VECTOR (7 downto 0));
    END COMPONENT;

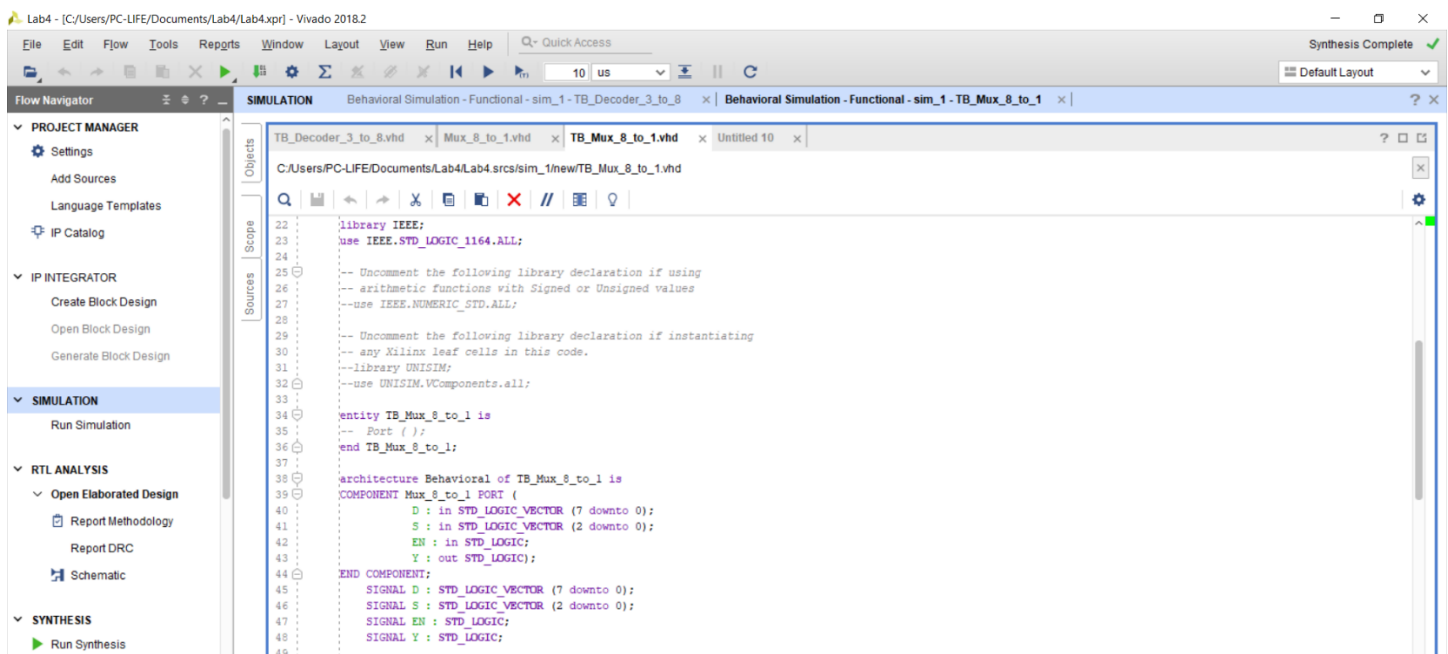
    SIGNAL I : STD_LOGIC_VECTOR (2 downto 0);
    SIGNAL EN : STD_LOGIC;
    SIGNAL Y : STD_LOGIC_VECTOR (7 downto 0);

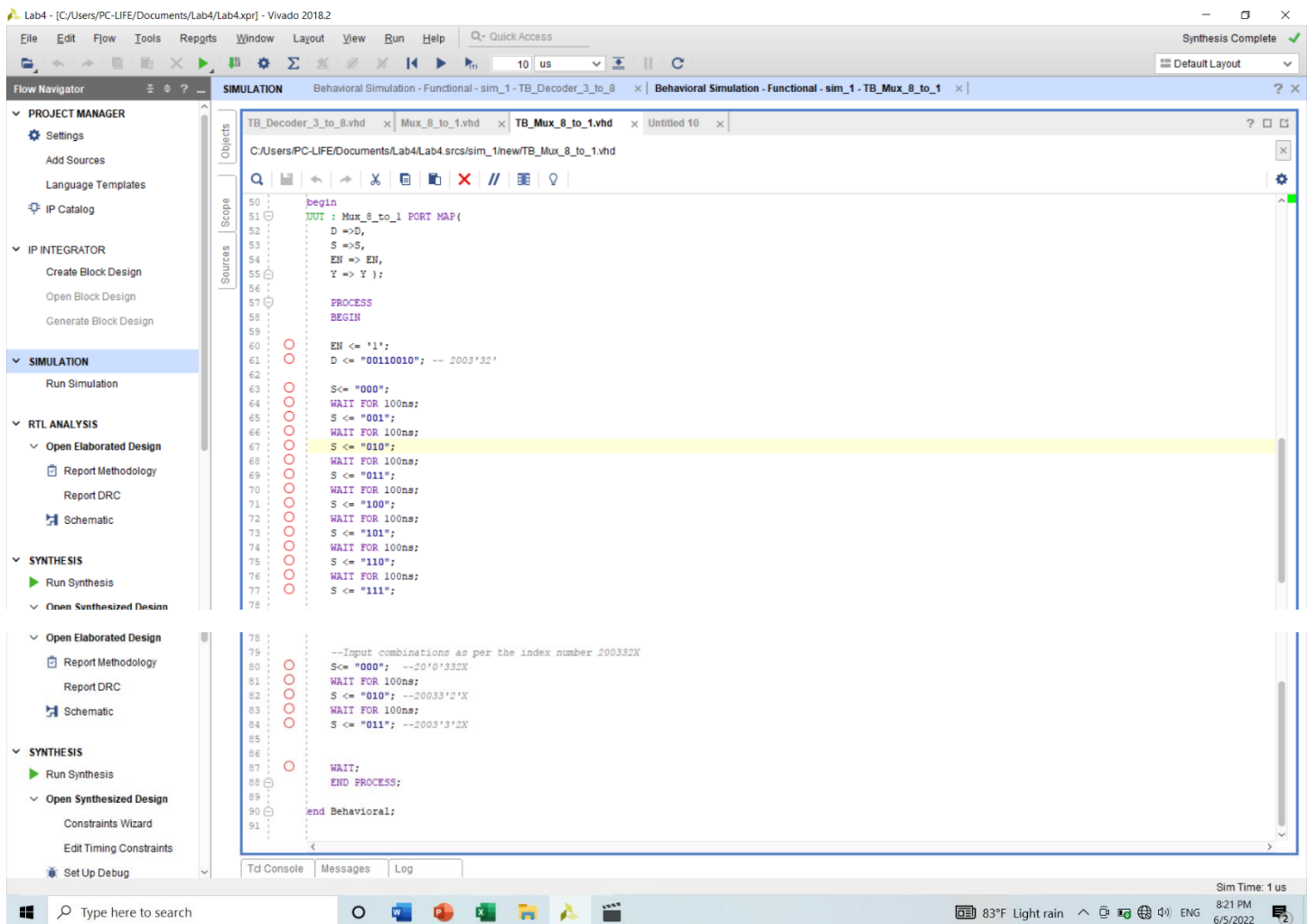
begin
    --
end Behavioral;
```

The code defines a test bench entity 'TB_Decoder_3_to_8' that instantiates the 'Decoder_3_to_8' component. It sets up signals for inputs 'I' and 'EN', and output 'Y'. The test process is not fully visible in the screenshot, but it follows a similar pattern to the 2-to-4 decoder test bench, applying input values to 'I' while 'EN' is high.



03. Test Bench code for 8 to 1 Multiplexer





Conclusions:

- A decoder converts binary data from n coded inputs to a maximum of 2^n unique outputs. *[In this lab 2 to 4 decoder (2^2) & a 3 to 8 decoder (2^3) is created]*
- A multiplexer receives binary data from 2^n lines and connect them to a single output line based on a given n bit selection. *[In this lab 8 to 1 multiplexer is created ($2^3 \rightarrow 1$)]*
- 3 to 8 decoders can be designed using two 2 to 4 decoders.
- 8 to 1 multiplexer can be designed using a 3 to 8 decoder.
- Functionality of circuits can be verified with a clear visualization using Vivado's simulation process.