Course Code	Course Title	L	T	P	J	C
ECE3002	VLSI SYSTEM DESIGN	3	0	2	0	4
Prerequisite:	ECE2003 Digital Logic Design					

Course Objectives:

- To illustrate the basic concepts of modern VLSI circuit design.
- Describe the fundamental principles underlying digital design using CMOS logic and analyze the performance characteristics of these digital circuits.
- Verify that a design meets its functionality, timing constraints, both manually and through the use of computer-aided design tools.
- Develop problem-solving skills in order to be able to successfully approach a digital design project of medium to high complexity in the final semester.

Expected Course Outcome:

The Students will be able to

- Design and analyze the performance (Speed, Power) of CMOS digital integrated circuits for different design specifications.
- Identify and interpret the design towards realizing digital IC design.
- Use modern EDA tools to simulate and synthesize the digital designs.

Student Learning Outcomes (SLO):	2,5,14

Module:1	MOS Transistor Theory:	6 hours	SLO: 2

I-V Characteristics, C-V Characteristics, Non ideal I-V effects of MOS Transistors

Module:2	CMOS Logic:	4 hours	SLO: 2

Basic gates, Compound Gates, Transmission Gates based combinational and sequential logic design

Module:3	CMOS Circuit characterization and Performance Estimation :	4 hours	SLO: 2

DC transfer Characteristics of CMOS inverter, Circuit characterization and performance estimation: Delay estimation, Logical effort and Transistor Sizing. Power Dissipation: Static & Dynamic Power Dissipation.

Module:4	CMOS Fabrication and Layout:	2 hours	SLO: 5

CMOS Process Technology N-well, P-well process, Stick diagram for Boolean functions using Euler Theorem, Layout Design Rule

Module:5	CMOS Combinational Circuit Design:	4 hours	SLO: 5

Static CMOS, Ratioed Logic, Cascode voltage Switch Logic, Dynamic circuits, Pass Transistor Circuits

Module:6	**CMOS Sequential Circuit Design:**	**4 hours**	**SLO: 5**
Conventional CMOS Latches and Flip Flops, Pulsed Latches, Resettable and Enabled Latches and Flip Flops			
Module:7	**Sub System Design:**	**4 hours**	**SLO: 5**
Single bit Adder, Carry look ahead adder, Carry propagate Adder, Magnitude Comparator, Barrel Shifter, Signed and unsigned multiplier.			
Module:8	**Contemproray Issues**	**2 hours**	
	Total Lecture Hours:	**30 hours**	

Text Books:

1.	Neil H.Weste, Harris, A. Banerjee, "CMOS VLSI Design, A circuits and System Perspective", 2014, Fourth Edition, Pearson Education, Noida, India.

Reference Books:

1.	Jan M. Rabaey, Anantha Chadrakasan, BorivojeNikolic, "Digital Integrated Circuits: A Design Perspective", 2014, Third Edition, Prentice Hall India, New Jersey, US.
2.	Yogesh Chauhan, Darsen Duane Lu, Vanugopalan Sriramkumar, Sourabh Khandelwal, Juan Duarte, NavidPayvadosi, Ai Niknejad, Chenming Hu, "FinFETModeling for IC Simulation and Design", 2015, Academic Press, Elsevier.

Mode of Evaluation: Continuous Assessment Test –I (CAT-I), Continuous Assessment Test –II (CAT-II), Digital Assignments/ Quiz / Completion of MOOC, Final Assessment Test (FAT).

Sl.No.	**List of Challenging Experiemnts (Indicative):**	**SLO:14**
1	i. Cadence EDA Tool Demo & Hands on - Schematic ii. Basic Cell structure (NMOS & PMOS) using conventional MOS iii. Verification with different corners iv. Design and Analysis of CMOS circuits (Analysis: Power, Delay, NM, PDP) (Design: Sizing)	8 hours
2	i. Cadence EDA Tool Demo & Hands on – Layout & Post Layout Simulation ii. Basic Cell layout (CMOS) iii. Fingering and folding iv. Standard cell design for different technology node	8 hours
3	i. Adder Design using conventional CMOS ii. Multiplier using conventional CMOS iii. Memory design (SRAM /DRAM /CAM). iv. Level converters (Optional)	8 hours

4	i. ALU Design using conventional CMOS ii. Simple Processor Design using conventional CMOS	6 hours
	Total Laboratory Hours:	**30 hours**
Mode of Evaluation: Continuous Assessment of Challenging experiments / Final Assessment Test (FAT).		