

Microprocessor and Computer Architecture

UE20CS252

4th Semester, Academic Year 2021-22

Date: 31/01/2022

Name: Vishwa Mehul Mehta	SRN: PES2UG20CS389	Section: F
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Week#3

Program Number: 1

Title of the Program

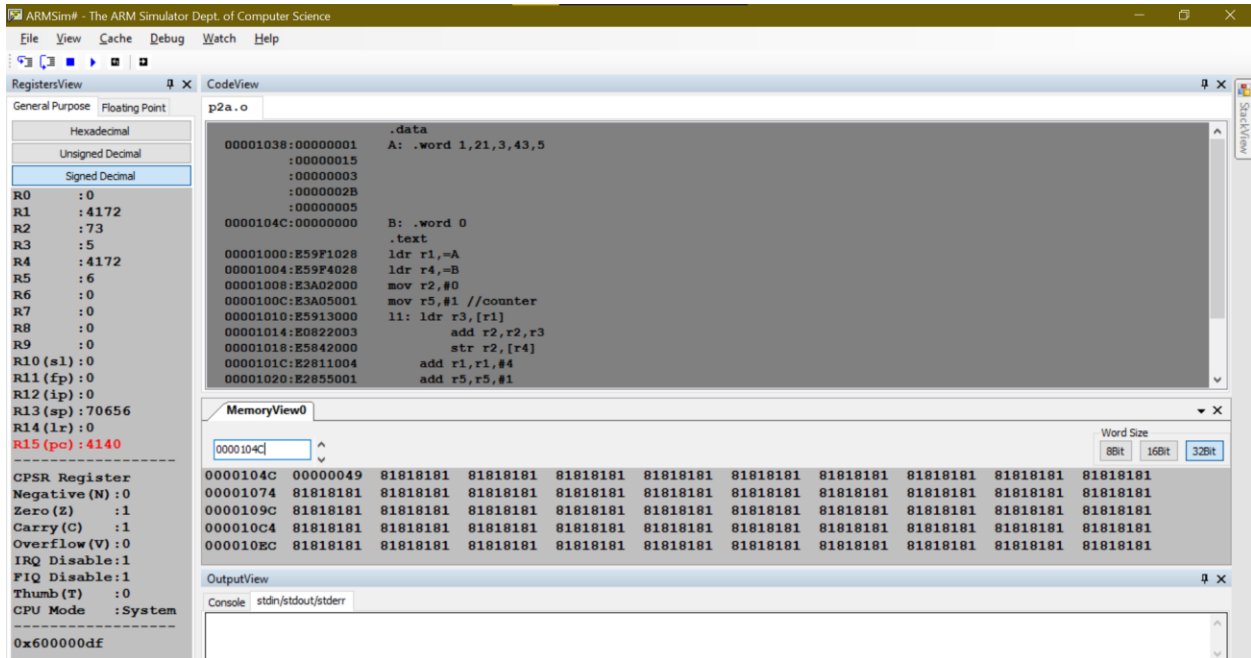
Write a program in ARM7TDMI-ISA to find the sum of N data items in the memory. Store the result in the memory location.

a. Use Full word (.word directive)

I. ARM Assembly Code:

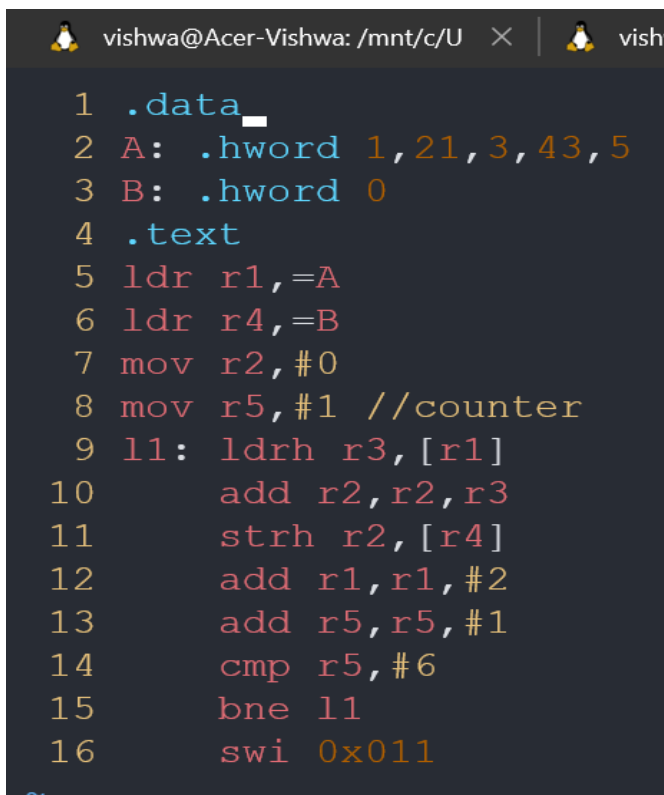
```
vishwa@Acer-Vishwa: /mnt/c/U  × |  
1  .data  
2  A:  .word 1,21,3,43,5  
3  B:  .word 0  
4  .text  
5  ldr r1,=A  
6  ldr r4,=B  
7  mov r2,#0  
8  mov r5,#1 //counter  
9  l1: ldr r3,[r1]  
10     add r2,r2,r3  
11     str r2,[r4]  
12     add r1,r1,#4  
13     add r5,r5,#1  
14     cmp r5,#6  
15     bne l1  
16     swi 0x011
```

II. Output Screen Shot:

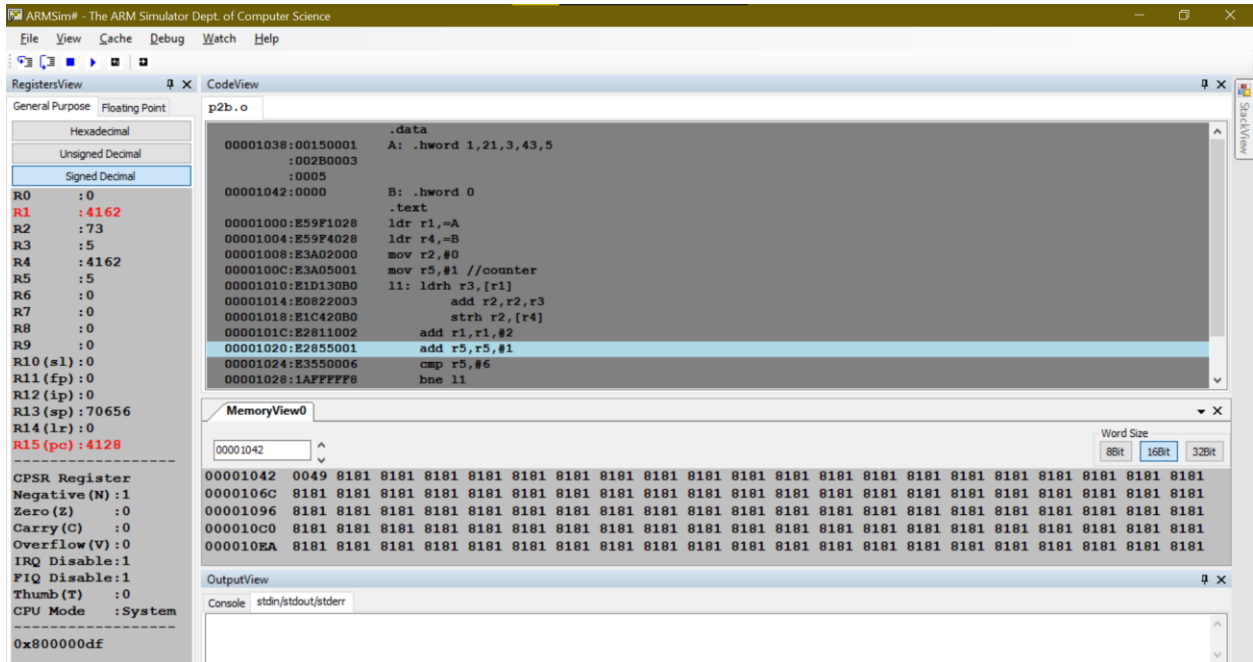


b. Use Half word(.Hword directive)

I. ARM Assembly Code:



II. Output Screen Shot:

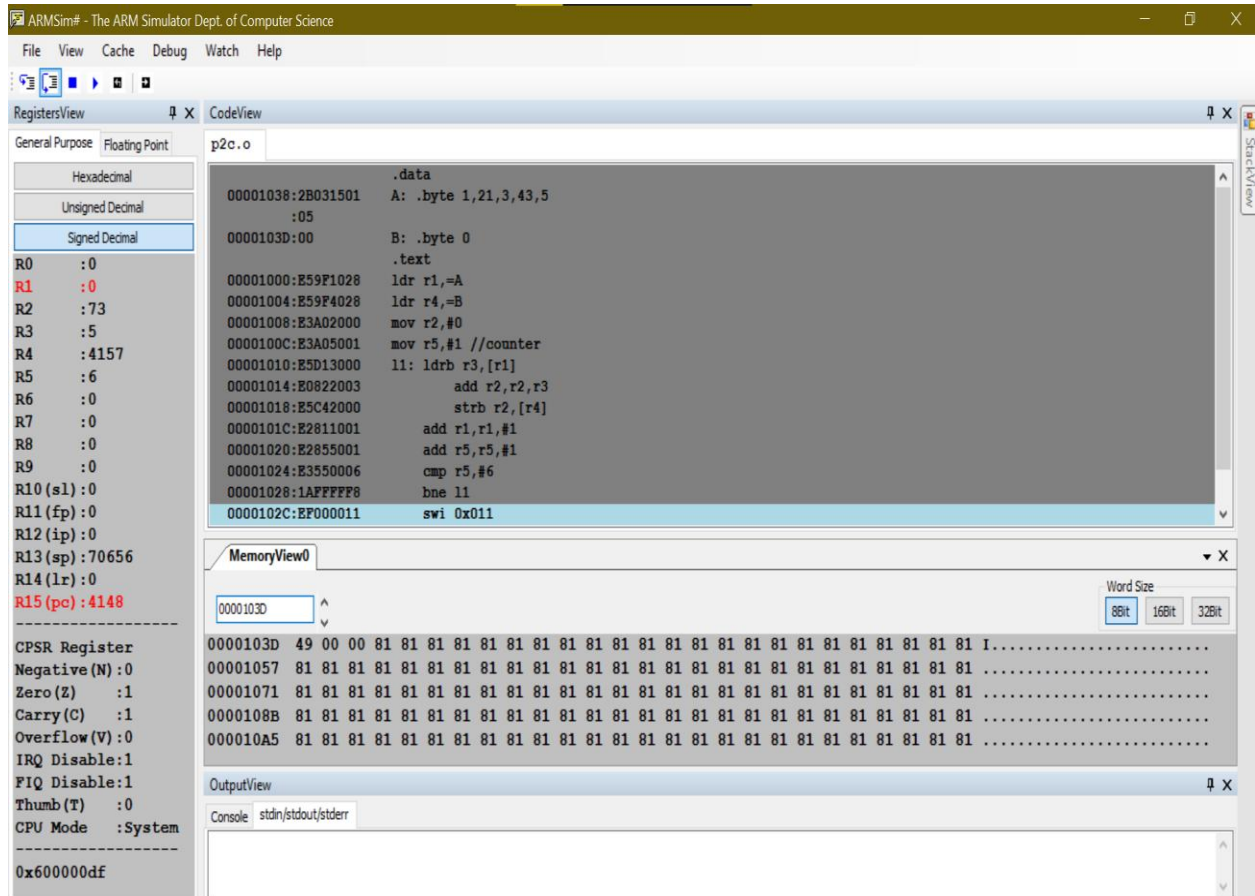


c. Use Byte wise (.Byte directive)

III. ARM Assembly Code:

```
1 .data
2 A: .byte 1,21,3,43,5
3 B: .byte 0
4 .text
5 ldr r1,=A
6 ldr r4,=B
7 mov r2,#0
8 mov r5,#1 //counter
9 l1: ldrb r3,[r1]
10     add r2,r2,r3
11     strb r2,[r4]
12     add r1,r1,#1
13     add r5,r5,#1
14     cmp r5,#6
15     bne l1
16     swi 0x011
```

IV. Output Screen Shot:



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Week#3

Program Number: 2

Title of the Program

Write a program in ARM7TDMI-ISA to find the sum of N natural numbers. Store the result in the memory location.

I. ARM Assembly Code:

```
vishwa@Acer-Vishwa: /mnt/c/U  × |
1  .data
2  B: .word 0
3  .text
4  ldr r4, =B
5  mov r2, #0
6  mov r5, #1
7  l1: add r2, r2, r5
8      str r2, [r4]
9      add r5, r5, #1
10     cmp r5, #6
11     bne l1
12     swi 0x011
~
```

II. Output Screen Shot:

The screenshot displays the ARMSim# - The ARM Simulator interface, which includes several panels for monitoring the system's state.

RegistersView: This panel shows the current state of the ARM registers. The General Purpose registers (R0-R15) are listed, with R15 (PC) highlighted in red at address 4128. The CPSR Register is also shown, indicating the current processor mode is System.

CodeView: This panel displays the assembly code being executed. The code is organized into sections: .data, .text, and .bss. The current instruction being executed is `swi 0x011` at address 00001020.

MemoryView0: This panel shows the memory contents at the current PC address (00001028). The memory is organized into a table with columns for address and data. The data is shown in hexadecimal, with the value 81818181 repeated across multiple locations.

OutputView: This panel shows the output of the program. The console output is currently empty, but it is configured to capture stdout and stderr.

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Week#3

Program Number: 3

Title of the Program

Convert the following statement in C language into an ALP using ARM7TDMI – ISA.

IF([A]==[B]) then C=[A]+[B];

ELSE IF ([B]==[C]) D=[A]-[B];

ELSE E=[A]*[B]

Where A,B C, D & E are memory locations.

I. ARM Assembly Code:



vishwa@Acer-Vishwa: /mnt/c/U



vishwa@Acer-Vishwa: /mnt/c/U

```
1  .data
2  A:  .word 12
3  B:  .word 5
4  C:  .word 5
5  D:  .word 0
6  E:  .word 0
7  .text
8  ldr r0,=A
9  ldr r1,=B
10 ldr r2,=C
11 ldr r3,=D
12 ldr r4,=E
13
14 ldr r5,[r0]
15 ldr r6,[r1]
16 ldr r7,[r2]
17 ldr r7,[r2]
18
19 cmp r5,r6
20 beq l1
21 cmp r6,r7
22 beq l2
23 b 13
24
25 l1: add r8,r5,r6
26     str r8,[r2]
27     b 1
28 l2: sub r9,r5,r6
29     str r9,[r3]
30     b 1
31 l3: mul r10,r5,r6
32     str r10,[r4]
33 l: swi 0x011
```


II. Output Screen Shot:

The image displays two screenshots of the ARMSim# - The ARM Simulator interface, showing the execution of assembly code and the state of registers and memory.

Top Screenshot:

- RegistersView:** Shows the state of registers R0 through R15. R15 (pc) is highlighted at 4180. The CPSR Register shows Negative (N): 0, Zero (Z): 0, Carry (C): 1, Overflow (V): 0, IRQ Disable: 1, FIQ Disable: 1, Thumb (T): 0, and CPU Mode: System.
- CodeView:** Displays assembly code for file p5.o. The code includes instructions like `cmp r5, r6`, `beq l1`, `cmp r6, r7`, `beq l2`, `b l3`, `add r8, r5, r6`, `str r8, [r2]`, `b l1`, `sub r9, r5, r6`, `str r9, [r3]`, `b l1`, `mul r10, r5, r6`, `str r10, [r4]`, and `swi 0x011`.
- MemoryView0:** Shows memory at address 0000106C. The word size is set to 32Bit. The memory contains the value 000000CC.
- OutputView:** Shows the console output: "Loading assembly language file C:\Users\Vishwa\Documents\Vishwa_PES\Sem4\MPCA\MPCA_HandsOn\week3\p5.s".

Bottom Screenshot:

- RegistersView:** Shows the state of registers R0 through R15. R15 (pc) is highlighted at 4156. The CPSR Register shows Negative (N): 0, Zero (Z): 1, Carry (C): 1, Overflow (V): 0, IRQ Disable: 1, FIQ Disable: 1, Thumb (T): 0, and CPU Mode: System.
- CodeView:** Displays assembly code for file p5.o. The code includes instructions like `.data`, `A: .word 12`, `B: .word 12`, `C: .word 5`, `D: .word 0`, `E: .word 0`, `.text`, `ldr r0, =A`, `ldr r1, =B`, `ldr r2, =C`, `ldr r3, =D`, `ldr r4, =E`, `ldr r5, [r0]`, `ldr r6, [r1]`, and `ldr r7, [r2]`.
- MemoryView0:** Shows memory at address 0000106C. The word size is set to 32Bit. The memory contains the value 00000018.
- OutputView:** Shows the console output: "Loading assembly language file C:\Users\Vishwa\Documents\Vishwa_PES\Sem4\MPCA\MPCA_HandsOn\week3\p5.s".



Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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