

# Microprocessor and Computer Architecture

UE20CS252

4th Semester, Academic Year 2021-22

Date: 22/02/2022

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Week# 5

Program Number: 1

Title of the Program

1. Write a program in ARM7TDMI-ISA to add 2 matrices of order 3.  
i.e., Implement  $c[i][j] = a[i][j] + b[i][j]$ .

## 1. ARM Assembly Code(1)

```
vishwa@Acer-Vishwa: /mnt/c/U  ×  +  ∨  
1  .data  
2  c: .word 0  
3  a: .word 10,20,30,40,50,60,70,80,90  
4  b: .word 1,2,3,4,5,6,7,8,9  
5  .text  
6  ldr r0,=a  
7  ldr r1,=b  
8  ldr r2,=c  
9  mov r3,#0 //sum  
10 mov r4,#9 //counter  
11 loop:  
12     ldr r5,[r0],#4  
13     ldr r6,[r1],#4  
14     add r3,r5,r6  
15     str r3,[r2]  
16     add r2,r2,#4  
17     sub r4,r4,#1  
18     cmp r4,#0  
19     bne loop  
20 swi 0x11  
21  
~  
~
```

## 2. Output Screen Shot (1)

The screenshot displays the ARMSim# ARM Simulator interface, which is divided into several panes. The top menu bar includes File, View, Cache, Debug, Watch, and Help. The main window is titled "ARMSim# - The ARM Simulator Dept. of Computer Science".

**RegistersView:** This pane shows the state of the ARM registers. The "General Purpose" tab is selected, displaying registers R0 through R15. R0 is 4204, R1 is 4240, R2 is 4200, R3 is 99, R4 is 0, R5 is 90, R6 is 9, R7 is 0, R8 is 0, R9 is 0, R10 (s1) is 0, R11 (fp) is 0, R12 (ip) is 0, R13 (sp) is 70656, R14 (lr) is 0, and R15 (pc) is 4148. The CPSR register is also shown with fields: Negative (N) is 0, Zero (Z) is 1, Carry (C) is 1, Overflow (V) is 0, IRQ Disable is 1, FIQ Disable is 1, Thumb (T) is 0, and CPU Mode is System. The PC value is 0x60000df.

**CodeView:** This pane shows the assembly code being executed. The code is from a file named "matrices.o". The instructions are: ldr r6, [r1], #4; add r3, r5, r6; str r3, [r2]; add r2, r2, #4; sub r4, r4, #1; cmp r4, #0; bne loop; and swi 0x11. The instruction at address 00001034 is highlighted.

**MemoryView0:** This pane shows the memory contents. The address 00001044 is selected. The memory is displayed in a table with columns for address and data. The data is shown in hexadecimal, with some values highlighted in red. The word size is set to 32Bit.

**OutputView:** This pane shows the output of the program. The "Console" tab is selected, and the output is displayed in a text area. The output is currently empty.

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Week# 4

Program Number: 2

Title of the Program

**2. Write a program in ARM7TDMI-ISA to find the ROWSUM of a matrix.**

## 1. ARM Assembly Code(1)

```
vishwa@Acer-Vishwa: /mnt/c/U  ×  +  ∨  
1  .data  
2  c: .word 0  
3  a: .word 10,20,30,40,50,60,70,80,90  
4  .text  
5  ldr r0,=a  
6  ldr r2,=c  
7  mov r1,#3  
8  loop:  
9      mov r3,#0 //sum  
10     mov r4,#3 //counter  
11     inner:  
12         ldr r5,[r0],#4  
13         add r3,r3,r5  
14         sub r4,r4,#1  
15         cmp r4,#0  
16         bne inner  
17     str r3,[r2],#4  
18     sub r1,r1,#1  
19     cmp r1,#0  
20     bne loop  
21     swi 0x11  
22  
~  
~
```

## 2. Output Screen Shot (1)

The screenshot displays the ARMSim# ARM Simulator interface. The main window is divided into several panes:

- RegistersView:** Shows the current state of ARM registers. R0 is 4204, R1 is 0, R2 is 4176, R3 is 240, R4 is 0, R5 is 90, R6 is 0, R7 is 0, R8 is 0, R9 is 0, R10 (s1) is 0, R11 (fp) is 0, R12 (ip) is 0, R13 (sp) is 70656, R14 (lr) is 0, and R15 (pc) is 4152. The CPSR Register shows Negative (N) as 0, Zero (Z) as 1, Carry (C) as 1, and Overflow (V) as 0. IRQ and FIQ are disabled, Thumb is 0, and CPU Mode is System.
- CodeView:** Displays the assembly code for the program. It includes data definitions for 'c' (word 0) and 'a' (word 10, 20, 30, 40, 50, 60, 70, 80, 90), and text instructions: 'ldr r0,=a', 'ldr r2,=c', and 'mov r1,#3'.
- MemoryView0:** Shows a memory dump starting at address 00001044. The dump consists of multiple rows of hexadecimal values, with the first row containing several non-zero values and subsequent rows containing mostly 81818181.
- OutputView:** Contains a console output area with the text 'stdn/stdout/stderr'.

**Disclaimer:**

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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