

**Indian Institute of Technology, Delhi**  
**ELL 832 Report**  
**Design amplifiers for Tow-Thomas Biquad**

May 4, 2025

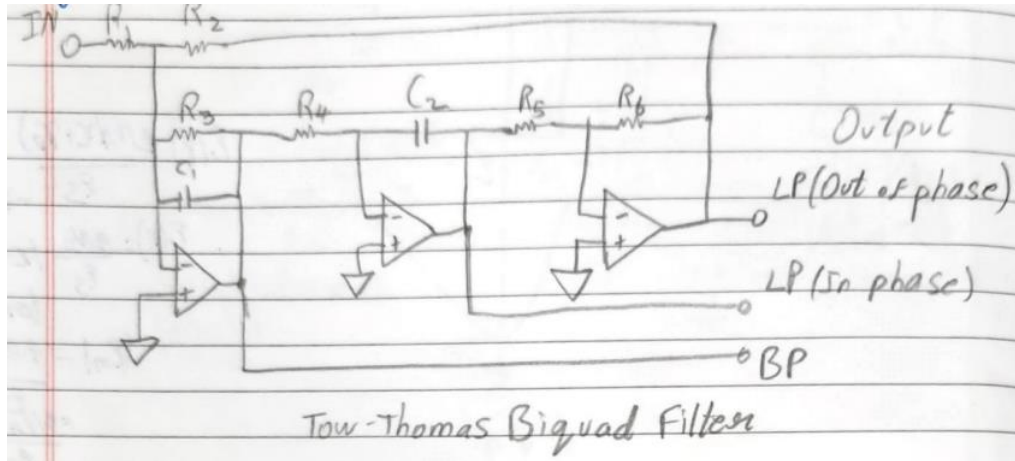
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## Contents

<b>1. Biquad Specifications and Design</b>	<b>2</b>
1.1 Schematics with Ideal Opamp and Results	4
<b>2. Fully Differential Operational Amplifier Design</b>	<b>6</b>
2.1 DC operating point	7
2.1.1 First stage	7
2.1.2 Second Stage	7
2.2 Stability Analysis of Fully Differential Opamp	8
<b>3. Analysis of Biquad Using Designed Fully Differential Opamp</b>	<b>10</b>
3.1 AC analysis	10
3.2 Transient Analysis	11
3.3 Noise Analysis	12
3.4 IM3 Linearity Analysis	13
<b>4. Corner Analyss of Biquad and Fully Differential Amplifier</b>	<b>14</b>
4.1 Stability Corner Analysis of Designed Fully Differential Opamp	15
4.2 AC corner analysis of Biquad	18
4.3 Linearity Corner Analysis	20
4.4 Noise Corner Analysis	21
4.5 Transient Corner Analysis	22
<b>5. References</b>	<b>23</b>

## 1. Biquad Specifications and Design



The above figure represents the biquad for single ended amplifier. The specifications are as given below.

<b>Power Supply</b>	1.8 V	<b>Linearity (IM3)</b>	80dB
<b>Technology</b>	TSMC 65 nm	<b>Phase Margin</b>	>55 degree
<b>Signal Swing</b>	200 mV to 1.6 V	<b>Gain Margin</b>	>10 dB
<b>Signal Bandwidth</b>	500 MHz	<b>Corners</b>	SS, FF, TT, SF, FS
<b>IRN</b>	100 uVrms	<b>Temperature</b>	-40 to 125

The name derives from the fact that the transfer function is a quadratic in both the numerator and denominator. Hence the transfer function is a biquadratic function. The parameters can be calculated as:

$k = 2\pi f_0 C$  Choose  $C, R_2, R_5$   
 $C_1 = C_2 = C$   
 $R_3 = \frac{1}{k\omega}$   $R_4 = \frac{1}{k^2 R_2}$   
 $R_1 = \frac{R_2}{H}$   $R_5 = R_6$

where  $H =$  voltage gain at resonance  
 $f_0 =$  central frequency  
 $Q =$  quality factor  
 $\alpha =$  damping ratio  $= 1/2$

Frequency would generally be adjusted ( $R_4$ ) first followed by Q ( $R_3$ ) and then gain ( $R_1$ ).

For low pass filter

$$G(s) = \frac{V_o}{V_i} = \frac{1}{s^2 + s \frac{R_1 R_2 C_1 C_2}{R_3 + R_4} + \frac{1}{R_3 R_4 C_1 C_2}}$$

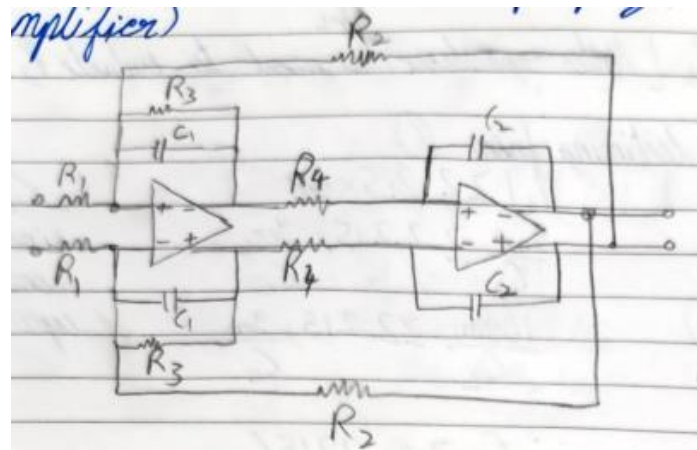
$$H = \frac{R_2}{R_1}$$

For band pass filter

$$V(s) = \frac{V_o}{V_i} = \frac{s \left( -\frac{1}{R_1 C_1} \right)}{s^2 + s \left( \frac{1}{R_4 C_1} \right) + \frac{1}{C_1 C_2 R_2 R_4}}$$

where  $|H| = \left| \frac{-R_3}{R_1} \right|$

The circuit can be redrawn to fully differential amplifier:



The equation can be rewritten as:

$$A_v = \frac{R_2}{R_1}, \quad \omega_0 = \frac{1}{\sqrt{R_4 R_2 C_1 C_2}}, \quad \phi = \frac{R_3 \sqrt{C_1}}{\sqrt{R_4 R_2 C_2}}$$

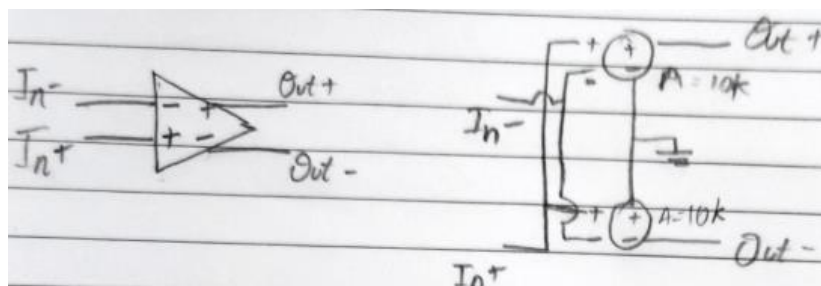
To meet the specifications such as **noise**, **gain (1)**, **frequency** as well as the **quality factor** we choose

$$R_1 = R_2 = R_4 = 300 \text{ Ohm}$$

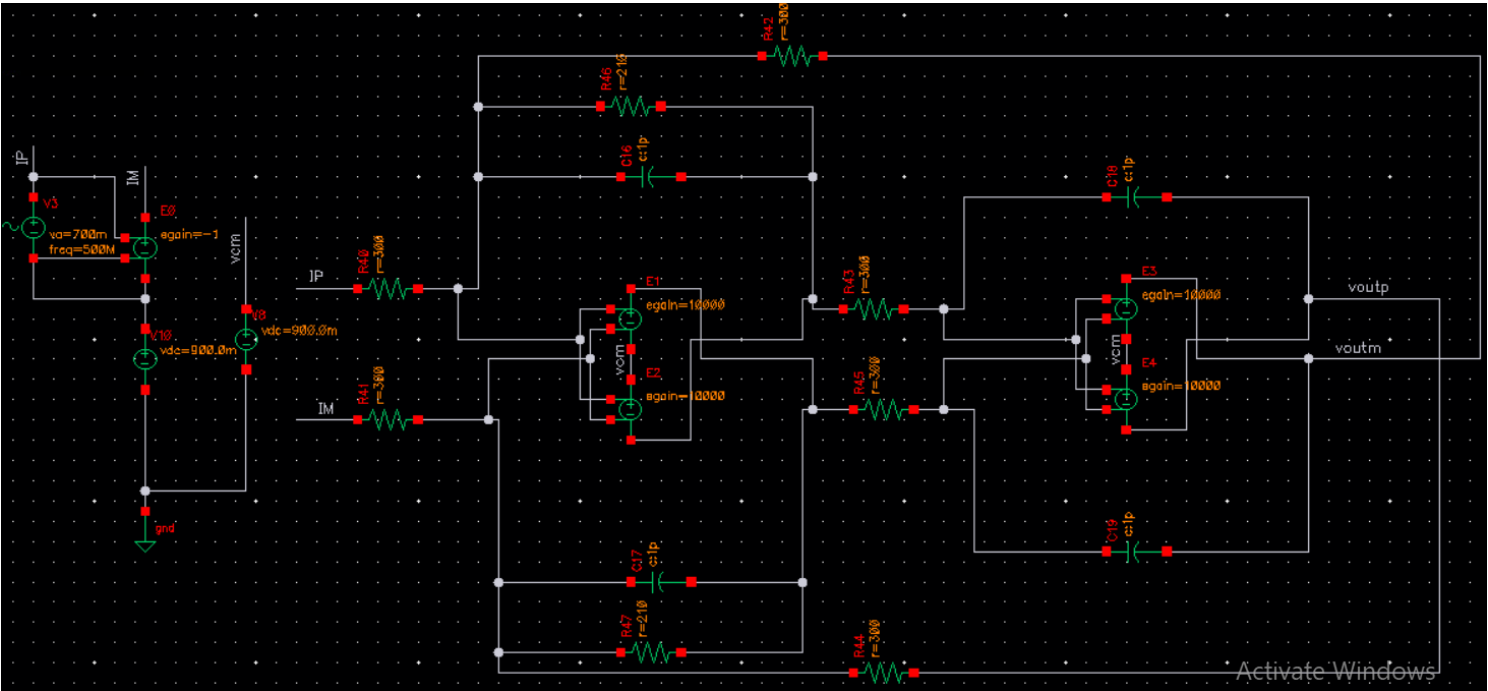
$$R_3 = 210 \text{ Ohm (for } Q = 0.707) \text{ and } R_3 = 300 \text{ Ohm (for } Q = 1)$$

$$C_1 = C_2 = 1 \text{ pF (for 500MHz Bandwidth)}$$

**An ideal fully differential amplifier** can be simulated from VCVS with the configuration below.



# 1.1 Schematics with Ideal Opamp and Results



Device	Param	Noise Contribution	% Of Total
/R43	rn	7.06413e-05	20.03
/R45	rn	7.06413e-05	20.03
/R46	rn	5.57684e-05	12.49
/R47	rn	5.57684e-05	12.49
/R42	rn	4.66592e-05	8.74
/R40	rn	4.66592e-05	8.74
/R44	rn	4.66592e-05	8.74
/R41	rn	4.66592e-05	8.74

Integrated Noise Summary (in V) Sorted By Noise Contributors  
Total Summarized Noise = 0.000157826  
Total Input Referred Noise = 8.4721e-05  
The above noise summary info is for noise data

Fig 1: Noise Summary. The INR is less than 100  $\mu\text{V}_{\text{RMS}}$ .

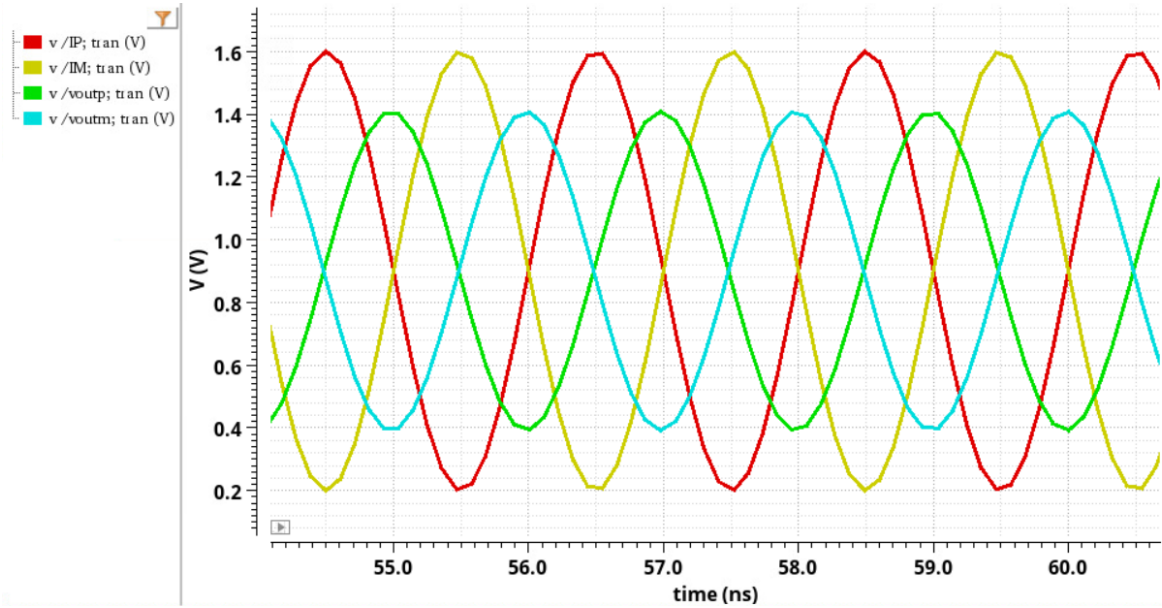


Fig 2: Transient Analysis Result ( $Q=0.707$ ,  $R_3=210\text{ Ohm}$ )



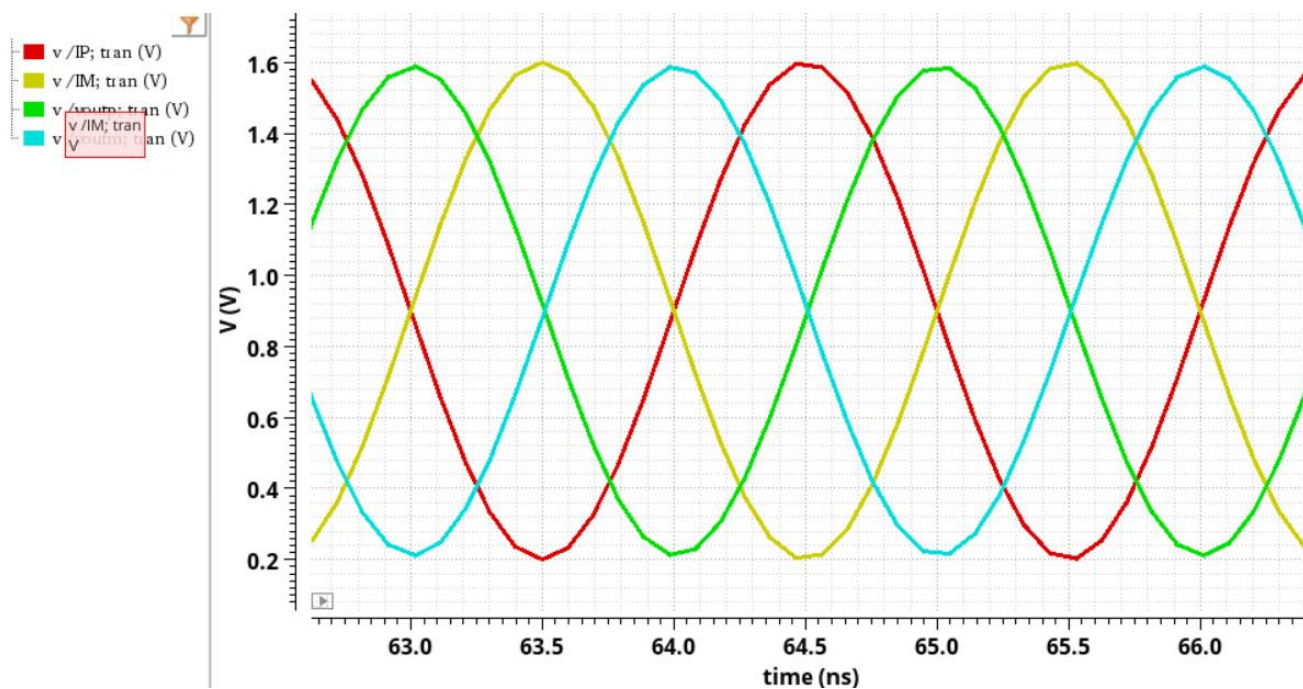


Fig 3: Transient Analysis Result ( $Q=1$ ,  $R_3=300$ )

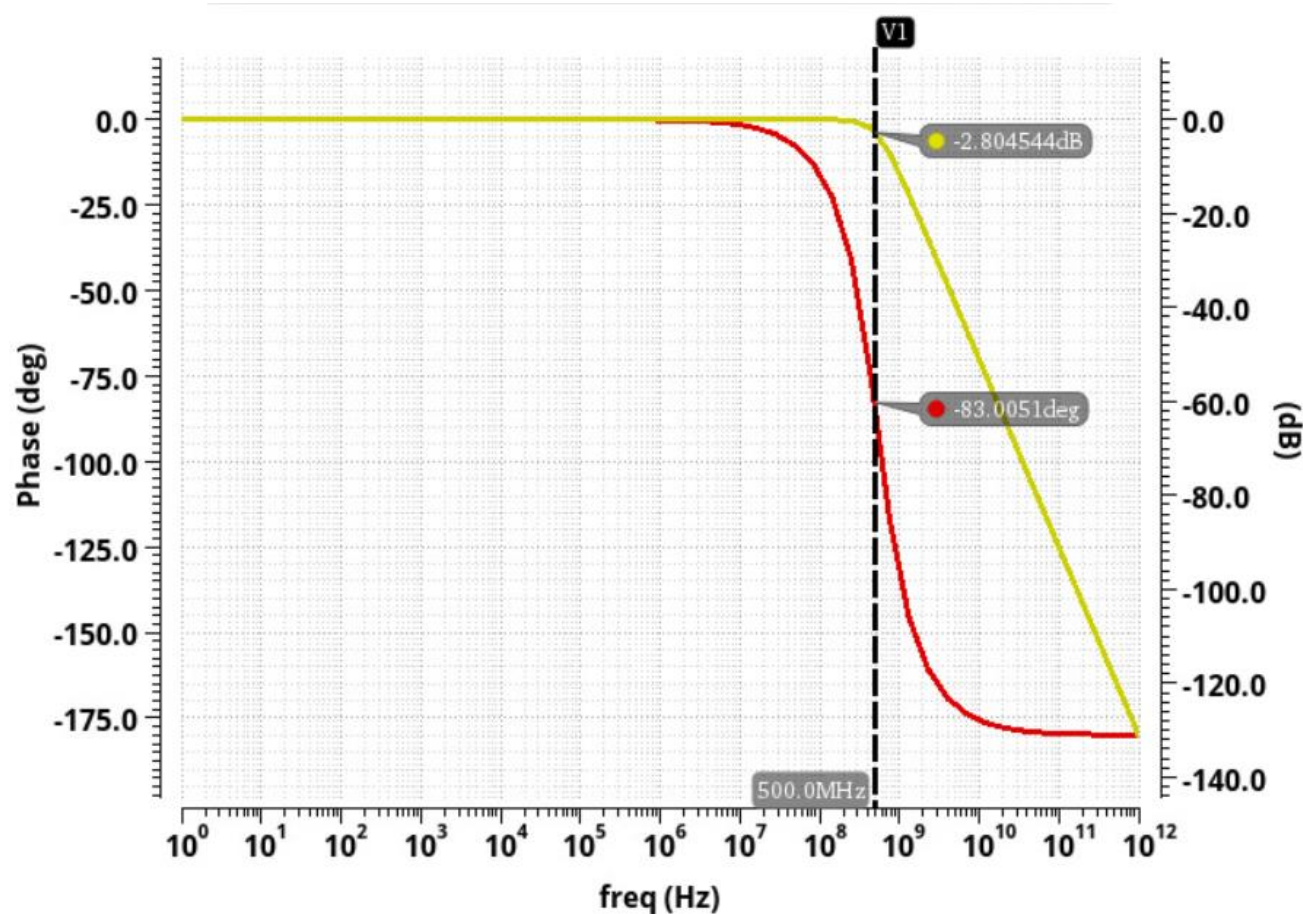


Fig 4: AC Response at  $Q = 0.707$

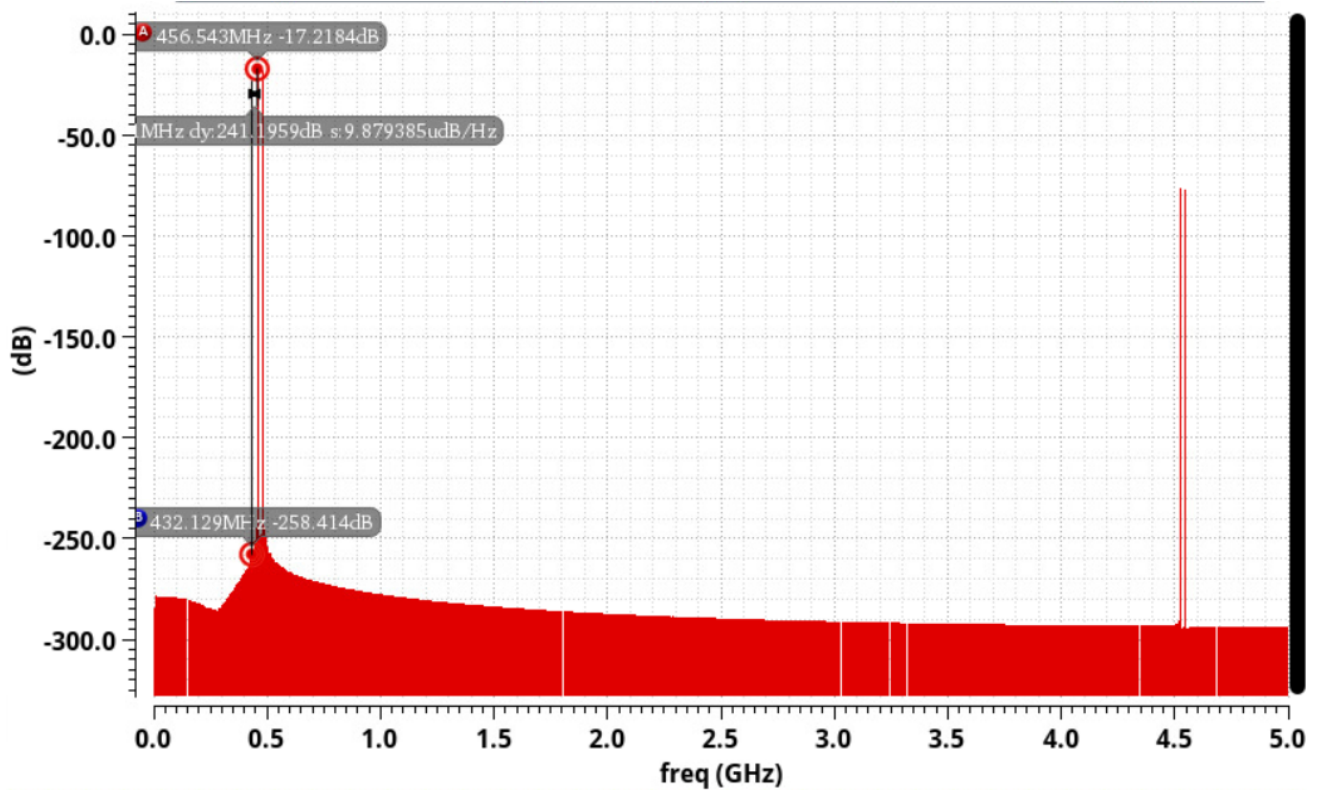


Fig 5: Linearity

## 2. Fully Differential Operational Amplifier Design

Since our biquad is designed for a bandwidth of 500MHz. We want the UGB of Opamp to be 10 times of bandwidth i.e. 5GHz. Below shows the Opamp schematic I have taken a simple 5T OTA with class AB second stage and compensated by miller capacitance.

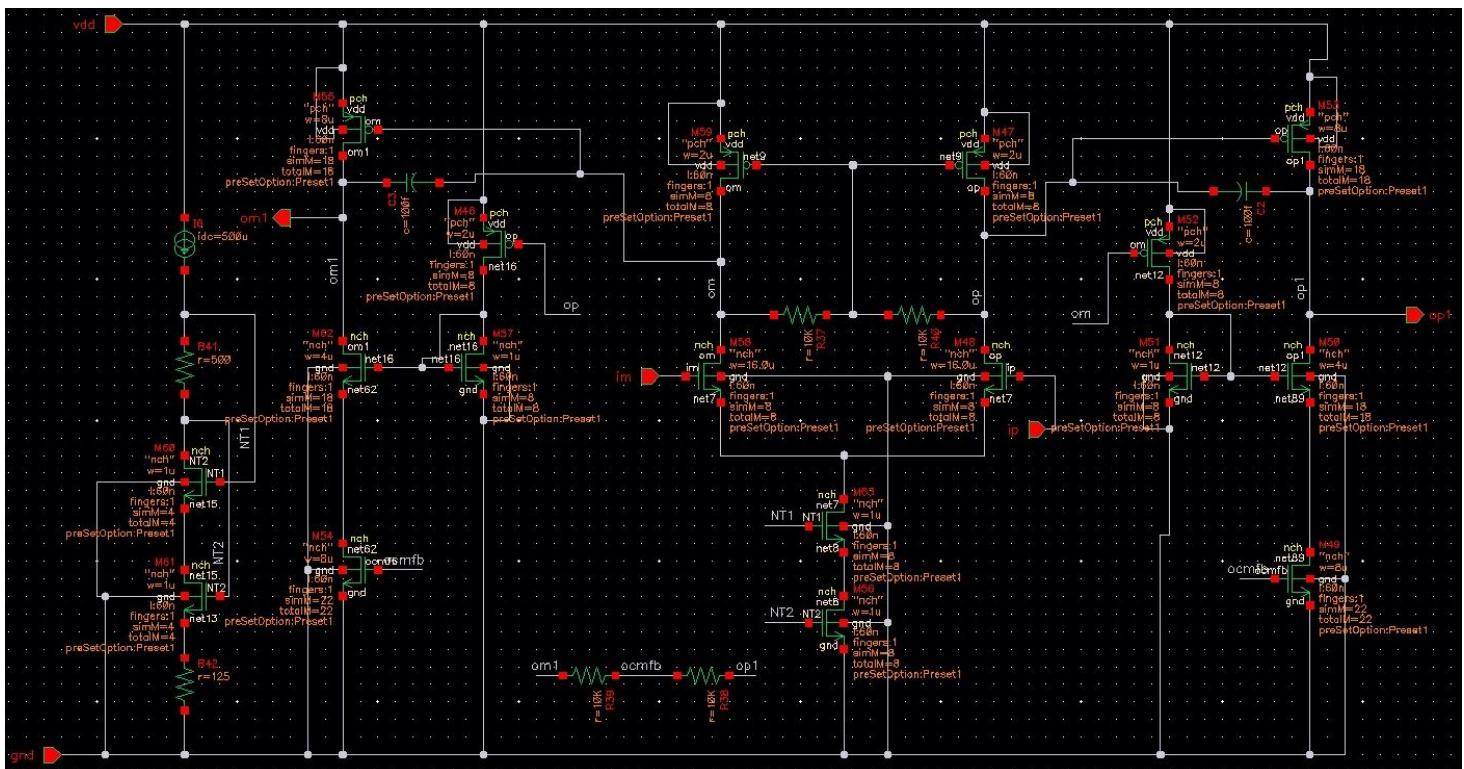


Fig 6: Opamp schematic



## 2.1 DC operating point.

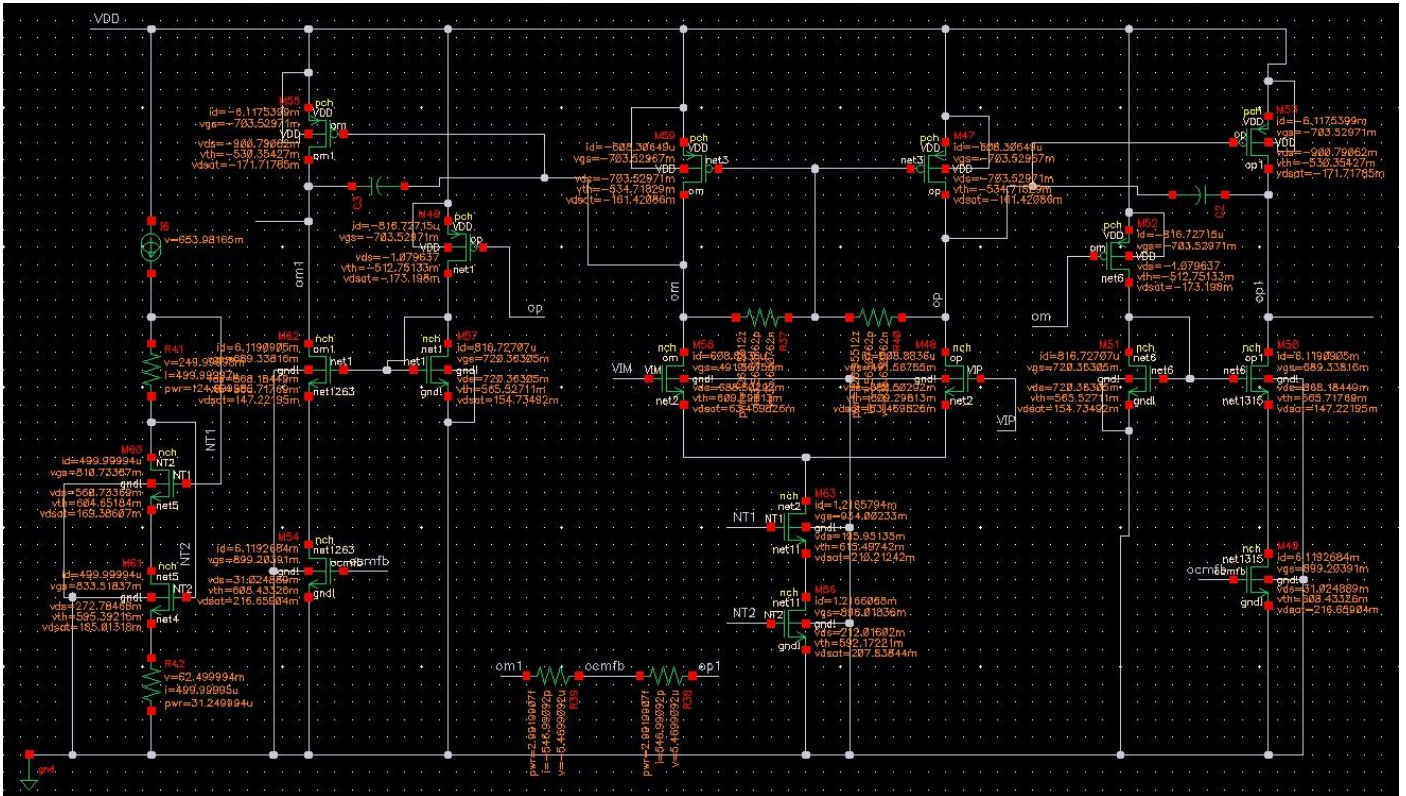


Fig 7 Schematic of DC operating point

### 2.1.1 First stage

We have a biasing branch at left side of Fig 7 with 500uA current source to bias the NMOS tail current of first stage as 1.2mA.

Then the differential pair receives a current of 600uA. The PMOS tail at top of the differential input pair doesn't requires a separate biasing stage since it utilizes the resistive common mode feedback (we are not considering any MOSFET mismatch – so no need of Opamp for common mode feedback).

$V_{DS}$  is greater than  $V_{DSAT}$  thus the MOSFETs are in saturation. The transconductance  $g_{m1}$  of input differential pair came up to be 10mS. For the Miller compensation scheme, we want the second stage to be far from the first stage  $g_m$ . Since the first stage determines the dominant pole and second stage determines the non-dominant pole. Since we don't have capacitive load in the biquad except the feedback path, we don't need to worry about the second pole coming too close.

### 2.1.2 Second Stage

The second stage has utilized **Class AB stage**. Consider what happens if the noninverting op-amp input, VIP, increases relative to the inverting input, VIM. The drain voltage of M48 drops while the drain voltage of M58 rises. The decrease in the gate voltage of M53 causes it to turn on and the output to go high. At the same time, the increase in the drain voltage of M58 causes M52 to shut off and thus so does M50 (giving class AB operation). In simple terms, we can yank the gates of M52 or M53 or M46 or M55 down independent of the diff-amp's tail current.

We bias the second stage with Multiplier M value in such as way it would have at least 6mA current. Here we have use  $Q=0.707$  values but in case of  $Q=1$  value with ideal simulation in Opamp we were able

to see that the current swing is -5.4mA to +5.4mA. Thus, we keep it to be at least 6mA as well as to have high transconductance value ( $g_{m2} = 42\text{mS}$ ), so the miller compensation works as desired.

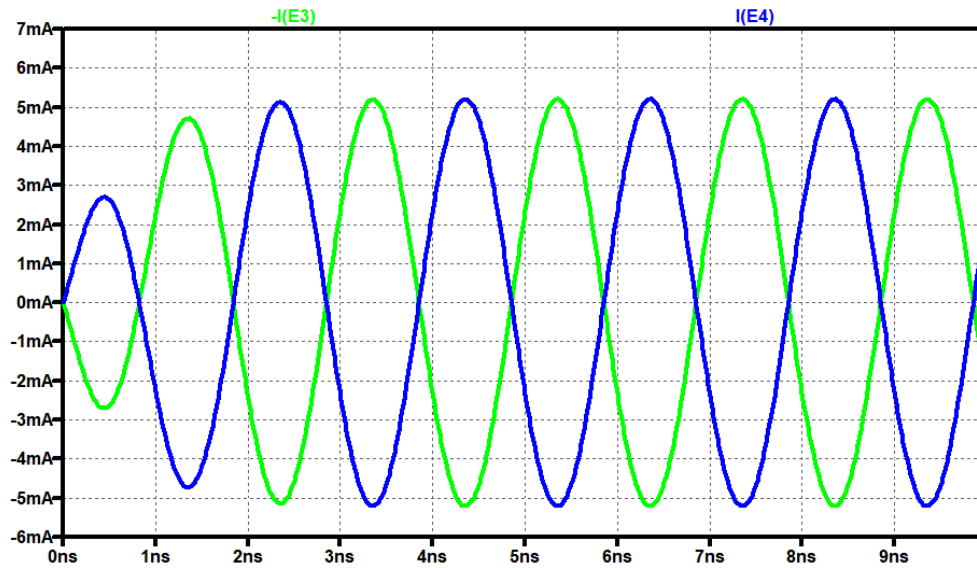


Fig 8 Current output of Ideal Opamp Ltspice (for Q=1)

## 2.2 Stability Analysis of Fully Differential Opamp

The miller capacitance is chosen to be 100fF. Usually, we would want single pole system while using miller capacitance pushing non dominant pole away from UGB ( $\frac{g_{m1}}{2\pi c_c}$ ). But pushing the non-dominant pole further away than UGB means increase in  $g_{m2}$  further either by increasing current (we are limiting to 6mA) or increasing W/L (Takes more space). It is not necessary to be further away if the UGB is more than **5GHz** (10 times more than the bandwidth of biquad – 500MHz).

Below shows the test bench for STB analysis. We use diffstb probe in front of the input of Opamp breaking the feedback.

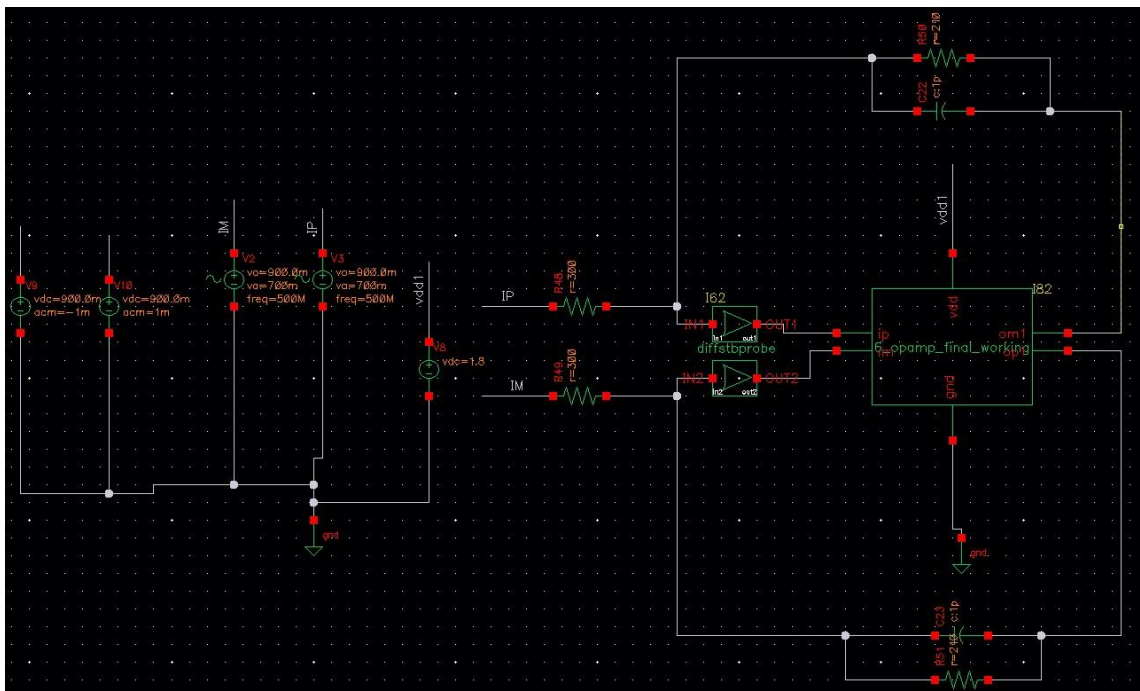


Fig 9 Test bench for stability analysis of Operational Amplifier



We apply stb analysis in ADE L analysis with frequency from 1Hz to 1THz. The results are as shown below.

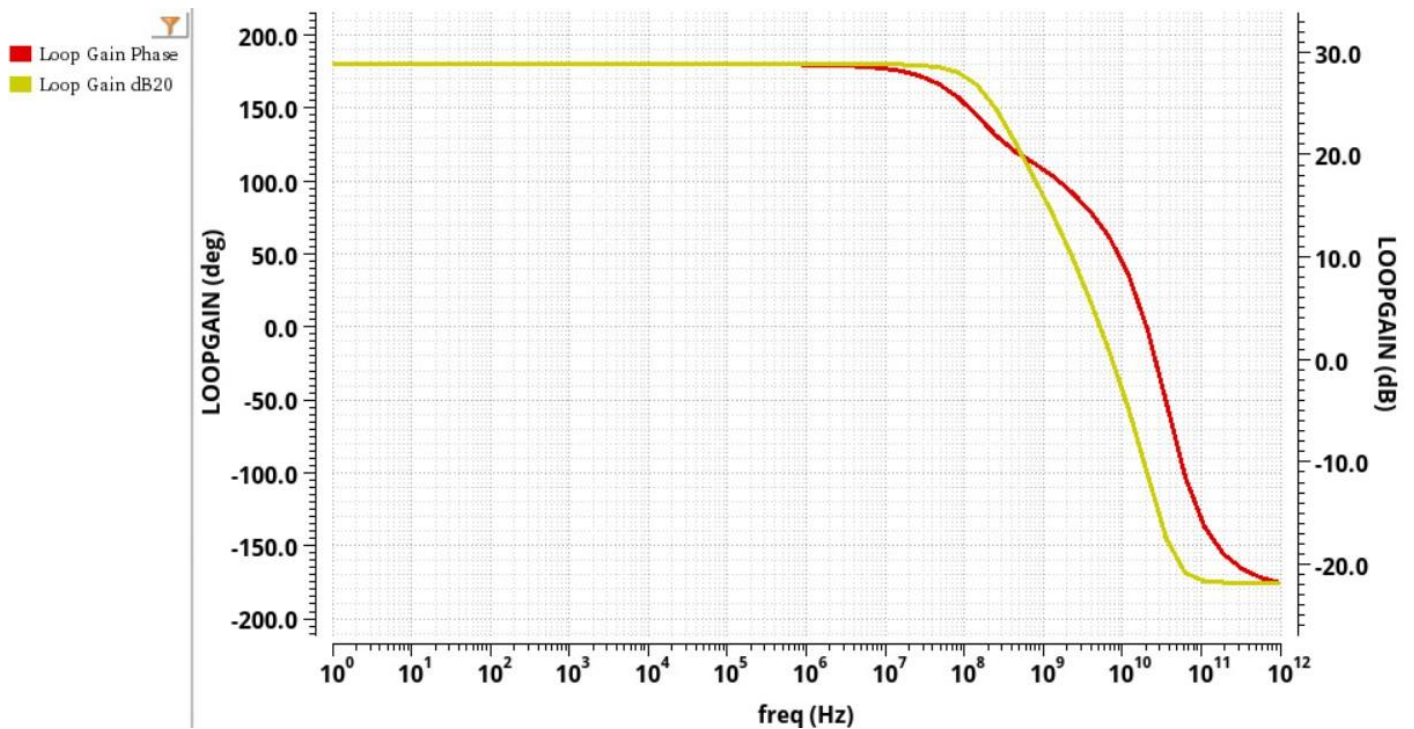


Fig 10 Bode plot of designed fully differential operational amplifier.



Fig 11 Stability Analysis summary

Here we have met the specifications that we mentioned earlier for gain margin ( $>10\text{dB}$ ), phase margin ( $>55^\circ$ ) and UGB ( $\geq 5\text{GHz}$ ). We also need to be careful of RHP zero created due to feedforward in miller. In the current design the RHP zero is away UGB (It is good).

### 3. Analysis of Biquad Using Designed Fully Differential Opamp

We have met the specifications of Opamp. Now let us simulate for the other specifications like AC analysis, transient analysis, noise, and linearity.

#### 3.1 AC analysis

Below shows the test bench for AC analysis of Biquad.

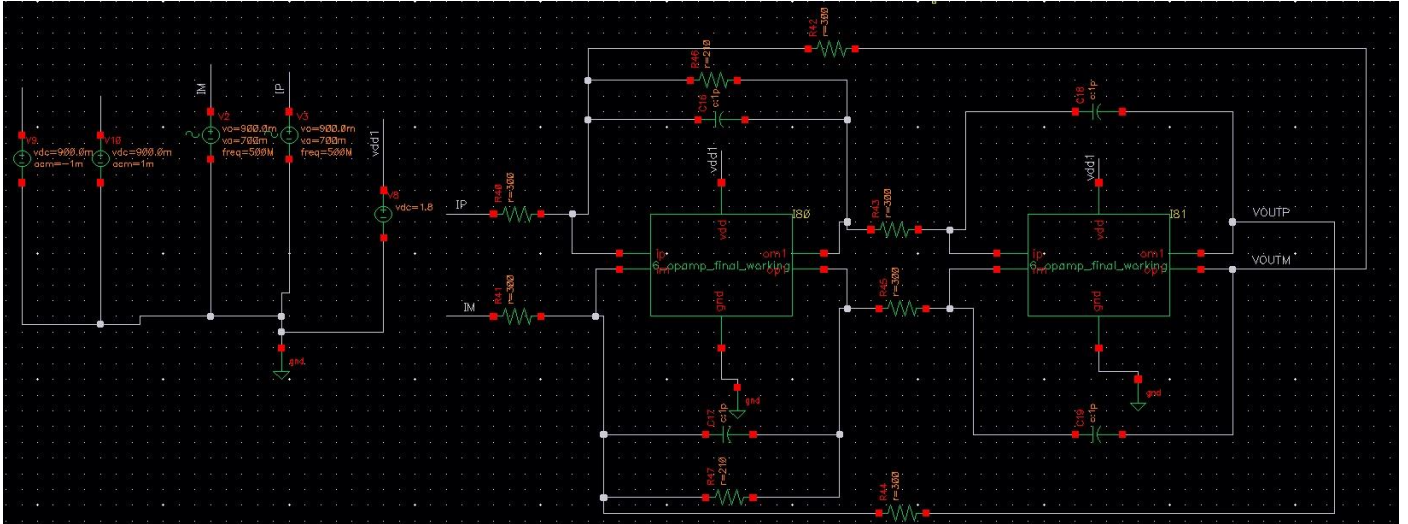


Fig 12 Test bench for AC and Transient analysis. For AC analysis switch IP and IM to V10 and V9

The AC analysis is setup in ADE L to run in the frequency range of 1Hz to 1THz. Since we are using  $Q = 0.707$  the feedback of first amplifier will have resistance of  $Q \times 300 \text{ ohm} = 210 \text{ Ohm}$ . Thus, the closed loop AC analysis should have **500MHz close to -3dB**. If  $Q=1$  then 500MHz would be close to 0dB.

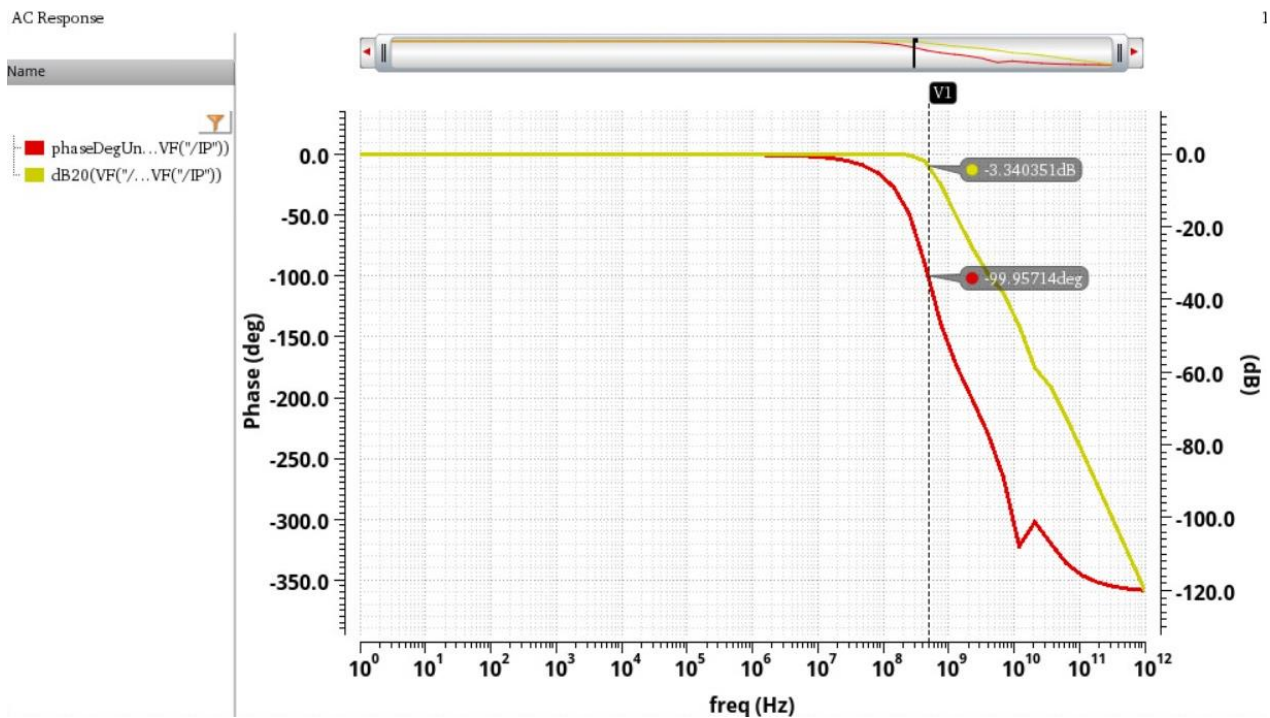


Fig 13 Closed AC response of Biquad Circuit

As expected, we are able to get 500MHz at **-3.3dB** i.e close to -3dB.

## 3.2 Transient Analysis

The same schematic is followed as shown in Fig 12. We run Transient Analysis for 100 ns in ADE L spectre. Below shows the output waveform.

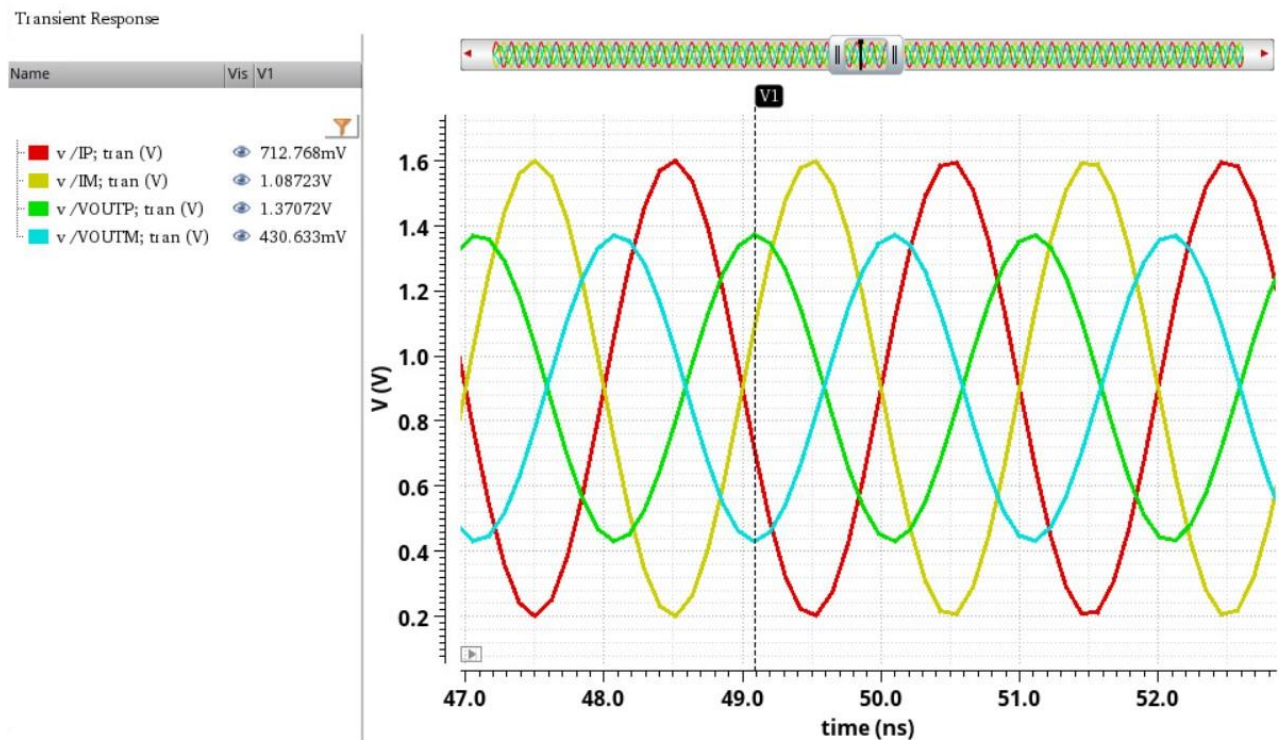


Fig 14 Transient Analysis input and output waveform (**500 MHz**). For **Q=0.707** we miss the swing only by **30mV**.

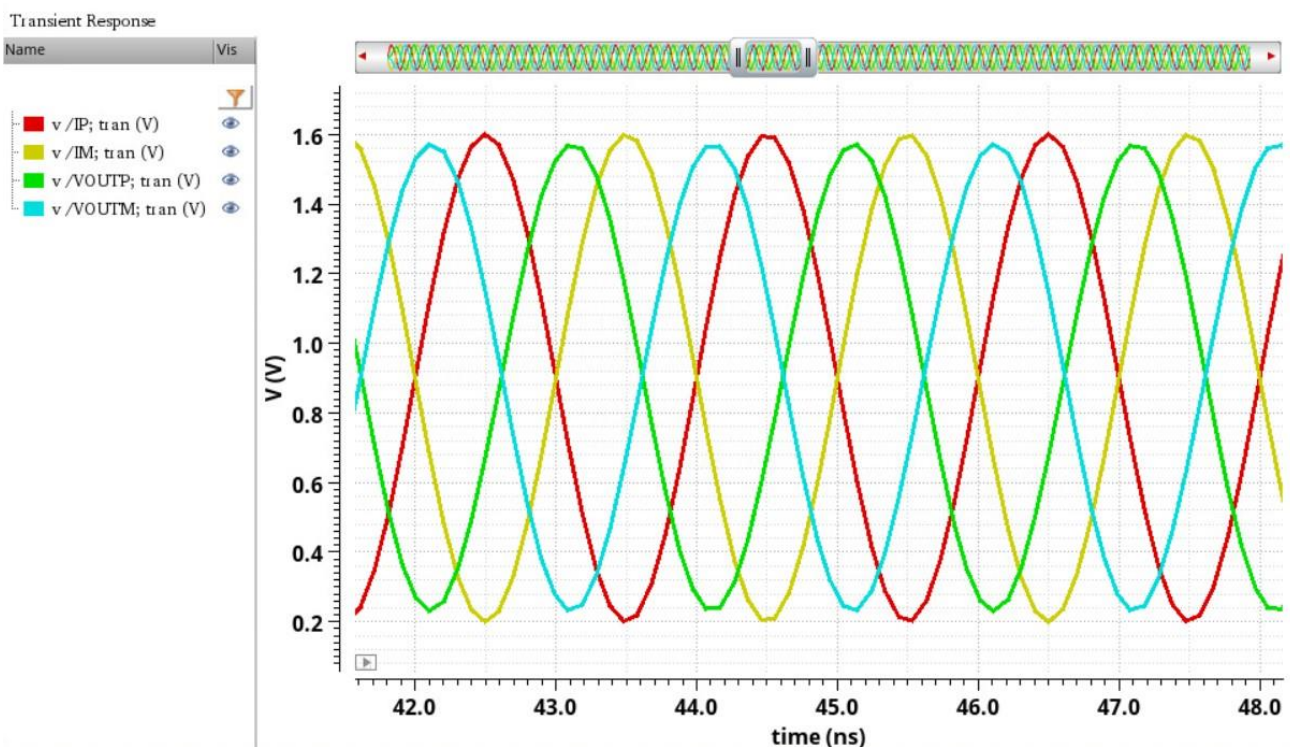


Fig 14 Transient Analysis input and output waveform (**500 MHz**). For **Q=1** we miss the swing only by **30mV**.



### 3.3 Noise Analysis

In the specifications at page 2 it is mentioned to be 100  $\mu\text{Vrms}$ . So, any range closer to that is acceptable. In ideal fully differential opamp configuration we got 83  $\mu\text{Vrms}$ . We run noise simulation from **1Hz to 500MHz**, selecting input source to be **V3** and output nodes to be **voutp** and **voutm**. Below shows the test bench and the results of noise simulation.

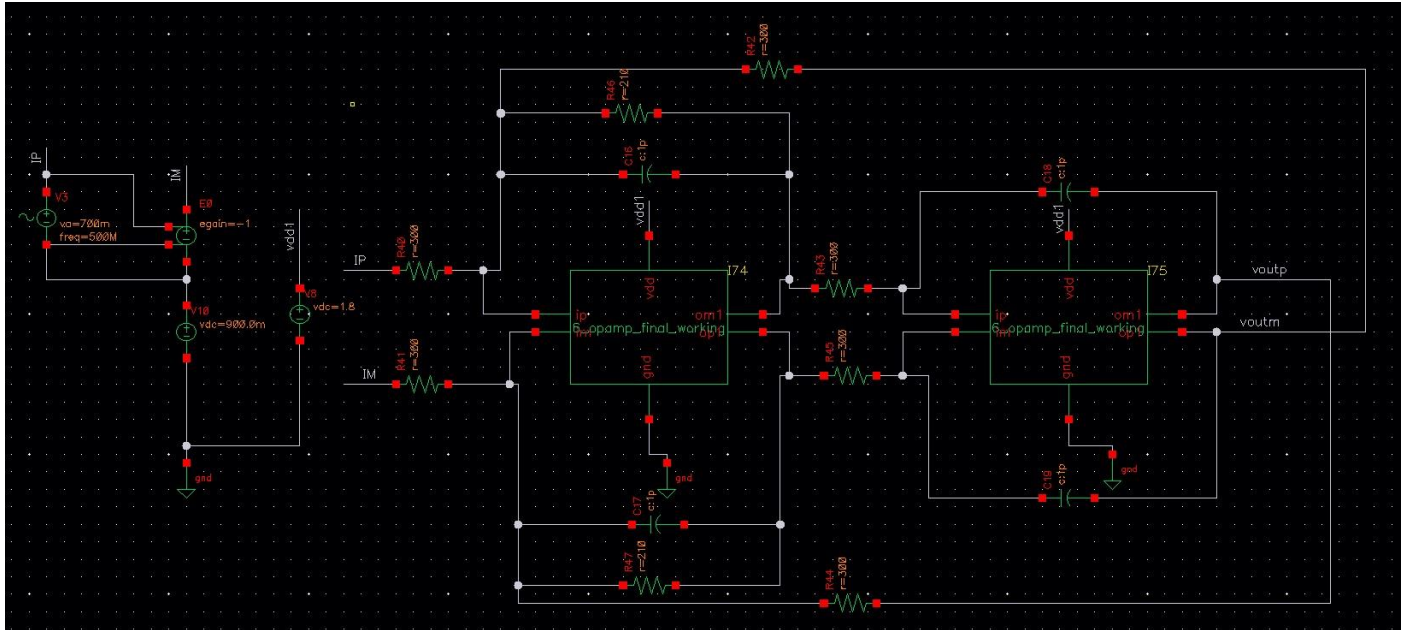


Fig 15 Test bench for Noise Analysis

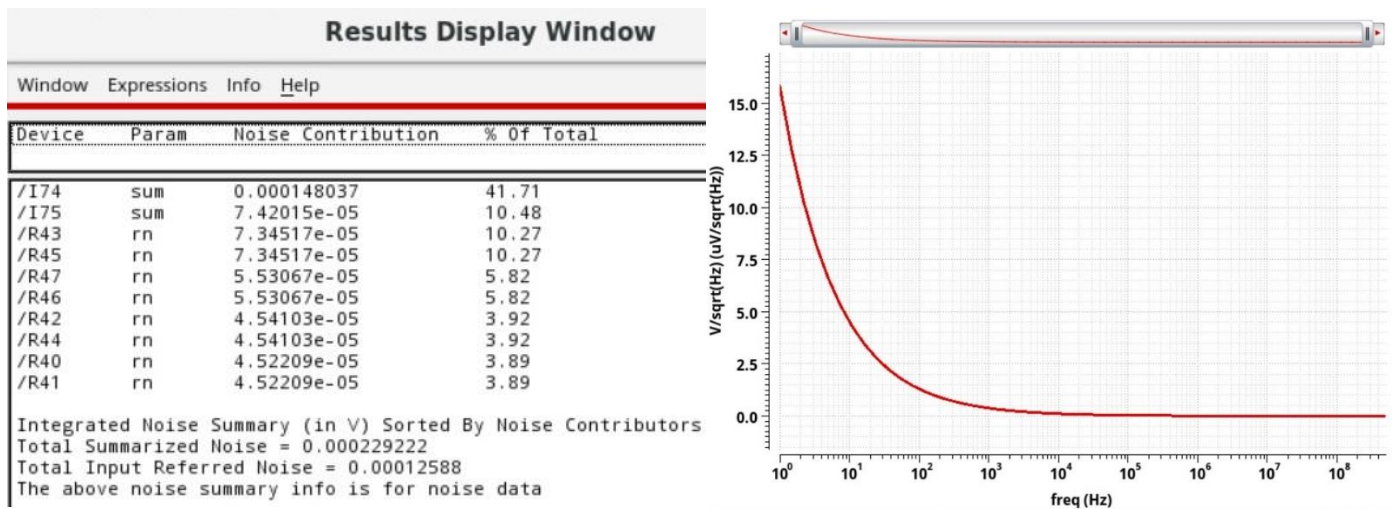


Fig 16 Noise Summary of the simulation and plot of input noise varying with frequency.

From above summary we can see that the Input referred noise is **125  $\mu\text{Vrms}$**  which is closer to the expected value of 100  $\mu\text{Vrms}$ . The plot is also smoother without any peaks in between. The noise is not high thanks to the higher  $g_{m1}$  value (10mS), number of MOSFETS being low and with good W/L ratio.

The INR value can also print using the expression: `sqrt(integ((getData("in" ?result "noise"))**2) 1 500000000))`.



### 3.4 IM3 Linearity Analysis

We run transient analysis setup for 2us and select the transient difference under results section. Then we select two voltage nodes VOUTP and VOUTM.

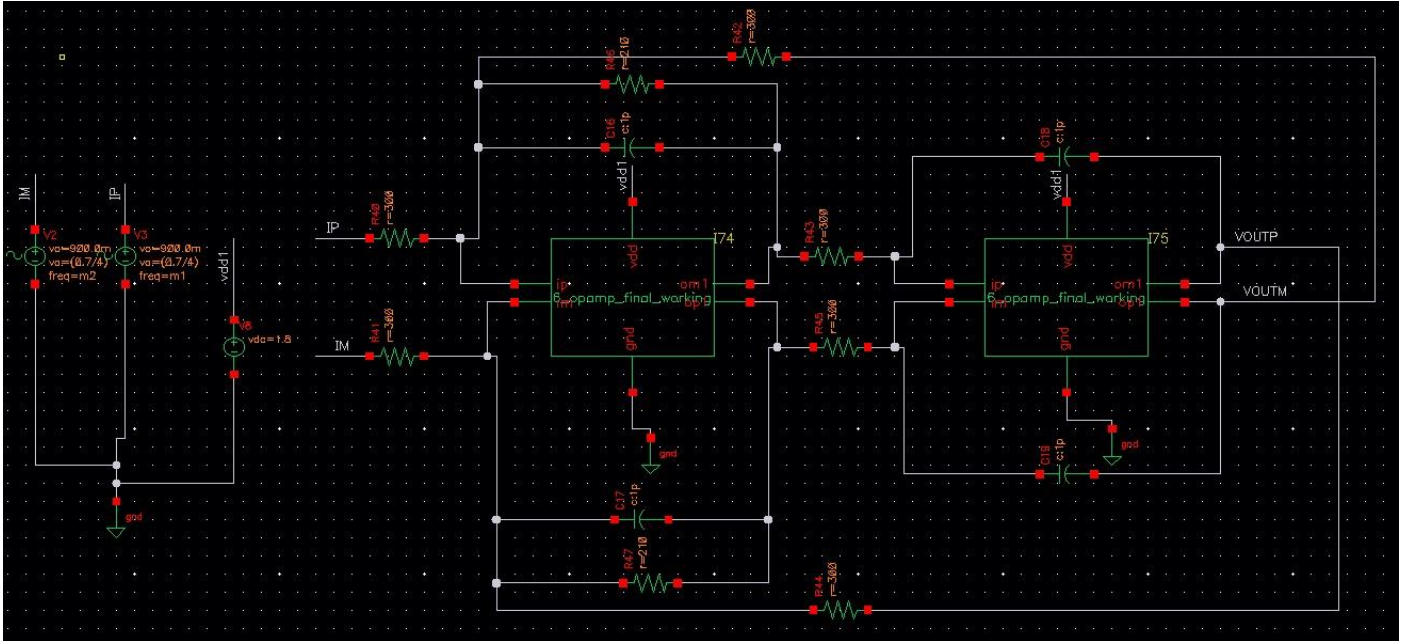


Fig 17 Testbench for linearity.  $m1 = 10e9 \cdot 197/4096$ ,  $m2 = 10e9 \cdot 187/4096$ .

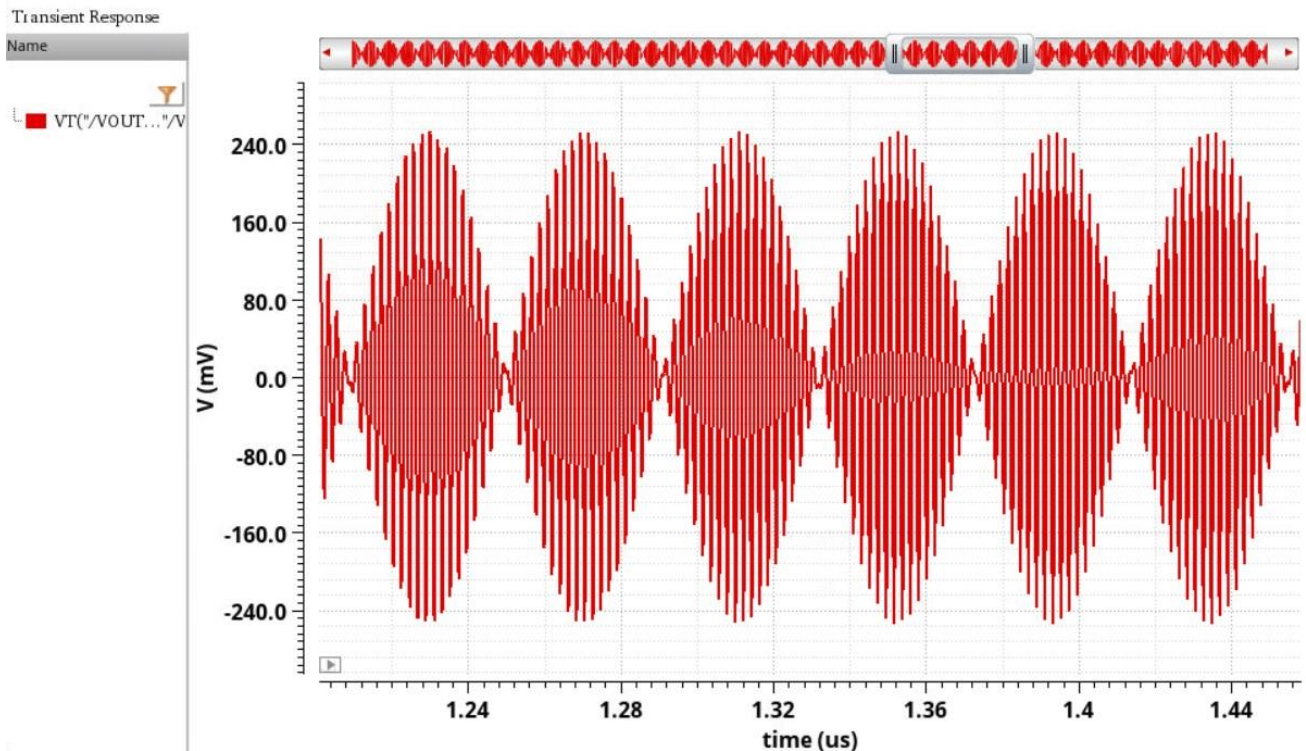


Fig 18 Transient Difference between VOUTP and VOUTM.

Then we use below equations to get linearity plot and the linearity value.

**$\text{dB20}(\text{dft}((\text{vtime}(\text{"tran "/VOUTP"}) - \text{vtime}(\text{"tran "/VOUTM"})) \cdot 100/10e9 \cdot 4196/10e9 \cdot 4096 \cdot \text{"Rectangular"} \cdot 1 \cdot \text{"default"} \cdot 1.0)) \rightarrow \text{save this as linearity in output section.}$**

**$(\text{value}(\text{linearity } 4.56543e+08) - \text{value}(\text{linearity } 4.321289e+08))$**

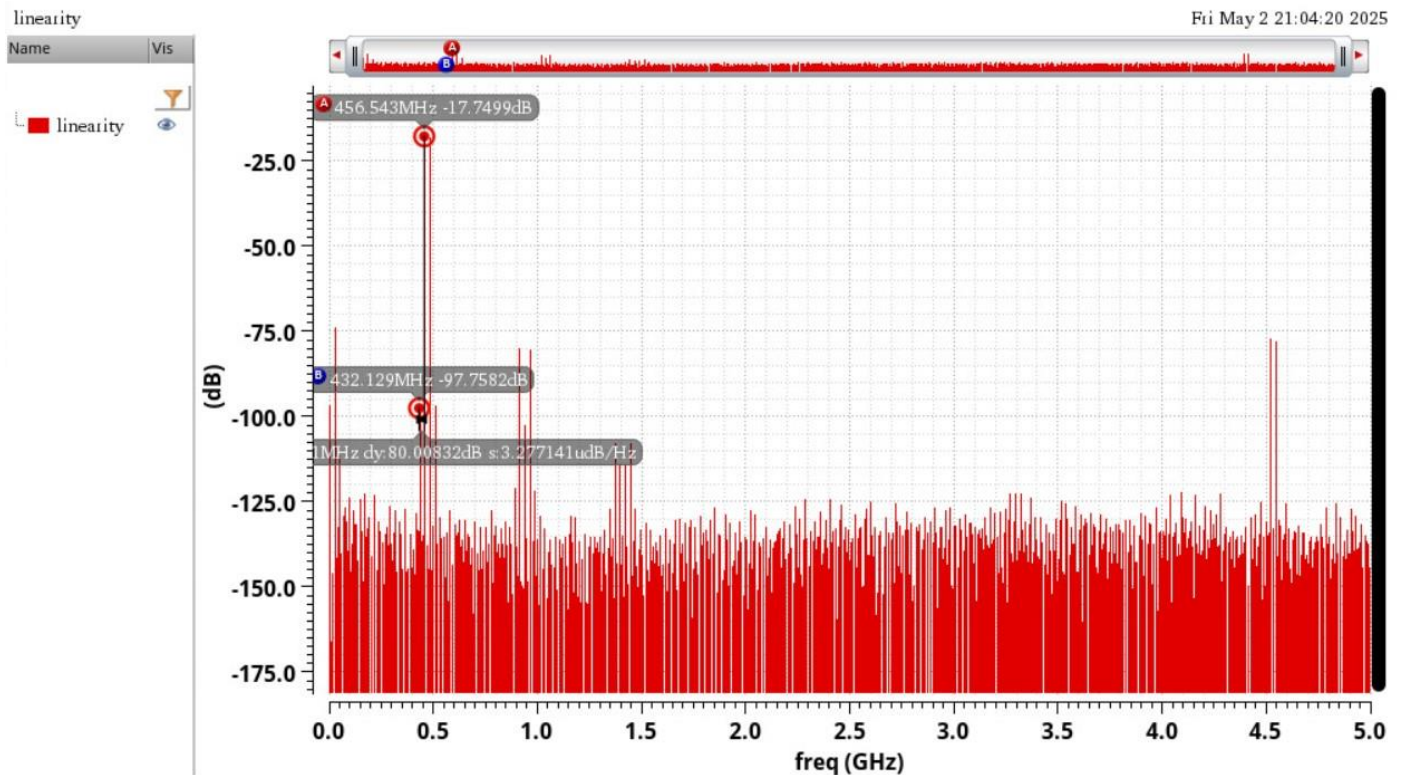


Fig 19 The IM3 Linearity Plot

The above plot also marks the difference **dy** between **456MHz** and **432MHz** giving us the linearity value. We get **80dB** which is the desired value as mentioned in page 2.

## 4. Corner Analyss of Biquad and Fully Differential Amplifier

We run corner analysis using ADE XL across process and temperature as given in below configuration. The corner analysis helps to understand how reliable our device is across different process and temperature.

Parameter	temperature	toplevel.scs
C0_0	-40	ss_lib
C0_1	27	ss_lib
C0_2	125	ss_lib
C0_3	-40	ff_lib
C0_4	27	ff_lib
C0_5	125	ff_lib
C0_6	-40	sf_lib
C0_7	27	sf_lib
C0_8	125	sf_lib
C0_9	-40	fs_lib
C0_10	27	fs_lib
C0_11	125	fs_lib
C0_12	-40	tt_lib
C0_13	27	tt_lib
C0_14	125	tt_lib

While running the corner analysis we load the saved session from ADE L in ADE XL.

## 4.1 Stability Corner Analysis of Designed Fully Differential Opamp

Below are the results of corner analysis in loop gain plot, loop phase plot, gain margin, phase margin and UGB.

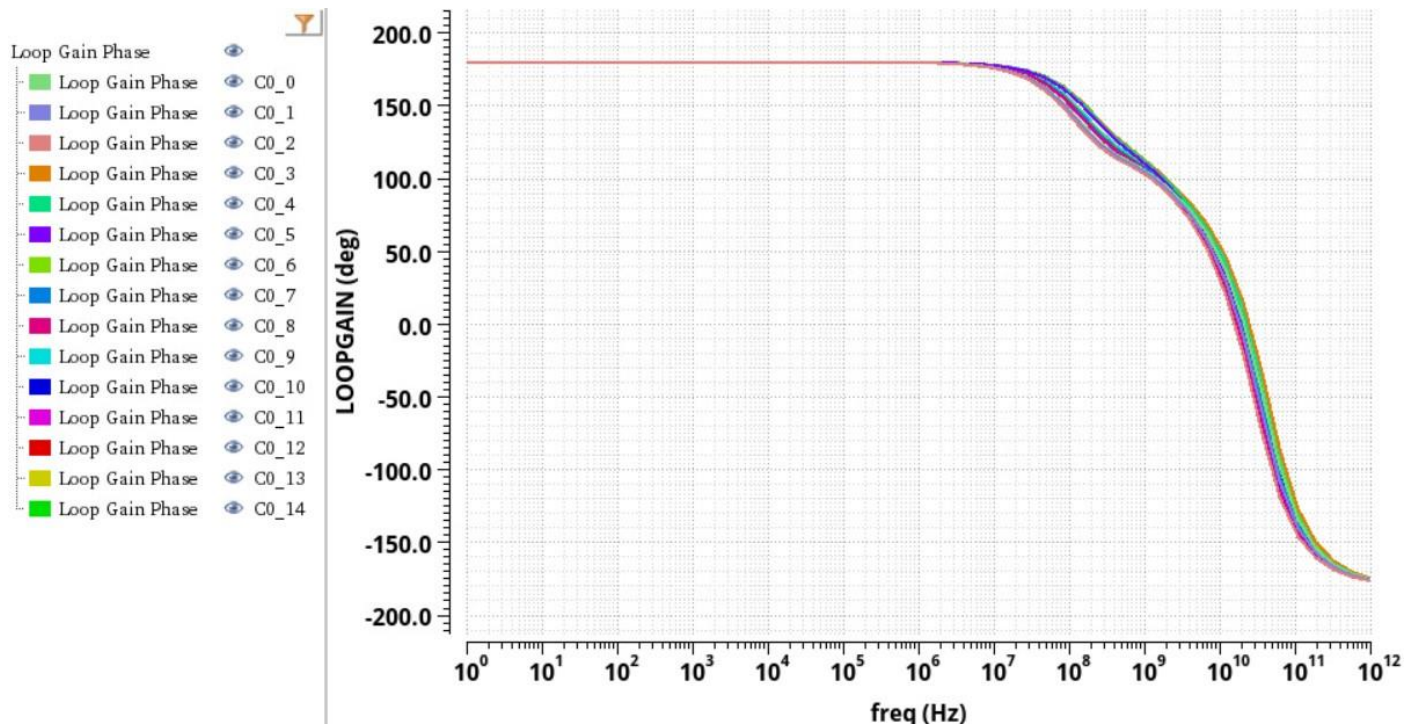


Fig 20 Variation of loop gain around corners.

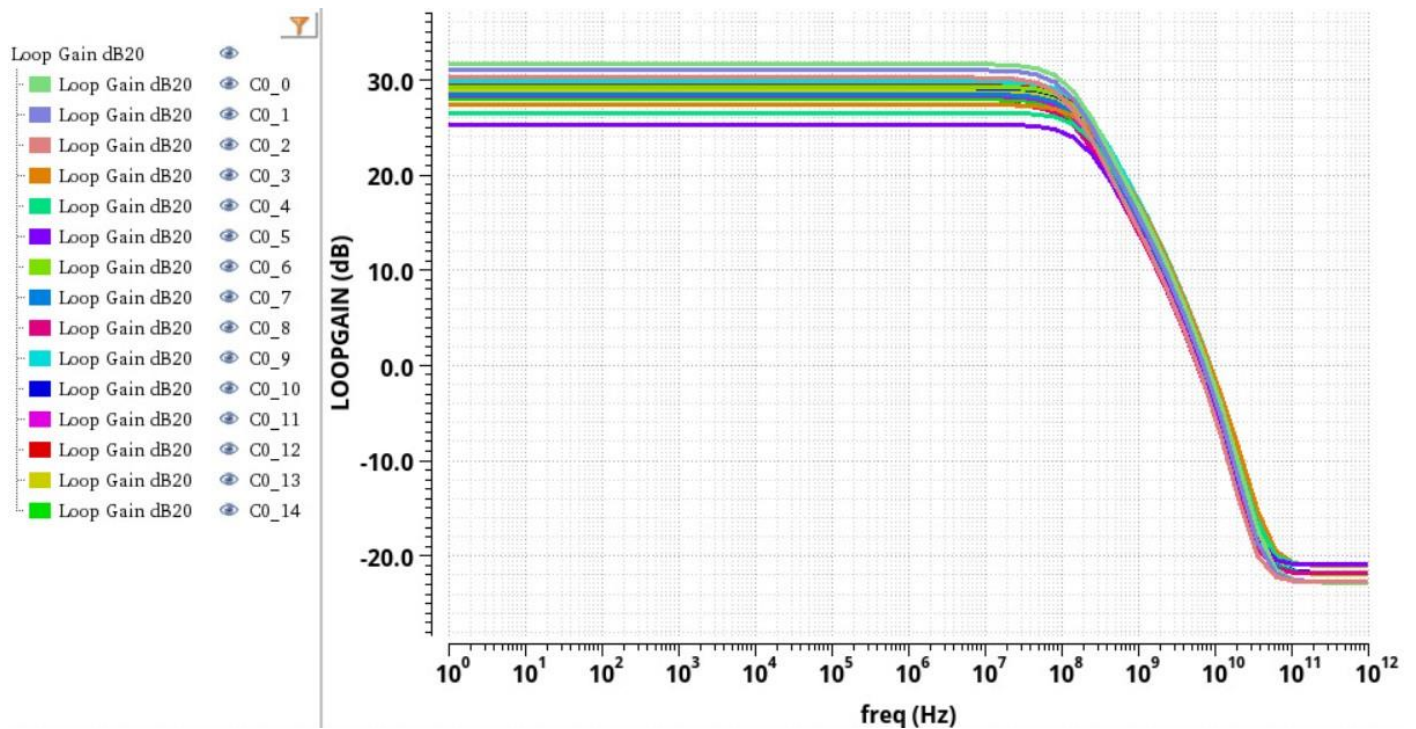


Fig 21 Variation of loop phase around corners



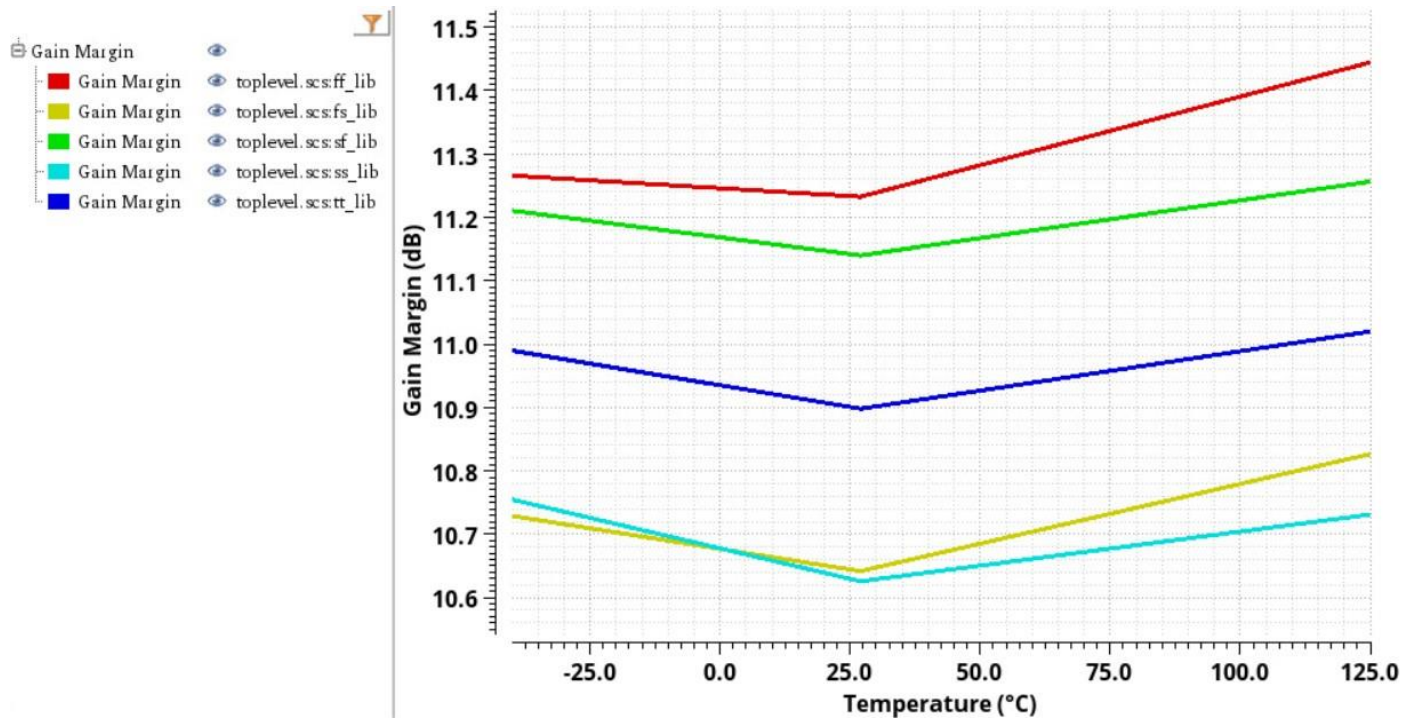


Fig 22 Variation of Gain Margin around corners.

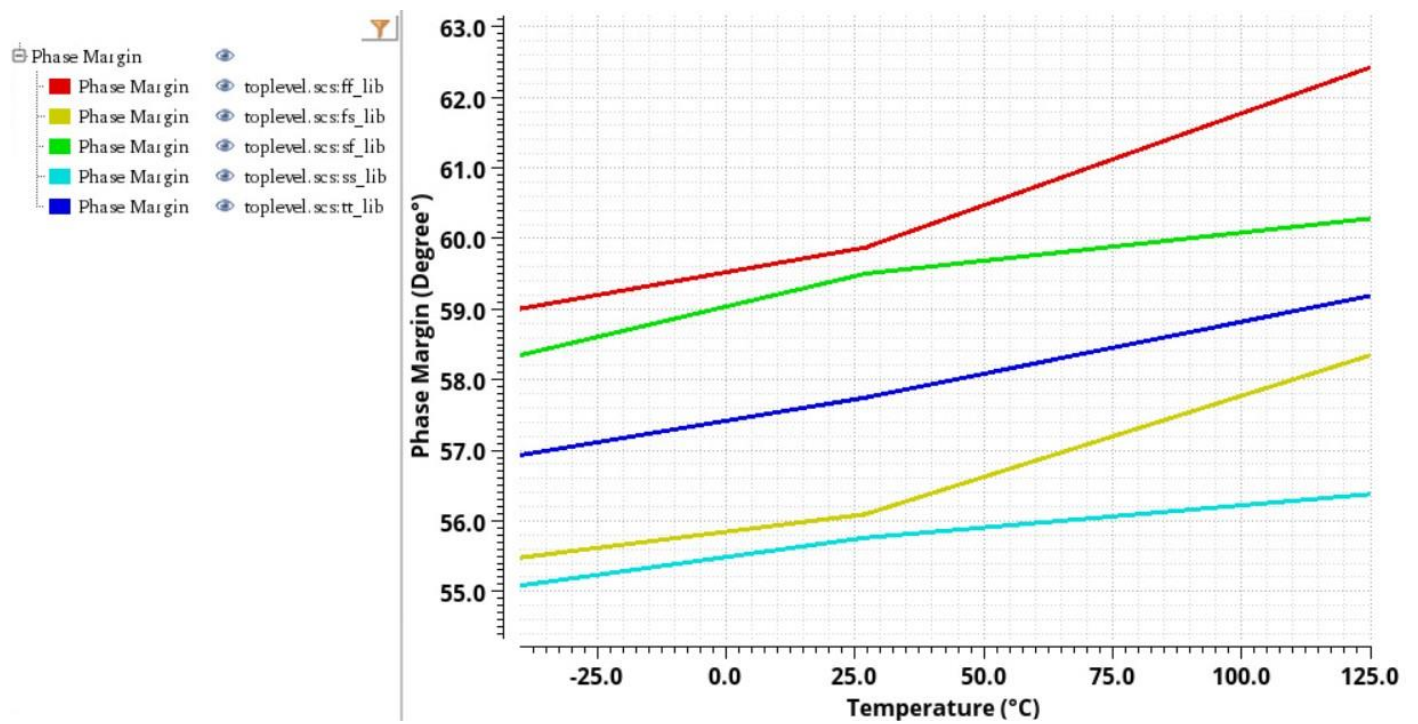


Fig 23 Variation of Phase Margin around corners



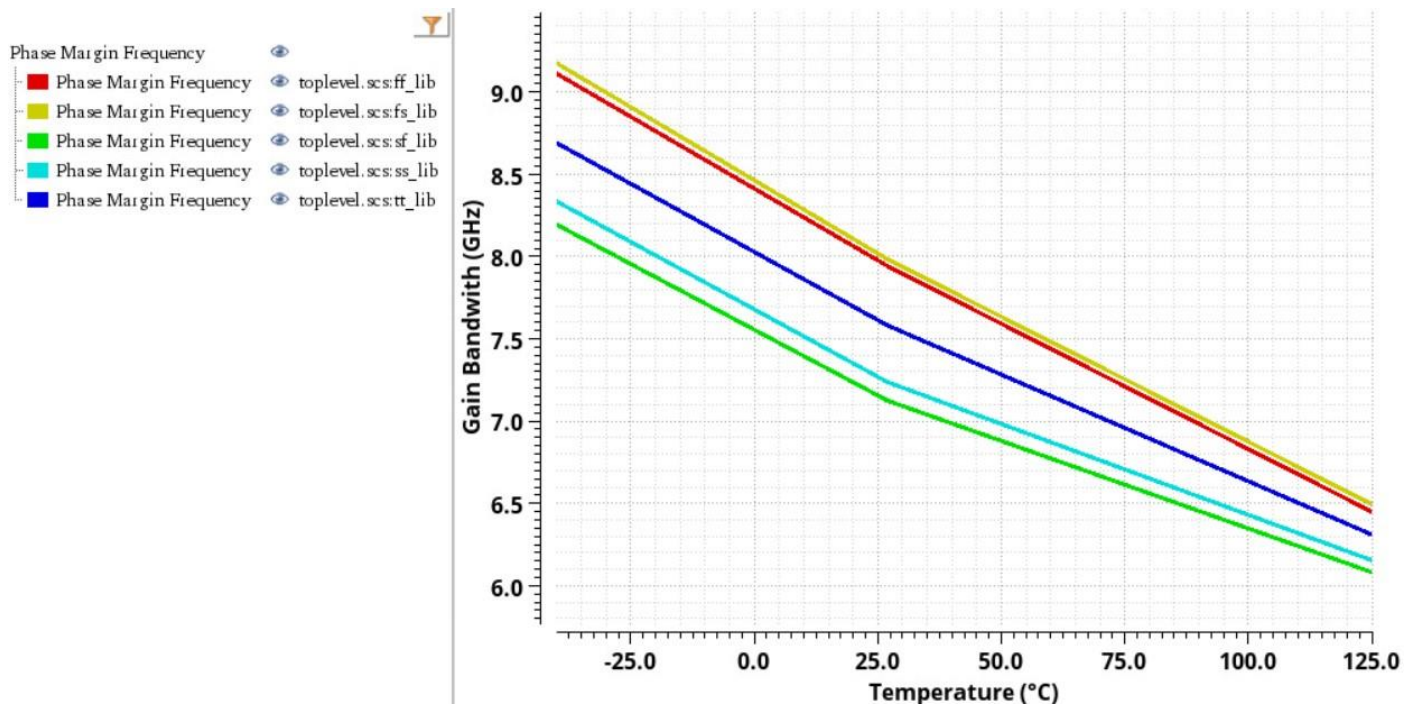


Fig 24 Variation of UGB around Corners

From the above results its clear that the values obtained are within the specification as mentioned in page 2.

Parameter	Min Value	Max Value
Gain Margin (dB)	10.63	11.14
Phase Margin (Degree)	55.08	62.43
UGB (GHz)	6.082	9.174

## 4.2 AC corner analysis of Biquad

Same as above we run corner analysis for AC response of Biquad and see whether we have any deviations. We run corners analysis for AC gain and phase. The results are as plotted below.

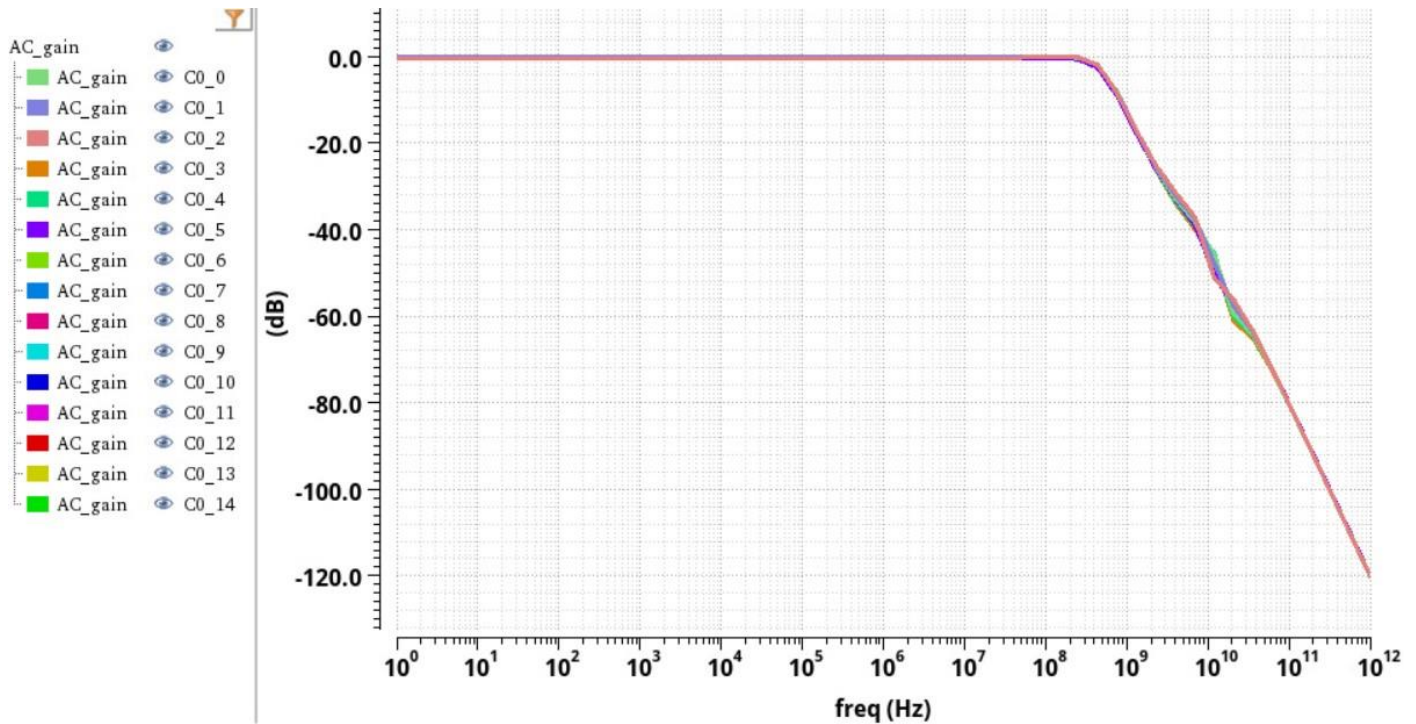


Fig 25 AC gain across different corner analysis.

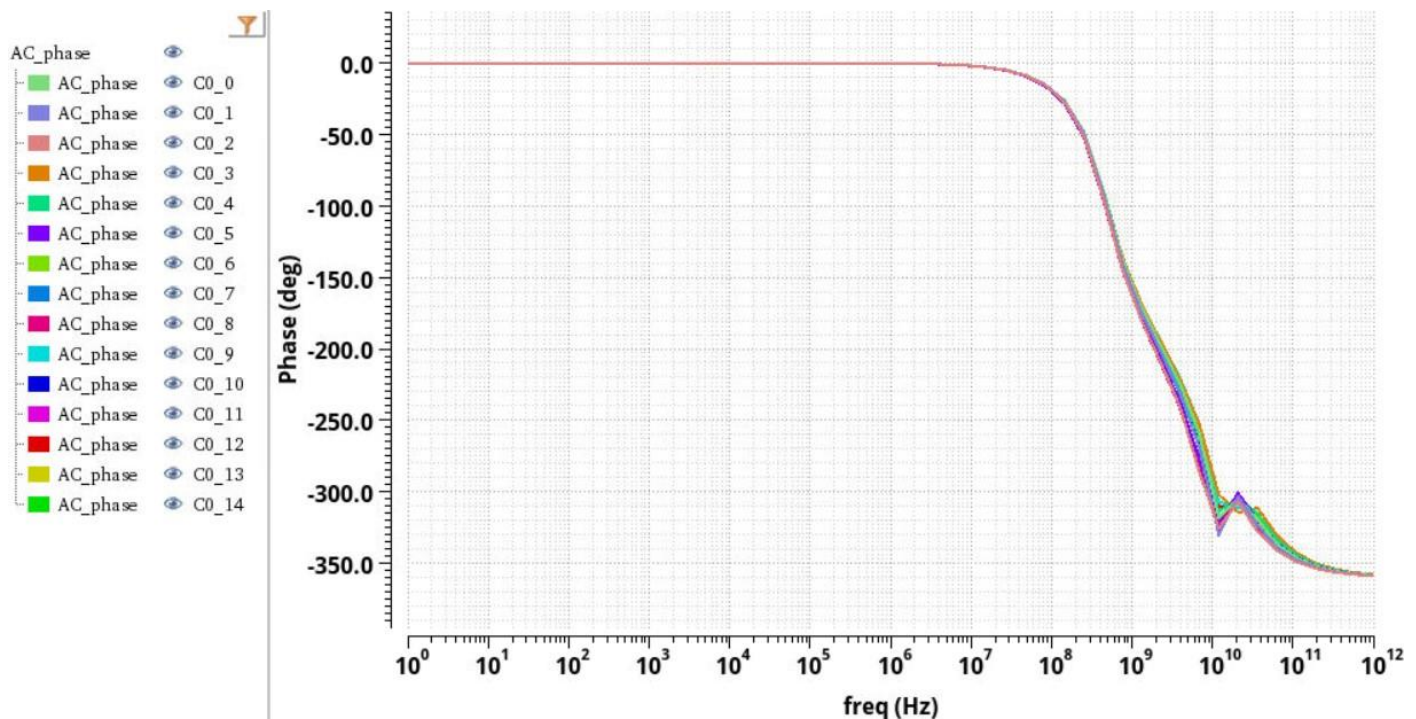


Fig 26 AC Phase across different corner analysis

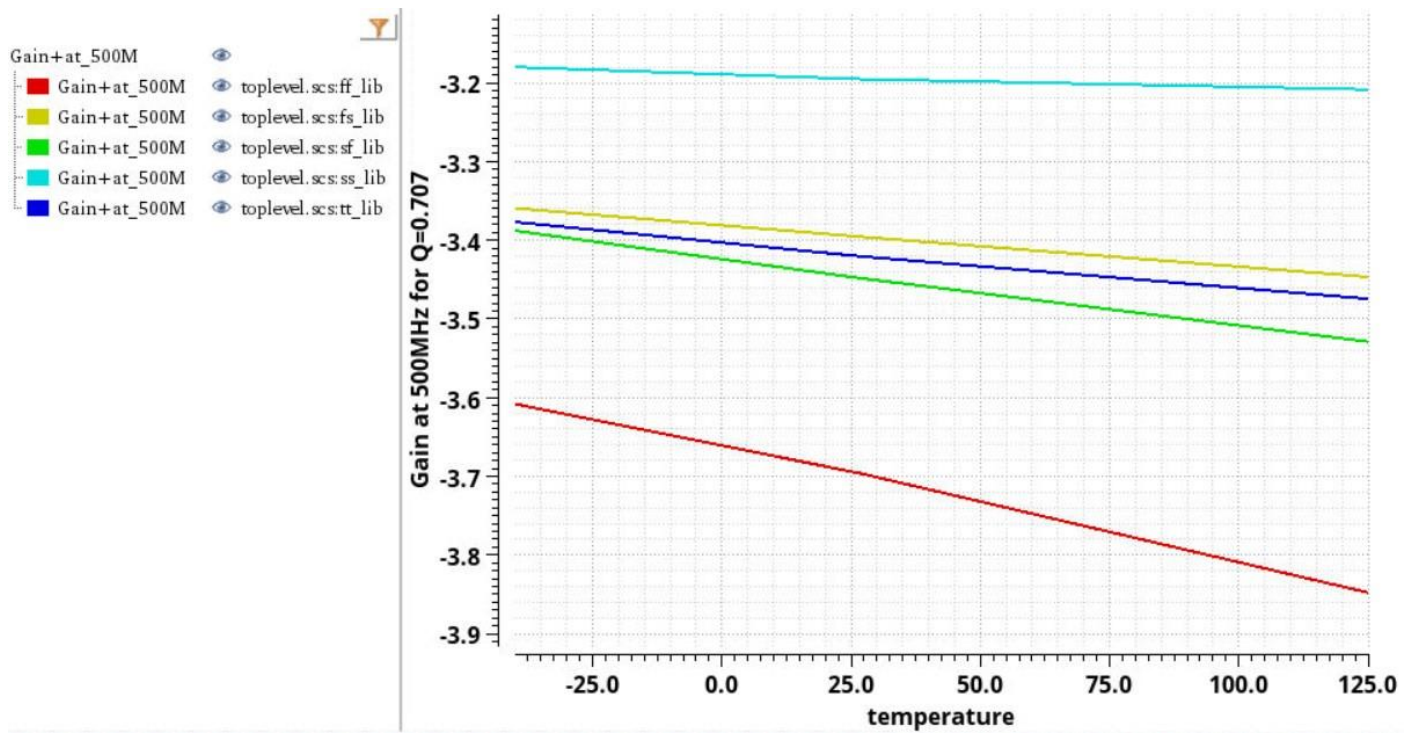


Fig 27 Gain seen at 500MHz at different corner analysis.

Even though the opamp corner analysis is within the specification the degradation of 500MHz gain is seen due to the increase in temperature which increases the resistance and in turn decreasing the cut off frequency.



### 4.3 Linearity Corner Analysis

To see the variation of linearity we use the same spectre from same linearity analysis done earlier and save the expressions in output section.

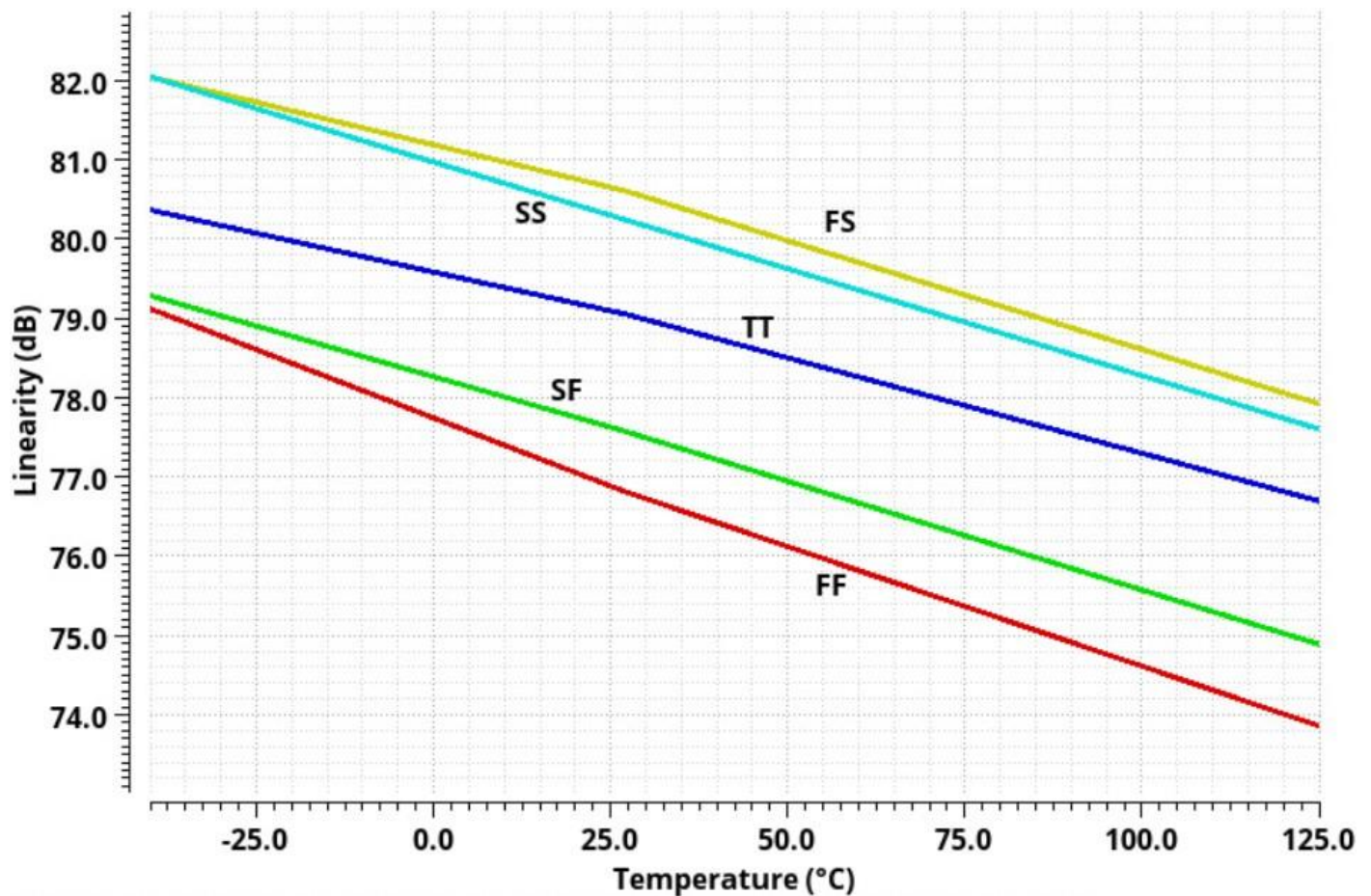


Fig 28 Linearity across different corner analysis

From the above plot we can see there is decrease in linearity with increase in temperature due to increase in leakage current which increases distortion. But the difference in linearity is not huge to be worried about.

Maximum Linearity	82.31 dB
Minimum Linearity	72.02 dB



## 4.4 Noise Corner Analysis

To see the variation of noise we use the same spectre from same noise analysis done earlier and save the expressions in output section.

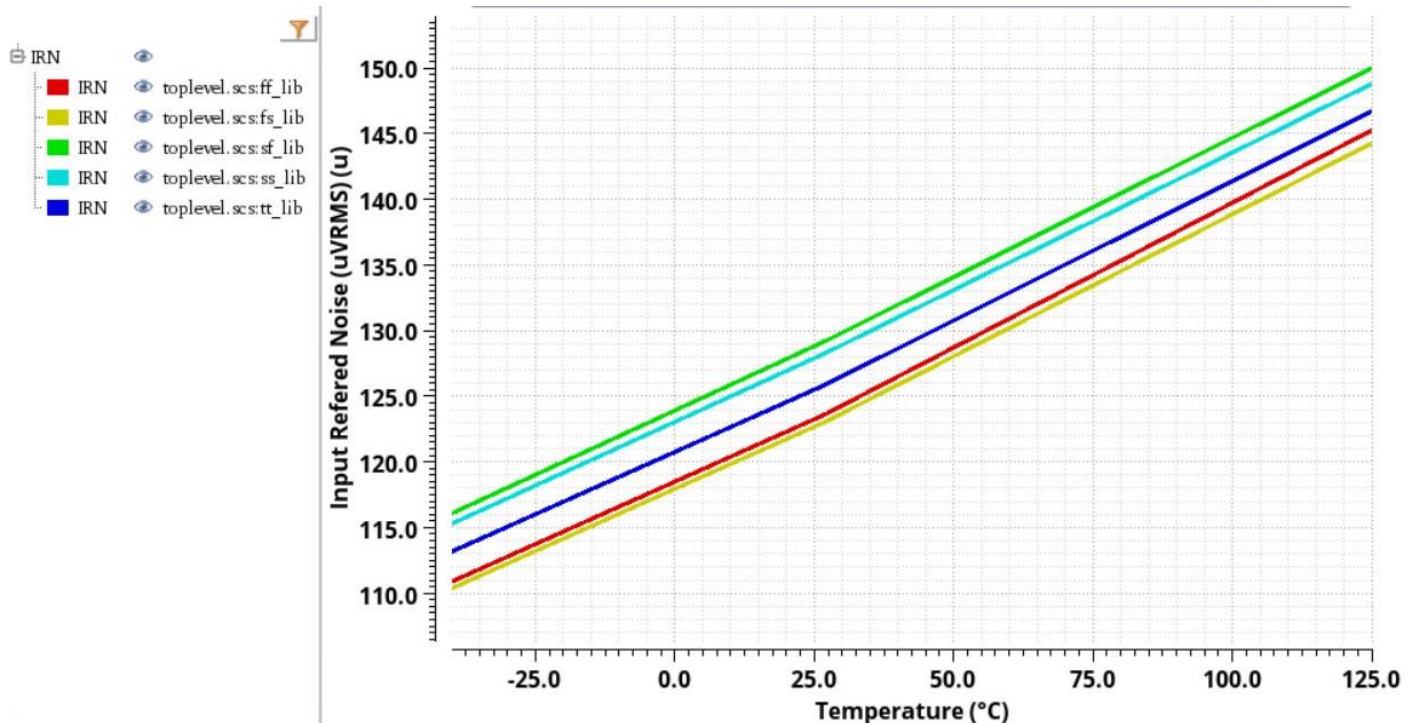


Fig 29 Noise across different corner analysis

The main source of noise is the resistance seen in the opamp and in biquad circuit. As mentioned earlier the resistance increases with temperature which in turn also increase the noise in circuit. The noise however does not have stark difference since its comparably close to 100 uVrms.

Maximum Noise	150 uVrms
Minimum Noise	110.4 uVrms

## 4.5 Transient Corner Analysis

As we have seen earlier the decrease in linearity and gain of 500MHz in biquad we can see its reflection in the transient analysis of different corners. As we see below there is variation in common mode voltage  $\pm 0.8V$  in different corners.

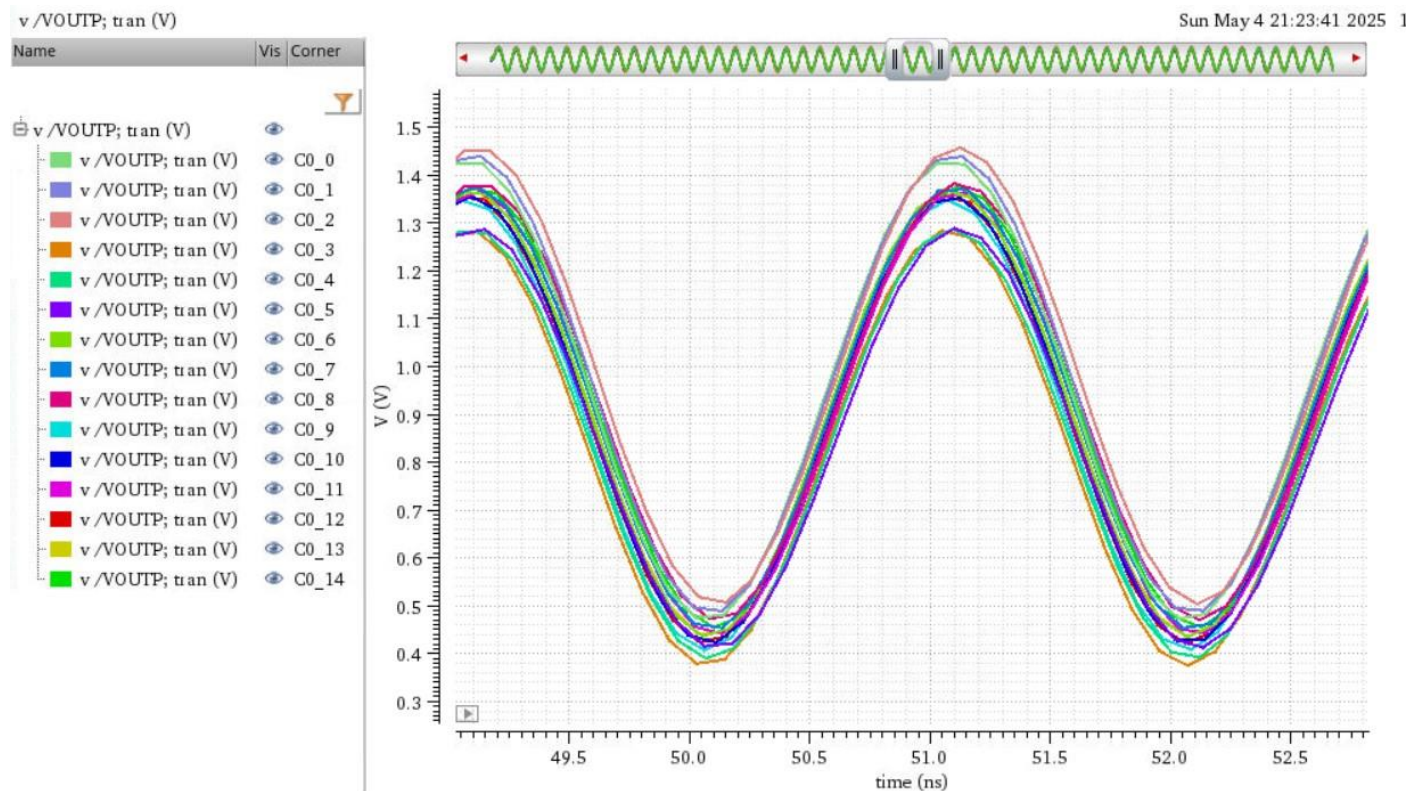


Fig 30 Variation of common mode seen in transient analysis.

There is some variation in upper swing compared to lower swing. This is due to the lower swing hitting an NMOS tail current or mirror, which often allows a cleaner rail-to-rail swing. The upper swing hits PMOS device which is directly connected to VDD.

## 5. References

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