

# Microprocessor and Computer Architecture

UE20CS252

4th Semester, Academic Year 2021-22

Date: 24/1/2022

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Week# 2 Program Number: 1

Title of the Program

**Write an ALP using ARM instruction set to check if a number stored in a register is even or odd. If even, store 00 in R0, else store FF in R0**

- I. ARM Assembly Code(1)
- II. Output Screen Shot (1)  
The output should be verified for both even and odd numbers.
- III. Output table (1)

**I.CODE:**

**.text**

**MOV r1, #8**

**ANDS r2,r1,#1**

**BEQ L1**

**MOV r0,#0xFF**

**B L2**

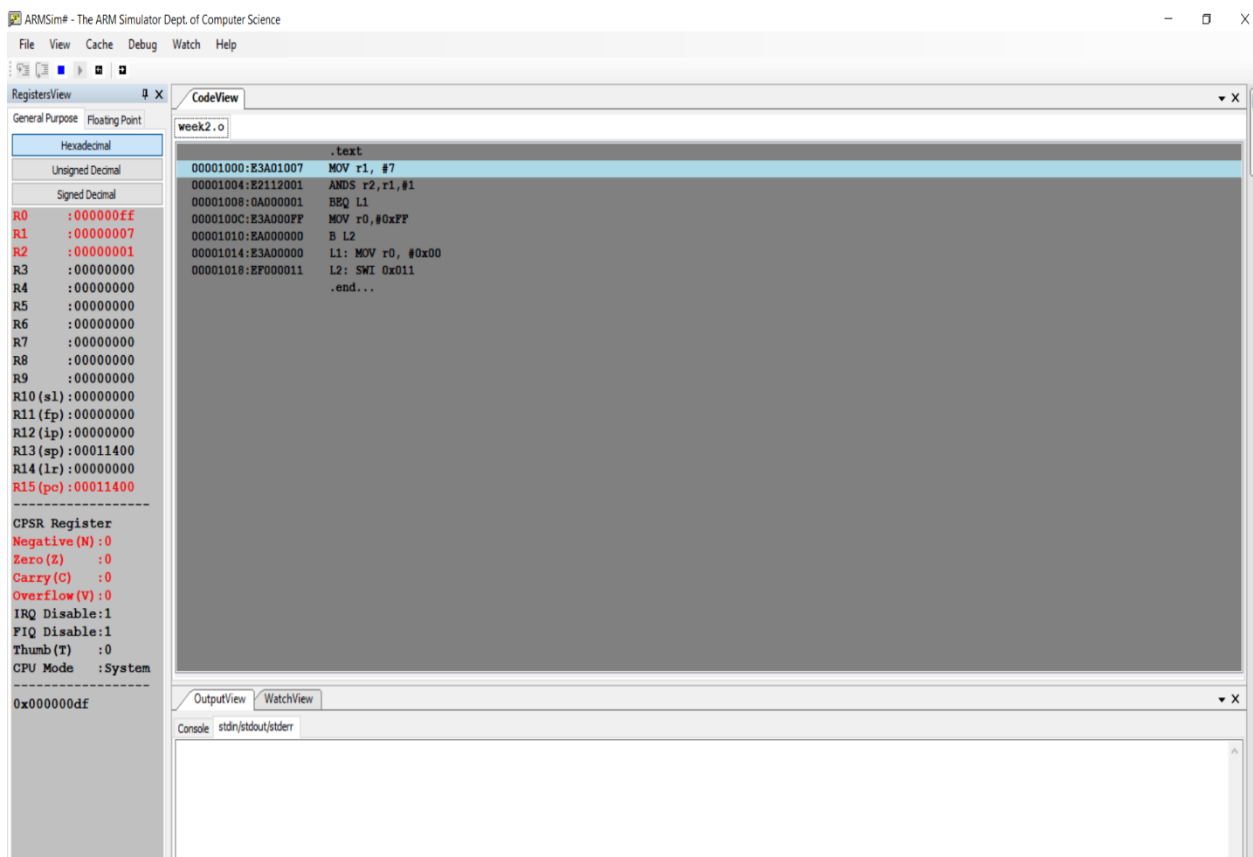
**L1: MOV r0, #0x00**

**L2: SWI 0x011**

**.end**

## II.SCREENSHOT:

**a)for odd number:**



## b)for even number:

ARMSim# - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView CodeView

General Purpose Floating Point

Hexadecimal Unsigned Decimal Signed Decimal

R0 :00000000  
R1 :00000008  
R2 :00000000  
R3 :00000000  
R4 :00000000  
R5 :00000000  
R6 :00000000  
R7 :00000000  
R8 :00000000  
R9 :00000000  
R10 (s1):00000000  
R11 (fp):00000000  
R12 (ip):00000000  
R13 (sp):00011400  
R14 (lr):00000000  
R15 (pc):00011400

CPSR Register  
Negative (N):0  
Zero (Z):1  
Carry (C):0  
Overflow (V):0  
IRQ Disable:1  
FIQ Disable:1  
Thumb (T):0  
CPU Mode :System

0x400000df

week2.o

```
.text
00001000:E3A01008 MOV r1, #8
00001004:E2112001 ANDS r2,r1,#1
00001008:0A000001 BEQ L1
0000100C:E3A000FF MOV r0,#0xFF
00001010:EAD00000 B L2
00001014:E3A00000 L1: MOV r0, #0x00
00001018:EP000011 L2: SWI 0x011
.end...
```

OutputView WatchView

Console stdin/stdout/stderr

# Microprocessor and Computer Architecture

UE20CS253

4th Semester, Academic Year 2021-22

Date:

Name: VISHWAS M	SRN: PES2UG20CS390	Section F
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Week# 1 Program Number: 2

Title of the Program

**Write an ALP to compare the value of R0 and R1, add if R0  
= R1, else subtract**

**I.CODE:**

**.text**

**MOV r0,#7**

**MOV r1,#7**

**CMP r0,r1**

**BEQ L1**

**SUB r2,r0,r1**

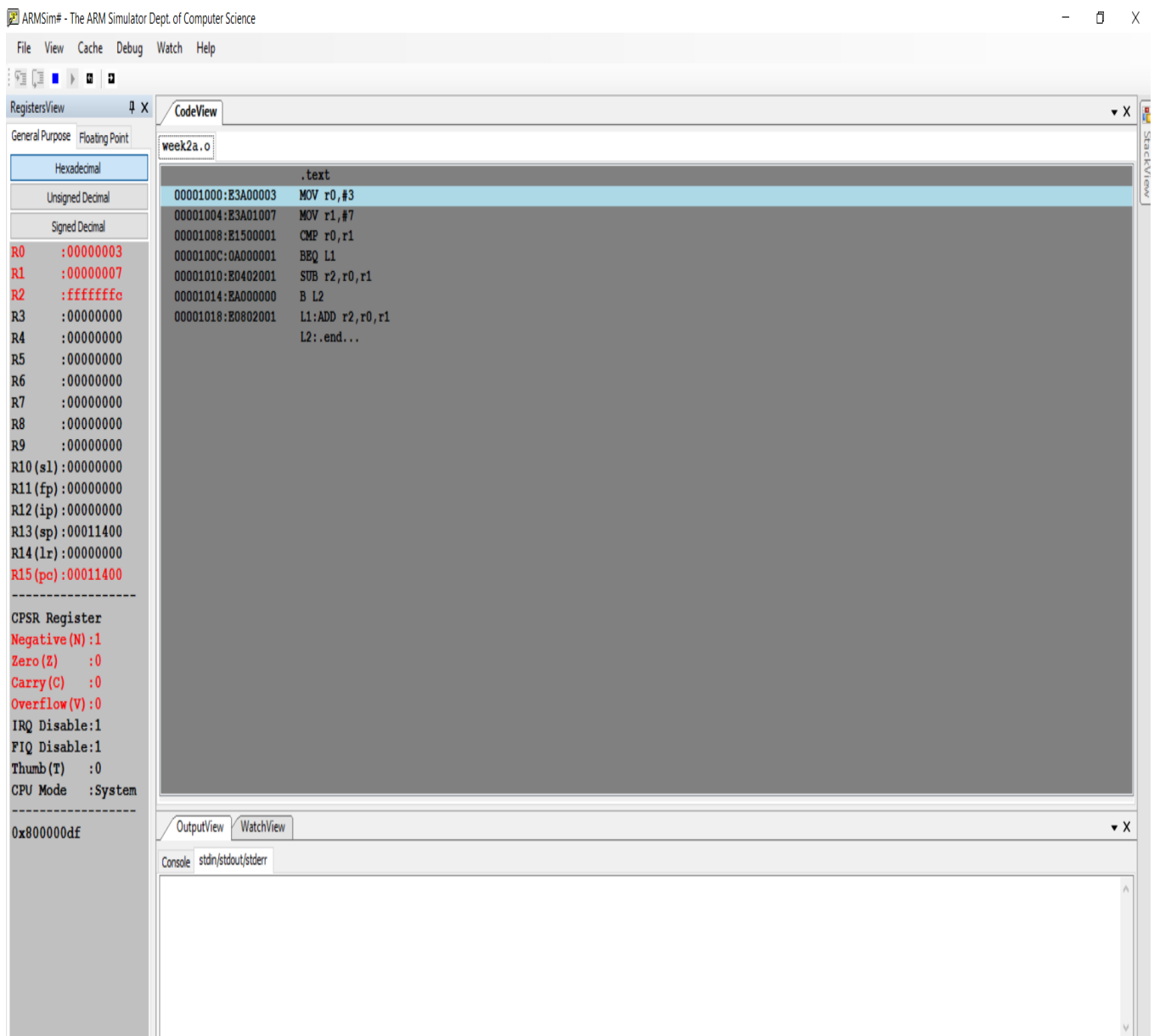
**B L2**

**L1:ADD r2,r0,r1**

**L2:.end**

## II.SCREENSHOT:

**a)for different numbers:**



b)for same numbers:

ARMSim# - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal  
Unsigned Decimal  
Signed Decimal

R0 : 00000007  
R1 : 00000007  
R2 : 0000000e  
R3 : 00000000  
R4 : 00000000  
R5 : 00000000  
R6 : 00000000  
R7 : 00000000  
R8 : 00000000  
R9 : 00000000  
R10 (s1) : 00000000  
R11 (fp) : 00000000  
R12 (ip) : 00000000  
R13 (sp) : 00011400  
R14 (lr) : 00000000  
R15 (pc) : 00011400

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CPSR Register  
Negative(N) : 0  
Zero(Z) : 1  
Carry(C) : 1  
Overflow(V) : 0  
IRQ Disable: 1  
FIQ Disable: 1  
Thumb(T) : 0  
CPU Mode : System

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0x600000df

CodeView

week2a.o

```
.text
00001000:E3A00007 MOV r0,#7
00001004:E3A01007 MOV r1,#7
00001008:E1500001 CMP r0,r1
0000100C:0A000001 BEQ L1
00001010:E0402001 SUB r2,r0,r1
00001014:EA000000 B L2
00001018:E0802001 L1:ADD r2,r0,r1
L2:.end...
```

OutputView WatchView

Console stdin/stdout/stderr

### **Disclaimer:**

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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