POWER AND ENERGY CONSUMPTION OF DIGITAL SYSTEM

Topic: -

Design of Low Power and Low Energy VLSI Domino Logic OR Gate Circuit

INTRODUCTION: -

The power dissipation of the circuit is reduced in normal mode of operation compared to test mode for any low power VLSI designs. This intern reduces the battery life of the device. Therefore, reducing power dissipation during normal operation has become a critical objective in today's any VLSI circuit designs. The power dissipation of the circuit can be reduced at different stages of the circuit by the designers. For any CMOS circuits, power dissipation may be dynamic or static. The dynamic power dissipation exists in CMOS circuit due to switching activates between the test patterns. Various design approaches had been investigated for realizing domino CMOS. The Extensive use of high-speed domino circuits attracts many researchers in this field. There are various issues related to domino circuits, such as power consumption, speed and noise immunity. But the static power dissipation due to leakage in the device. the proposed design uses a smaller number of clocked transistors, thus reduces the dynamic power consumption as well as leakage current to accessible design. Each accessible design and proposed design are replicated utilizing Cadence device at 180nm technology.

A) Conventional Diode Footed Domino Logic OR gate: -

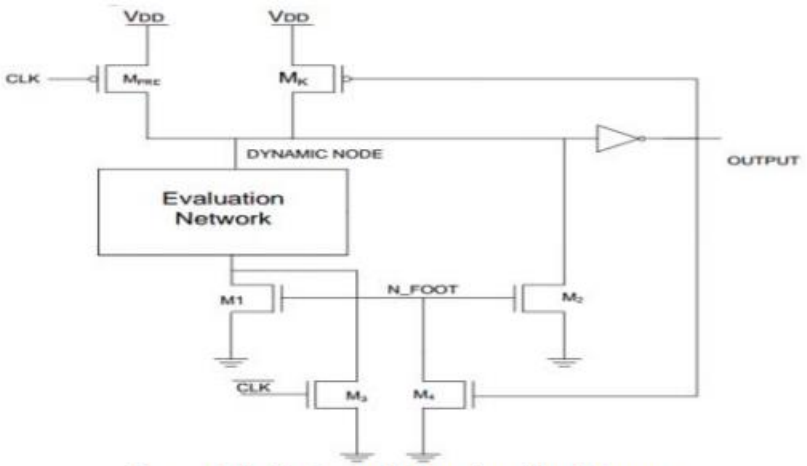


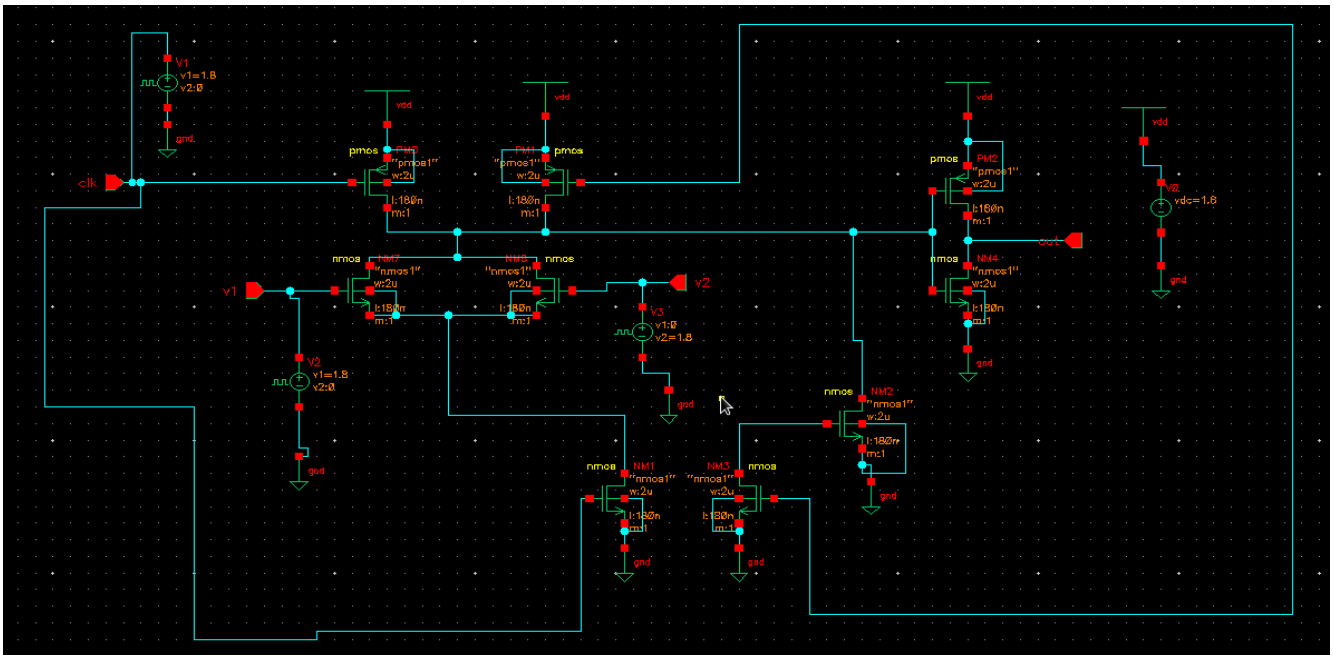
Fig. Diode Footed Domino for OR gate

Diode footed domino OR gate is shown in Figure. Customization to the standard domino circuit has been done by adding an NMOS transistor in a diode configuration in series with the evaluation network as shown in Fig. 3. The diode footer (M1) results in the sub threshold leakage reduction due to the stacking effect. But there is performance degradation due to the diode footer that's why mirror transistor (M2) is employed to increase the performance characteristic.

IMPLIMENTATION: -

the circuit design of Diode Footed Domino Logic for OR gate using cadence platform for 180 nm technology with supply voltage of 1.8v and 100 MHz frequency.

Fig2. Schematic of Diode Footed Domino Logic OR Gate:



Attempts are made to design a domino CMOS circuit in 180nm technology by characterizing the all the transistor in saturation region by keeping 1.8V supply voltage with 100 MHz frequency. The attempt is made to calculate power, area and delay for the design. Then an attempt is made to bring some changes in the structural and logical implementation to reduce power, area and delay even further. To investigate a new technique to implement the same Domino CMOS circuit even reduced power, area and delay. The proposed technique is compared with existing conventional technique in terms of power, area and delay. Then attempt is made implement this proposed Domino CMOS circuit in any one of the application circuits attempts are made implement this proposed Domino CMOS circuit in any one of the application circuits

B) Modified Conventional Design Proposed Circuit for Domino Logic OR gate: -

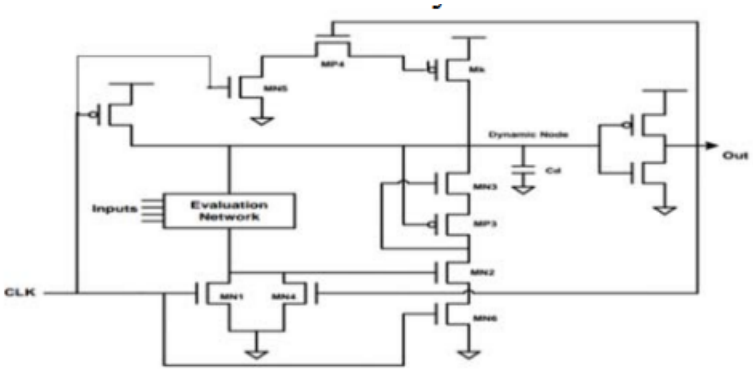


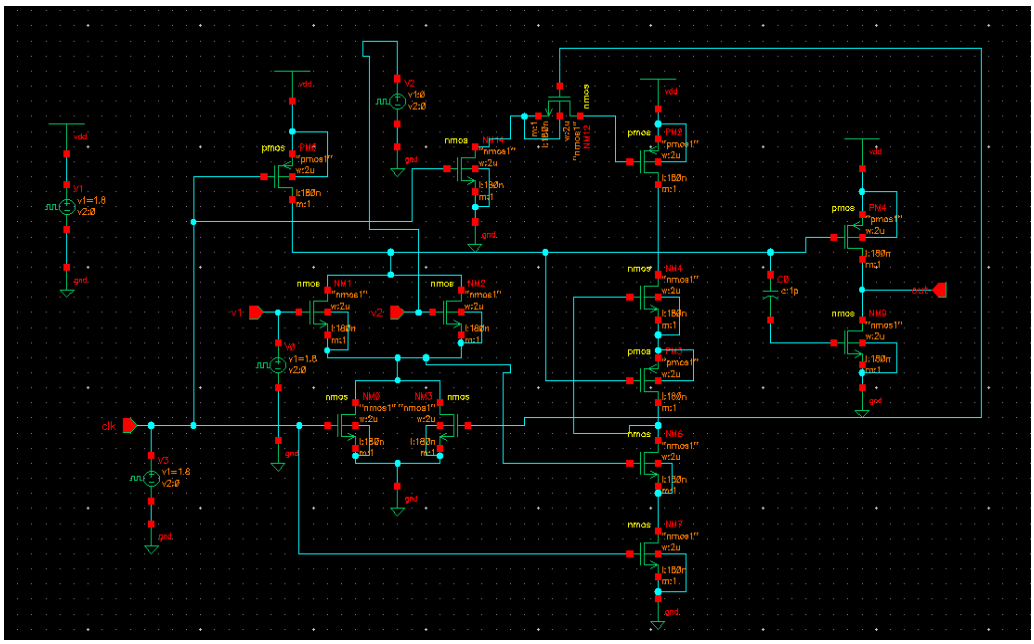
Fig. Proposed Circuit 2 for Domino Logic OR gate

The proposed circuit shown in Figure consists of an extra enable signal, which should be enabled always to get static output even in pre-charge phase. The circuit operation is as follows: when the clock is low (normally said as recharge phase), the transistor MN1 is in OFF condition. According to the input logics dynamic node may charge to VDD or discharged to GND. If inputs make dynamic node to discharge to footer voltage, then this potential makes use of level restorer to discharge and also can provide the exact outputs irrespective of the clock. An external enable signal here, so the GND level is brought up to the keeper circuit if no inputs make to discharge the dynamic node and more than one transitions are allowed in every case.

IMPLIMENTATION: -

the circuit design of proposed circuit 2 domino logic for OR gate using cadence platform for 180 nm technology with supply voltage of 1.8v and 100 MHz frequency.

Fig1. Schematic of proposed Circuit for Domino Logic OR gate



Attempts are made to design a domino CMOS circuit in 180nm technology by characterizing the all the transistor in saturation region by keeping 1.8V supply voltage with 100 MHz frequency. The attempt is made to calculate power, area and delay for the design. Then an attempt is made to bring some changes in the structural and logical implementation to reduce power, area and delay even further. To investigate a new technique to implement the same Domino CMOS circuit even reduced power, area and delay. The proposed technique is compared with existing conventional technique in terms of power, area and delay. Then attempt is made implement this proposed Domino CMOS circuit in any one of the application circuits

SIMULATED OUTPUTS: -

The simulated outcomes of Domino Logic OR gate using Cadence Virtuoso tool using 180nm CMOS technology with supply potential of 1.8V. By using the Diode Footed techniques the power dissipation and energy get optimized. Specifically, the proposed circuit method for Domino Logic OR gate design gives better result in terms of power dissipation and static power and energy.

Fig3.simulated transient output of Diode Footed Domino Logic OR gate: -

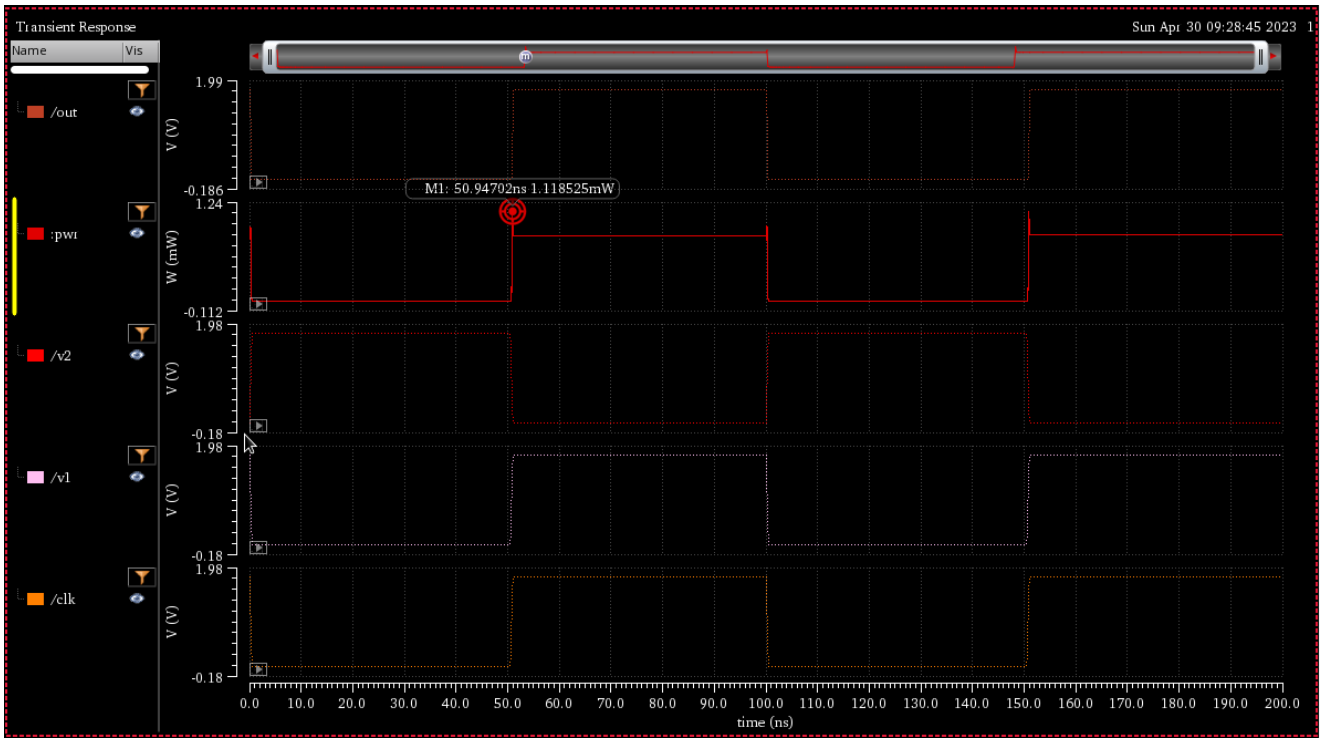


Fig4.simulated transient output of Proposed Circuit Domino Logic OR gate: -

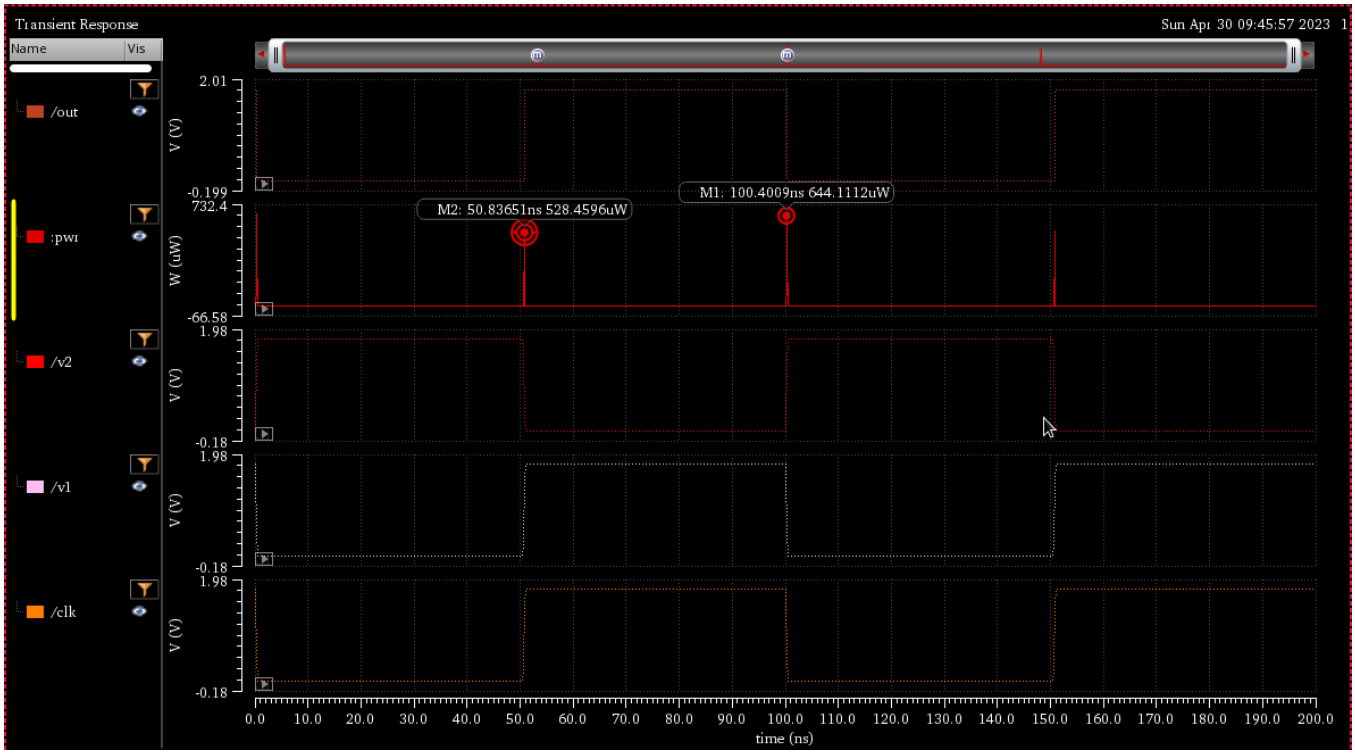


Table1: - Analogy of Domino logic OR gate using different methods

PERFORMANCE PARAMETER	CONVENTIONAL DIODE FOOTED DOMINO LOGIC OR GATE	MODIFIED PROPOSED CIRCUIT DOMINO LOGIC OR GATE
TECHNOLOGY USED	180nm	180nm
SUPPLY VOLTAGE	1.8V	1.8V
POWER DISSIPATION	406.7E-6	1.344E-6
ENERGY	425.0E-15	136.1E-15
STATIC POWER	68.27E-12	48.73E-12

Conclusion: -

In this initially power and energy are calculated for conventional Diode Footed Domino Logic OR gate and modified conventional proposed circuit Domino Logic OR gate is designed for the 180nm technology with 1.8 supply voltage using cadence virtuoso flat form.

The conventional domino logic design is modified as proposed circuit for domino logic OR gate for domino logic OR gate, which results in better power dissipation and energy compared to conventional designs.