

## TRANSISTORS AND OPERATIONAL AMPLIFIERS

### BJT Transistor: Introduction

- A **bipolar junction transistor (BJT)** is a *three terminal device* consisting of either a p-type semiconductor or n-type semiconductor sandwiched between opposite types. It has **two p-n junctions** connected back-to-back.
- In a BJT, the operation depends on the active participation of both the **majority carriers**, and the **minority carriers**; hence the name “**bipolar**”.
- The combination of two terms *transfer* + *resistor* results in **TRANSISTOR** as the current is transferred from a low to a high-resistance circuit.
- The three terminals of a Bipolar junction transistor are Emitter, Base & Collector.

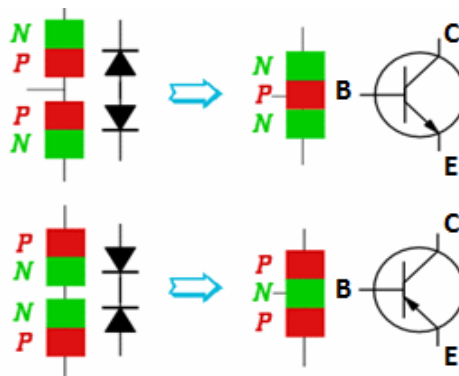
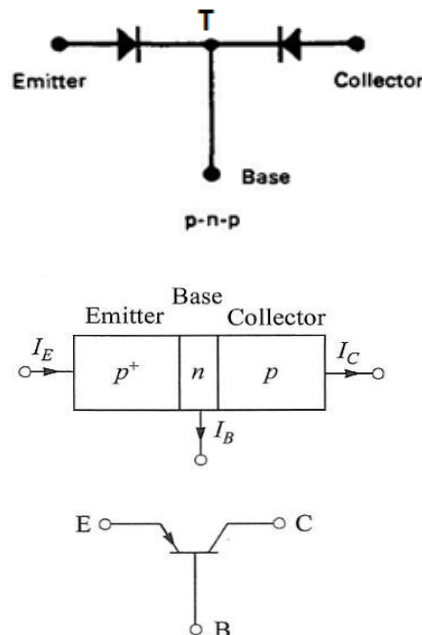
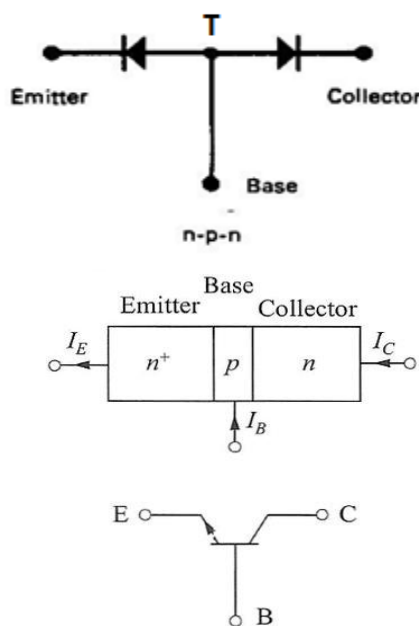
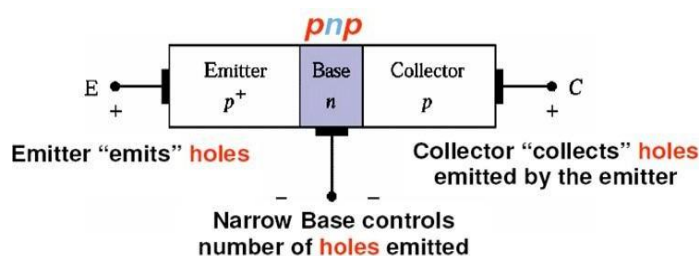


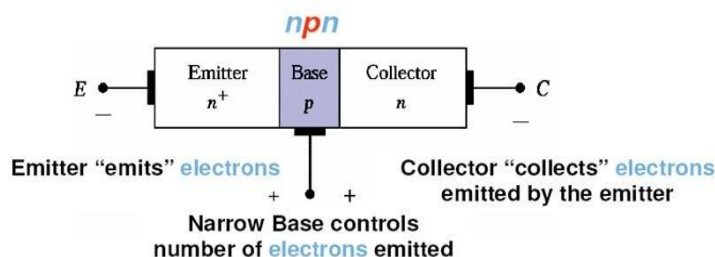
Fig: Transistor symbols

- The **Emitter (E)** is the portion of the transistor that **supplies** charge carriers (either electrons or holes) and it is a **heavily doped** region. The area is moderate in size.
- The **Base (B)** is the **middle** portion of the transistor that forms **two PN junction** between the emitter and the collector and it is a **lightly doped** region. It is the smallest in width of all the three regions.
- The **Collector (C)** is the portion of the transistor that **collects** charge carriers (either electrons or holes) and it is a **moderately doped** region. It is the widest of all the three regions as maximum heat is dissipated in this region.

#### pnp Transistor :



#### nnp Transistor :



### Transistor Configurations

Based on the terminal common to the input and output side of the transistor, following are the transistor configurations:

- 1) **Common Base (CB)** configuration
- 2) **Common Emitter (CE)** configuration
- 3) **Common Collector (CC)** configuration

### BJT Biasing and Modes of operation

A Transistor has two p-n junctions.

- 1) Emitter-base (EB) Junction
- 2) Collector-base (CB) Junction
  - Each junction can either be **forward or reverse biased** independently.
  - Depending on the bias we have the following regions of operation of BJT.

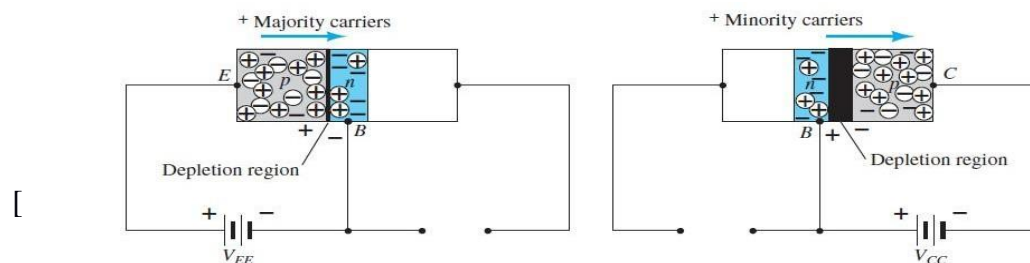
Regions of Operation	Emitter-base Junction	Collector-base Junction	Application
Active region( <i>commonly used</i> )	Forward biased	Reverse biased	Transistor works as an Amplifier
Saturation region	Forward biased	Forward biased	Transistor works as a switch (ON)– Digital Application
Cut-off region	Reverse biased	Reverse biased	Transistor works as a switch (OFF)– Digital Application
Inverse active region( <i>rarely used</i> )	Reverse biased	Forward biased	Transistor works as an Attenuator

## BJT Operation

The transistor operated in **Common Base** configuration, with the external sources, **VEE** and **VCC**, connected as shown:

- The emitter – base junction is **forward biased**
- The collector – base junction is **reverse biased**

As the EB junction is forward biased the current flow is because of majority charge carriers. Similarly as the CB junction is reverse biased the current flow is because of minority charge carriers (Hence wider depletion region)



- A large number of majority carriers will diffuse across the forward biased p-n junction into the n -type material.
- Since the n -type material is very thin and lightly doped, a very small number of these (holes) will recombine with the electrons in base region and flow through the base terminal as base current (is typically in the order of microamperes).
- Thus, a larger number of these majority carriers from the emitter region will diffuse across the reverse-biased junction into the p -type material connected to the collector terminal.

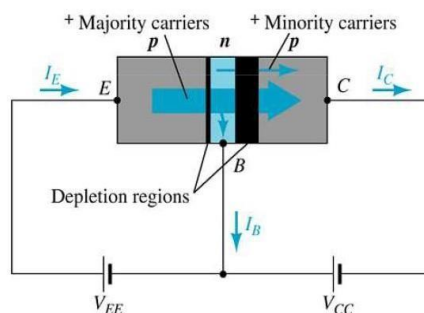


Fig: Currents in BJT

### BJT Operation (pnp transistor)

In the above figure both biasing potentials have been applied to a p-n-p transistor, with resulting majority and minority carriers flow indicated. Since Emitter-Base junction is forward biased, depletion region is very narrow and collector-base junction is reverse biased, depletion region is wider. A large number of majority carriers will diffuse across the forward-biased p-n junction into the n-type material.

Since the sandwiched n-type material is very thin and has a low conductivity, a small number of these carriers will take this path of high resistance to the base terminal. The magnitude of the base current is typically on the order of micro-amperes, as compared to milliamperes for the emitter to collector currents.

The larger number of these majority carriers will diffuse across the reverse biased junction into the p-type material connected to the collector terminal. The reason for the relative ease with which the majority carriers can cross the reverse-biased junction is easily understood if we consider that for the reverse-biased diode the injected majority carriers will appear as minority carriers in the n-type material.

In other words, there has been an injection of minority carriers into the n-type base region material. Combining this with the fact that all the minority carriers in the depletion region will cross the reverse-biased junction of a diode accounts for the flow as shown in figure.

Applying KCL to the transistor, we get

$$I_E = I_C + I_B$$

The collector current comprises two components namely the majority and the minority carriers.

The minority current is called as leakage current ( $I_{CO}$ )

$I_{CO} = I_C$  with emitter terminal open

The collector current, therefore, is determined in total by

$$I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}$$

### BJT Operation (npn transistor)

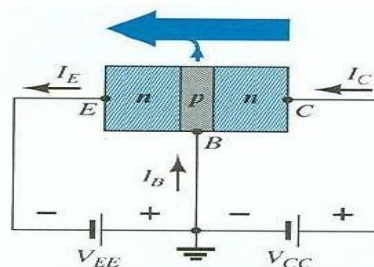
#### Currents in a transistor

- Emitter current is the sum of the collector and base currents:

$$I_E = I_C + I_B$$

- The collector current is comprised of two currents:

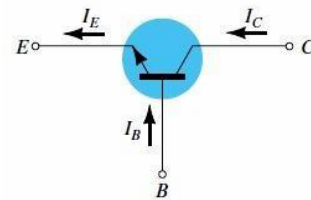
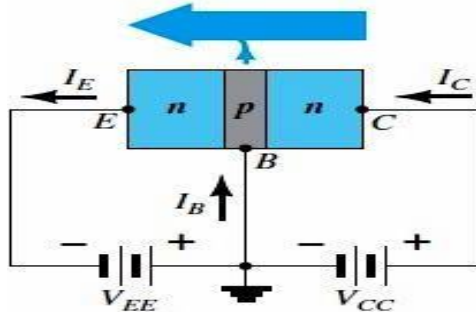
$$I_C = I_{C_{\text{Majority}}} + I_{CO_{\text{Minority}}}$$



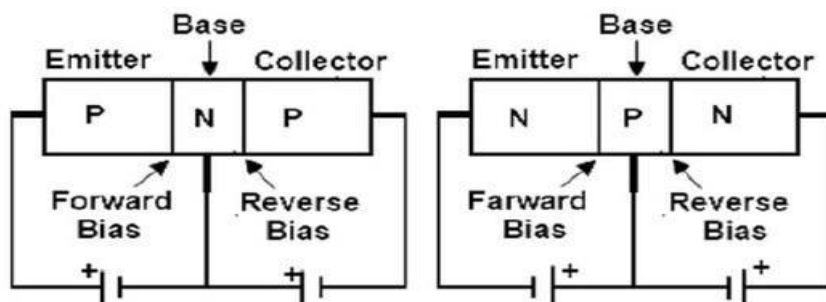
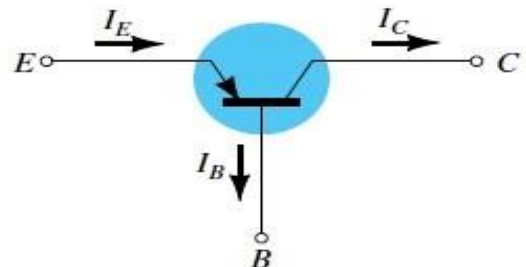
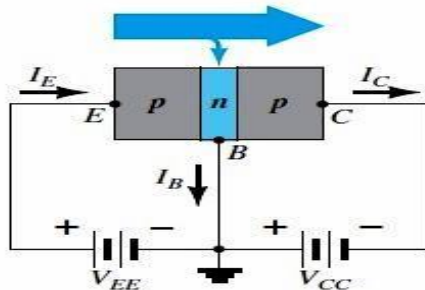
Current directions in a BJT

## Common Base Configuration

- The arrow in the diagram indicates the direction of the emitter current.
- Easy way to remember matching the letters *n**p**n* of the transistor type and with the appropriate letters of the phrases “*not pointing in*”
- The **NPN** transistor requires two voltage sources **VEE** and **VCC** to bias the two junctions respectively.

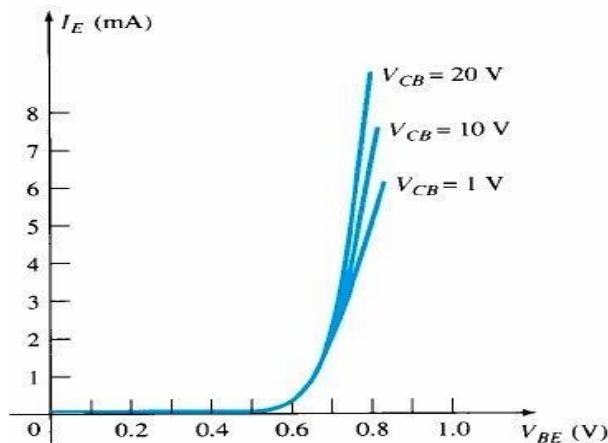


- The arrow in the diagram, indicates the direction of the emitter current and matching the letters *p**n**p* of the transistor type and with the appropriate letters of the phrases “*pointing in permanently*”
- The **PNP** BJT requires two voltage sources **VEE** and **VCC** to bias the two junctions respectively

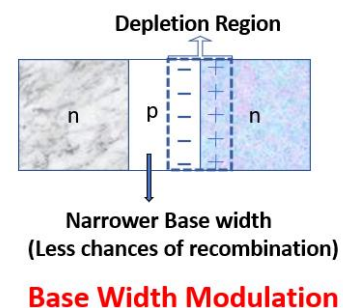


The biasing of **PNP** and **NPN** transistors to operate in active region

- Since the analogy of transistor is two diodes connected back-to-back. One diode is **forward biased** and the other is **reverse biased** for the device to operate in **active region**.
- Hence, biasing the **emitter base junction (EB Jn)** in forward bias condition and **collector base junction (CB Jn)** in reverse bias condition, gives the input characteristic of the device.
- For the transistor in CB configuration, when the output voltage  $V_{CB}$  is increased, it causes an **increase** in the emitter current and hence the graph **shifts inwards or towards the left**.



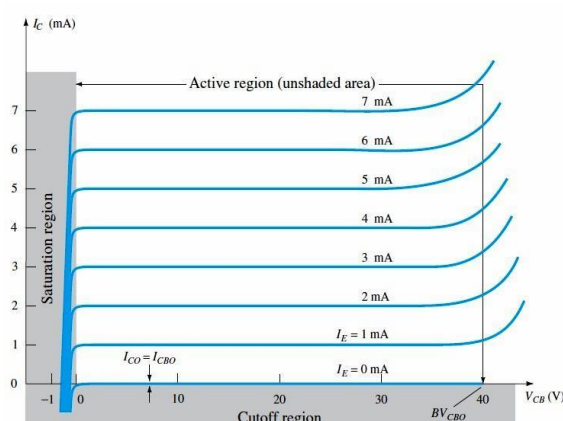
The input characteristic of BJT (Si)  
for varying output voltage  $V_{CB}$



### Base Width Modulation or Early Effect :

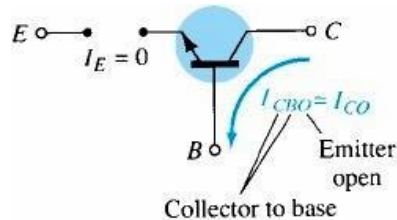
- A greater reverse bias across the collector- base junction increases the collector-base depletion width. There is a variation in the width of the base in a bipolar transistor due to a variation in the applied base-to-collector voltage.
- Base-narrowing has two consequences that affect the current:
  - There is a lesser chance for recombination within the "smaller" base region.
  - The charge gradient is increased across the base, and consequently, the current of minority carriers injected across the collector-base junction increases.
- The Early effect is observed as an increase in the collector or "output" current with increasing collector-emitter voltage.

### CB - Output Characteristics



The output characteristic of BJT (Si)  
for varying input current  $I_E$

- **Active region:** The operating range of the amplifier. It is noticed that  $I_E$  is approximately equal to  $I_C$  ( $I_E \approx I_C$ ). BJT is a current controlled device in the active region and is independent of the output voltage  $V_{CB}$
- **Cut-off region:** The region where the collector current  $I_C$  is approximately equal to 0 ( $I_C < I_{CBO}$ ). The device is basically **OFF** i.e., there's no input voltage, but only reverse – bias output voltage and negligible reverse saturation current



### Reverse saturation current

- **Saturation region:** The region to the left of  $V_{CB} = 0V$ . Note the exponential increase in collector current  $I_C$  as  $V_{CB}$  approaches 0V. In this region,  $I_C$  depends on  $V_{CB}$  but is independent of  $I_E$

### CB Configuration - Approximations

- **Emitter and collector current:**  $I_E \approx I_C$ .
- **Base – emitter voltage ( $V_{BE}$ ):**  $V_{BE} = 0.7V$  (Si).

### Alpha ( $\alpha$ ): Ratio of $I_C$ to $I_E$ .

$$\alpha_{dc} = \frac{I_C}{I_E}$$

$$I_C = \alpha I_E + I_{CBO}$$

Ideally:  $\alpha = 1$

In reality:  $\alpha$  is between 0.9 and 0.998

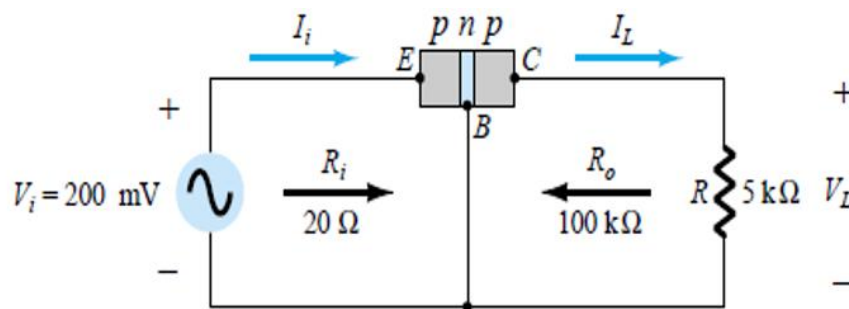
For AC mode:

$$\alpha_{ac} = \left. \frac{\Delta I_C}{\Delta I_E} \right|_{V_{CB}=\text{constant}}$$

$\alpha$  - Current amplification factor or current gain in CB config.



### Common Base Amplifying action



$$I_i = \frac{V_i}{R_i} = \frac{200 \text{ mV}}{20 \Omega} = 10 \text{ mA}$$

If we assume for the moment that  $\alpha_{ac} = 1$  ( $I_c = I_e$ ),

$$I_L = I_i = 10 \text{ mA}$$

and

$$\begin{aligned} V_L &= I_L R \\ &= (10 \text{ mA})(5 \text{ k}\Omega) \\ &= 50 \text{ V} \end{aligned}$$

The voltage amplification is

$$A_v = \frac{V_L}{V_i} = \frac{50 \text{ V}}{200 \text{ mV}} = 250$$

### Numerical

1. A common base transistor amplifier has an input resistance of  $20 \Omega$  and output resistance of  $100 \text{ k}\Omega$ . The collector load is  $1 \text{ k}\Omega$ . If a signal of  $500 \text{ mV}$  is applied between emitter and base, find the voltage amplification. Assume  $\alpha_{ac}$  to be nearly one.

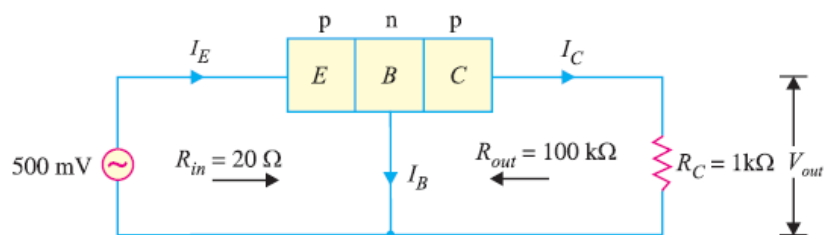


Fig. 1

Input current,  $I_E = \frac{\text{Signal}}{R_{in}} = \frac{500 \text{ mV}}{20 \Omega} = 25 \text{ mA}$ . Since  $\alpha_{ac}$  is nearly 1, output current,  $I_C = I_E = 25 \text{ mA}$ .

$$\text{Output voltage, } V_{out} = I_C R_C = 25 \text{ mA} \times 1 \text{ k}\Omega = 25 \text{ V}$$

$$\therefore \text{Voltage amplification, } A_v = \frac{V_{out}}{\text{signal}} = \frac{25 \text{ V}}{500 \text{ mV}} = 50$$



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2. In a common base connection,  $I_E = 1\text{mA}$ ,  $I_C = 0.95\text{mA}$ . Calculate the value of  $I_B$ .

Using the relation,

$$I_E = I_B + I_C$$

$$1 = I_B + 0.95$$

$$I_B = 1 - 0.95 = \mathbf{0.05\text{ mA}}$$

3. In a common base connection, current amplification factor is 0.9. If the emitter current is 1mA, determine the value of base current.

Here,  $\alpha = 0.9$ ,  $I_E = 1\text{ mA}$

Now  $\alpha = \frac{I_C}{I_E}$

or  $I_C = \alpha I_E = 0.9 \times 1 = 0.9\text{ mA}$

Also  $I_E = I_B + I_C$

$\therefore$  Base current,  $I_B = I_E - I_C = 1 - 0.9 = \mathbf{0.1\text{ mA}}$

4. In a common base connection,  $I_C = 0.95\text{ mA}$  and  $I_B = 0.05\text{ mA}$ . Find the value of  $\alpha$ .

We know  $I_E = I_B + I_C = 0.05 + 0.95 = 1\text{ mA}$

$\therefore$  Current amplification factor,  $\alpha = \frac{I_C}{I_E} = \frac{0.95}{1} = \mathbf{0.95}$

5. In a common base connection, the emitter current is 1mA. If the emitter circuit is open, the collector current is  $50\text{ }\mu\text{A}$ . Find the total collector current. Given that  $\alpha = 0.92$ .

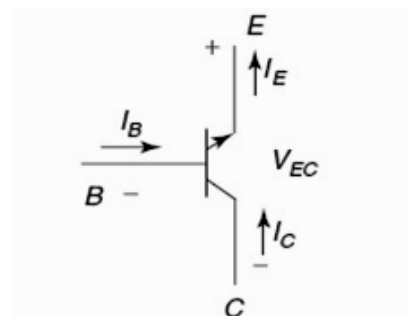
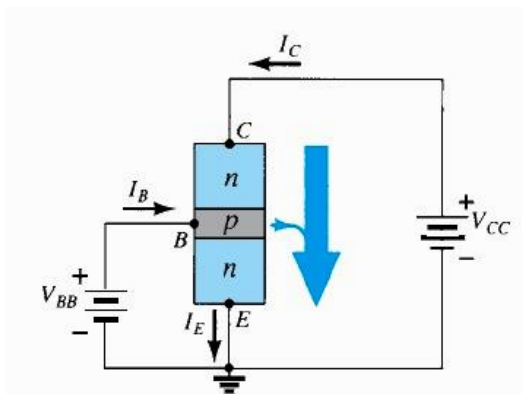
Here,  $I_E = 1\text{ mA}$ ,  $\alpha = 0.92$ ,  $I_{CBO} = 50\text{ }\mu\text{A}$

$\therefore$  Total collector current,  $I_C = \alpha I_E + I_{CBO} = 0.92 \times 1 + 50 \times 10^{-3}$

$$= 0.92 + 0.05 = \mathbf{0.97\text{ mA}}$$

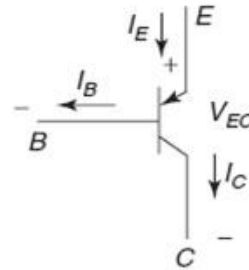
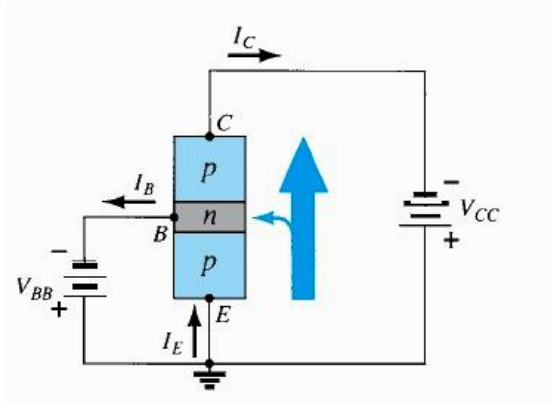
### Common Emitter Configuration

- The arrow in the diagram, indicates the direction of the emitter current.
- The NPN BJT requires two voltage sources  $V_{BB}$  and  $V_{CC}$  to bias the two junctions respectively.

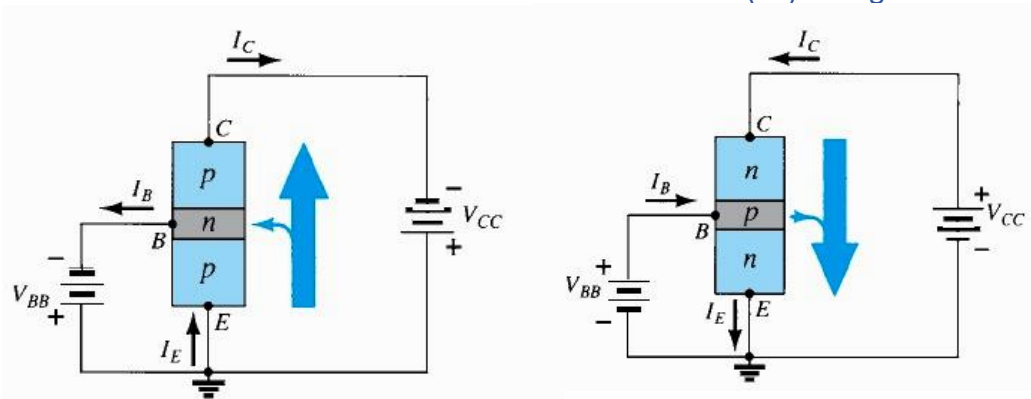


An **NPN** transistor used in Common Emitter (CE) configuration

- The **arrow** in the diagram, indicates the direction of the emitter current and we can observe that the **direction** of the current in this type of transistor is **opposite** to that of a NPN transistor.
- The **PNP** BJT requires two voltage sources **V<sub>BB</sub>** and **V<sub>CC</sub>** to bias the two junctions respectively.



A **PNP** transistor used in Common Emitter (CE) configuration

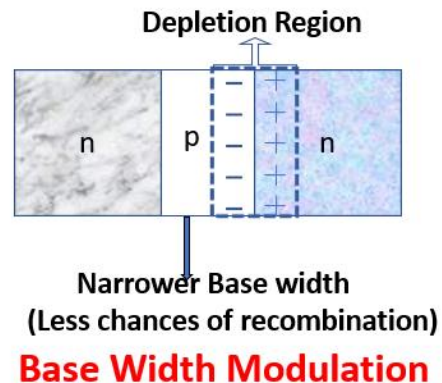
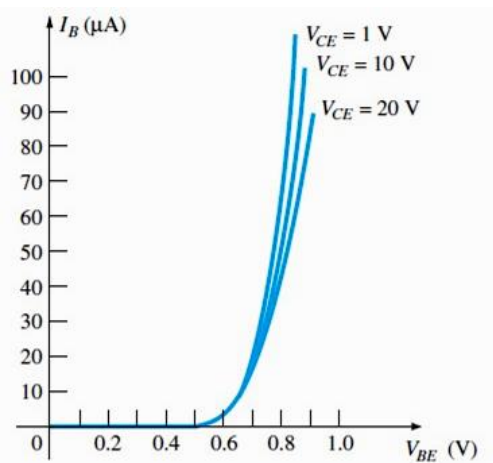


The biasing of **PNP** and **NPN** transistor to operate in active region

- The analogy of a BJT is two diodes connected back-to-back. One diode is **forward biased** and the other is **reverse biased** for the device to operate in **active region**.
- Hence, biasing the **emitter base junction (EB Jn)** in forward bias condition and **collector base junction (CB Jn)** in reverse bias condition, gives the input characteristic of the device.

### CE Configuration - Input Characteristics

- For the transistor in CE configuration, **I<sub>B</sub>** is the input current (usually in  $\mu\text{A}$ ) and **V<sub>BE</sub>** is the input voltage. A plot of **I<sub>B</sub>** v/s **V<sub>BE</sub>** is called the input characteristics.
- The characteristics resemble the forward bias characteristics of a diode.
- When the output voltage **V<sub>CE</sub>** is increased, this high voltage causes a decrease in the current **I<sub>B</sub>** through the device and hence the graph **shifts towards the right**.



The input characteristic of BJT (Si) for varying output voltage  $V_{CE}$

It is called common-emitter configuration because the emitter is common to both the input and output terminals. The input circuit is base-emitter circuit, output circuit is collector-emitter characteristics.

### Base Width Modulation or Early Effect :

- A greater reverse bias across the collector- emitter junction increases the base-emitter depletion width. There is a variation in the width of the base in a bipolar transistor due to a variation in the applied collector- to-emitter voltage.
- Base-narrowing has two consequences that affect the current:
  - There is a lesser chance for recombination within the "smaller" base region & so  $I_B$  decreases further .
  - The charge gradient is increased across the base, and consequently, the current of minority carriers injected across the collector-base junction increases.
- The Early effect is observed as an increase in the collector or "output" current with increasing collector-emitter voltage.

### CE – Output characteristics

- **Active region:** The B-E junction is forward biased. Collector voltage is greater than the base voltage which reverse biases the C-B junction.

$$V_{CE} > V_{BE}$$

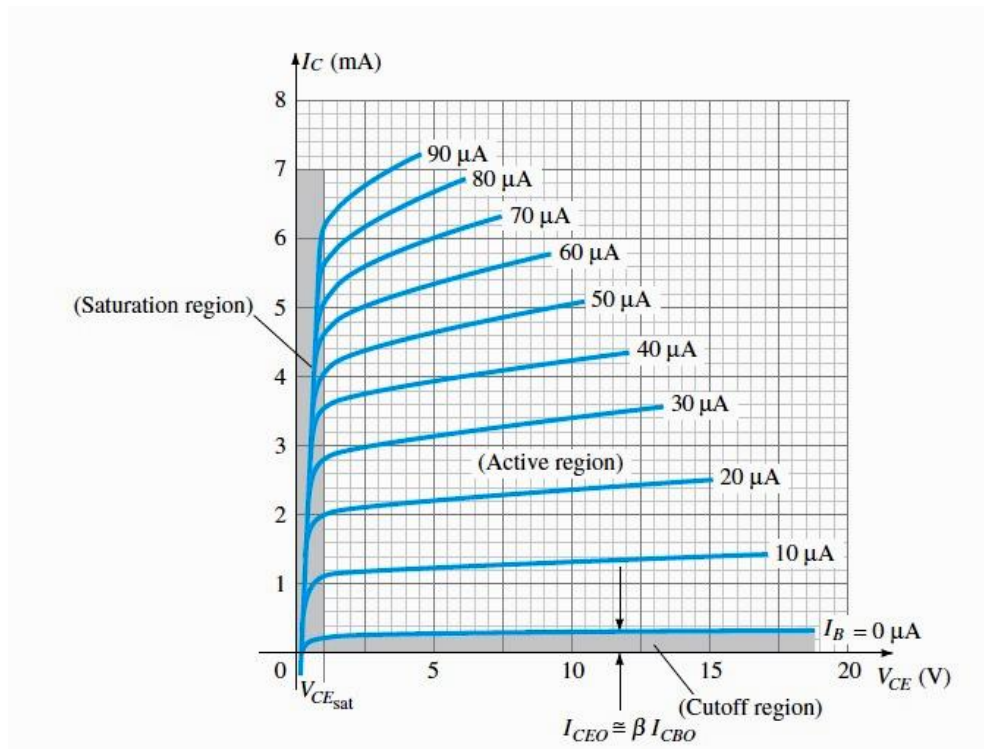
In this region,  $I_C$  depends on  $I_E$  and is almost independent of  $V_{CE}$ .

$$I_C = \beta I_B.$$

- **Cut-off region:** Both junctions are *reverse biased*. No base current. Only a small reverse leakage current between C and E. For practical purposes, current is assumed to be zero.

- **Saturation region:** The E-B and C-B junctions are forward biased.

$I_C$  varies with  $V_{CE}$  and is *independent* of  $I_B$  and  $\beta$ .



The output characteristic of BJT (Si) for varying input current  $I_B$ .

### Relation between $\alpha$ and $\beta$

|

$$I_E = I_C + I_B$$

We know that  $I_C / \alpha = I_E$  and  $I_C / \beta = I_B$ . Using this relation in the above equation we get

$$I_C / \alpha = I_C + I_C / \beta$$

Dividing the above equation by  $I_C$ , we get

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\beta = \alpha \beta + \alpha = (\beta + 1) \alpha$$

$$\alpha = \frac{\beta}{1 + \beta} \quad \text{or} \quad \beta = \frac{\alpha}{1 - \alpha}$$

## Numerical

1. Find the value of  $\beta$  if (i)  $\alpha = 0.9$  (ii)  $\alpha = 0.98$  (iii)  $\alpha = 0.99$ .

(i)  $\alpha = 0.9$

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.9}{1 - 0.9} = 9$$

(ii)  $\alpha = 0.98$

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.98}{1 - 0.98} = 49$$

(iii)  $\alpha = 0.99$

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.99}{1 - 0.99} = 99$$

### Limit of Operation

- The limit of operation ensures that the transistor works within its maximum rating with minimum signal distortion. It is specified in the data sheet.
- $V_{CEsat}$ : Specifies the minimum  $V_{CE}$  that can be applied without transistor going to saturation region.
- The maximum power dissipation is given as

$$P_{C_{max}} = V_{CE} I_C$$

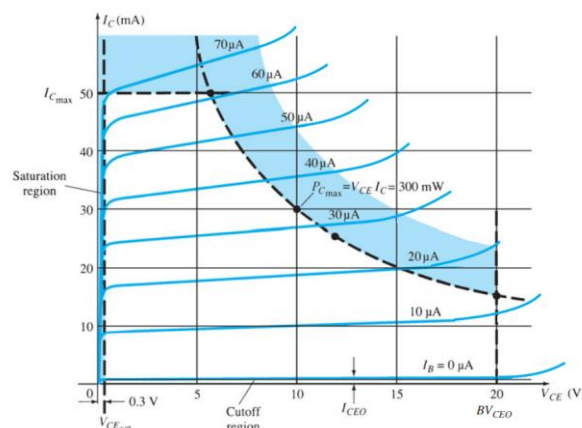


Fig: Defining the linear(Undistorted) region of operation for a transistor

For example if,

$$P_{C_{max}} = V_{CE} \cdot I_C = 300 \text{ mW}$$

At  $I_C = I_{C_{max}}$  i.e, 50 mA,  $V_{CE} = 6 \text{ V}$

At  $V_{CE} = V_{CE_{max}}$  i.e, 20V,  $I_C = 15 \text{ mA}$

At  $I_C = I_{C_{max}}/2$ ,  $V_{CE} = 12 \text{ V}$

These three points give a rough estimate of the power curve and the transistor must be operated within this region.

The cutoff region is the region below  $I_C = I_{CEO}$  ( $= \beta I_{CBO}$ ). This region must also be avoided to have minimum distortion.

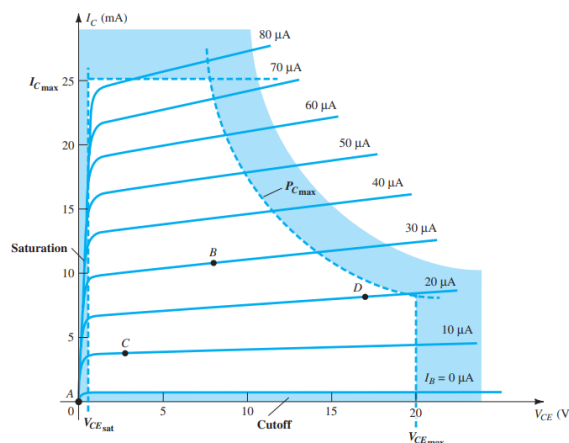
If the characteristic curve/specification sheet is not available, one must ensure the following conditions are satisfied to ensure minimum distortion.

$$\begin{aligned} I_{CEO} &\leq I_C \leq I_{C_{max}} \\ V_{CE_{sat}} &\leq V_{CE} \leq V_{CE_{max}} \\ V_{CE} I_C &\leq P_{C_{max}} \end{aligned}$$

For CB Characteristics,  $P_{C_{max}}$  is defined as  $P_{C_{max}} = V_{CB} \cdot I_C$

### Operating Point

Biassing refers to application of DC voltages to establish a fixed level of current and voltage in a transistor. For a transistor amplifier, the resulting DC current and voltage on the characteristic curve establish an **Operating Point**. This indicates the region of operation of the transistor. Since the operating point is **fixed** on the Characteristic curve, it is also called as **Quiescent point** or **Q point**.



**Fig: Various Operating points within the limits of Operation of a transistor**

Biassing circuit can be used to set the operating point within the active region. A, B, C, D are some of the possible operating points.

- **Q Point at A:** If there is no bias, the device is completely off, resulting in Q point at A. This point is not suitable as complete input range can not be covered for amplification.

- **Q Point at B:** can cover a large range of input signal. It is also far from both cut-off and saturation region.
- **Q Point at C:** This is near to both cutoff and saturation region thus limiting the swing of input signal.
- **Q Point at D:** as is near to the maximum voltage and power level, limits the positive swing of input signal

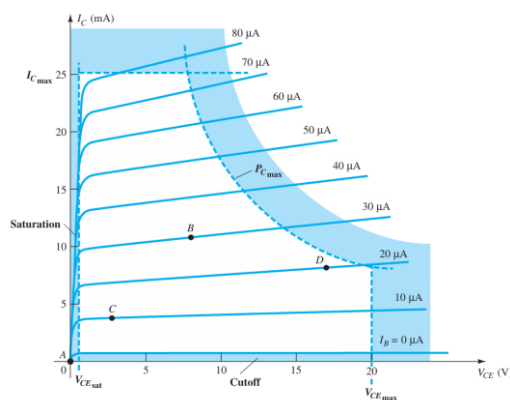


FIG. 4.1  
Various operating points within the limits of operation of a transistor.

Above figure shows a general output device characteristic with four operating points indicated.

The maximum ratings are indicated on the characteristics of figure by

- a horizontal line for the maximum collector current  $I_{Cmax}$  and a vertical line at the maximum collector-to-emitter voltage  $V_{CEmax}$ .
- The maximum power constraint is defined by the curve  $P_{Cmax}$ .
- At the lower end of the scales are the cutoff region, defined by  $I_B = 0$  mA, and the saturation region, defined by  $V_{CE} = V_{CEsat}$ .

### Temperature effect on the Operating point

- Temperature causes the device parameters like transistor current gain ( $\beta_{ac}$ ) and the transistor leakage current ( $I_{CEO}$ ) to change.
- As temperature increases,  $I_{CEO}$  increases, resulting in changing the Q point. Thus the network design must also consider temperature stability to reduce the changes in Q point.
- The variation of operating point due to variation in temperature is indicated by stability factor (S). Higher the stability of the circuit, better is the circuit.

### Transistor Biasing

#### **Transistor Biasing:**

Biasing is the process of providing DC voltage which helps in the functioning of the circuit.



A transistor is biased in order to make the base-emitter junction forward biased and base-collector junction reverse biased, so that it maintains in active region, to work as an amplifier.

**Need for DC biasing:**

If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.

- The input voltage should exceed cut-in voltage for the transistor to be ON.
- The BJT should be in the linear / active region, to be operated as an amplifier.

**DC biasing:**

- The operating point is a fixed point on the characteristics and is also called quiescent point, denoted by Q-point. The term biasing means the application of dc voltages used to setup a fixed level of current and voltage. Called “dc basing” or “biasing analysis”
- This step determines both the region of operation and the small-signal parameters of each device.

**Different regions of operation of BJT**

Operation in the cutoff, saturation, and linear regions of the BJT characteristic are provided as follows:

1. Linear-region (or Active region) operation:

Base-emitter junction forward-biased Base-collector junction reverse-biased

2. Cutoff-region operation:

Base-emitter junction reverse-biased Base-collector junction reverse-biased

3. Saturation-region operation:

Base-emitter junction forward-biased Base-collector junction forward-biased

**Types of BJT Biasing Configuration**

Objective is to determine the terminal voltages and currents of *BJT transistor* and obtain the conditions that ensure biasing in the Active /Linear mode.

Types of Biasing (only the first 3 is included in the syllabus )

1. Fixed Bias configuration
2. Emitter- bias configuration
3. Voltage –divider bias configuration
4. Collector-feedback
5. Emitter-follower
6. Common-base

**1. Fixed Bias configuration**

Fixed bias Configuration is also called as simple biasing.

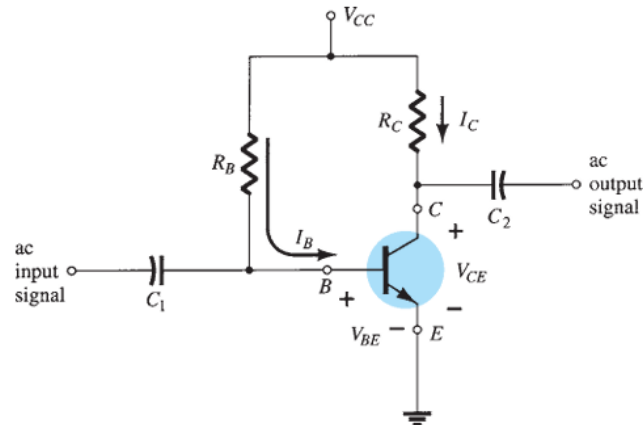


Fig: Fixed Bias Configuration Circuit

For DC, frequency  $f=0$  and  $X_C = \frac{1}{2\pi f c} = \frac{1}{2\pi 0 c} = \infty \Omega$ .

#### Forward Bias of Base–Emitter:

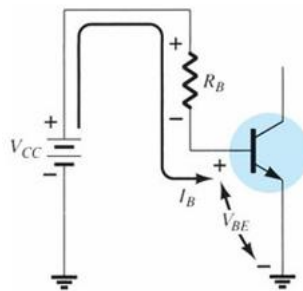


Fig: Base-Emitter Loop

$$I_C = \beta \cdot I_B$$

Applying KVL to base emitter loop,

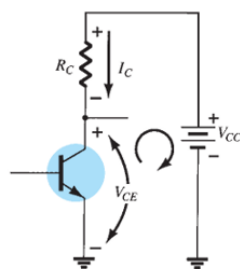
$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

The supply voltages  $V_{CC}$  and  $V_{BE}$  are constants.

The selection of a base resistor sets the level of base current for the operating point.

#### Collector–Emitter Loop :



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Fig: Collector-Emitter Loop

The collector–emitter section of the network appears in above figure with the indicated direction of current  $I_C$  and the resulting polarity across  $R_C$ .

$$I_C = \beta \cdot I_B$$

Changing  $R_C$  to any level will not affect the level of  $I_B$  or  $I_C$  as long as the device is in the active region.

The level of  $R_C$  will determine the magnitude of  $V_{CE}$ .

Applying KVL to Collector-Emitter Loop,

$$V_{CE} + I_C R_C - V_{CC} = 0$$

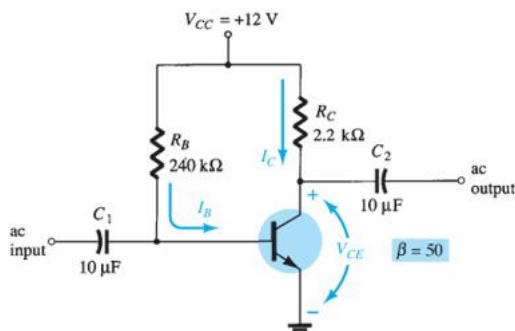
$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E = V_C \quad (\text{As emitter is grounded})$$

$$V_{BE} = V_B - V_E = V_B$$

**Numerical: Determine the following for the fixed-bias configuration of Fig.**

- a.  $I_{BQ}$  and  $I_{CQ}$ .
- b.  $V_{CEQ}$ .
- c.  $V_B$  and  $V_C$ .
- d.  $V_{BC}$ .



**Answer:**

$$\text{a) } I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 \text{ V} - 0.7 \text{ V}}{240 \text{ k}\Omega} = 47.08 \mu\text{A}$$

$$I_{CQ} = \beta I_{BQ} = (50)(47.08 \mu\text{A}) = 2.35 \text{ mA}$$

$$\begin{aligned} \text{b) } V_{CEQ} &= V_{CC} - I_C R_C \\ &= 12 \text{ V} - (2.35 \text{ mA})(2.2 \text{ k}\Omega) \\ &= 6.83 \text{ V} \end{aligned}$$

$$\begin{aligned} \text{c) } V_B &= V_{BE} = 0.7 \text{ V} \\ V_C &= V_{CE} = 6.83 \text{ V} \end{aligned}$$

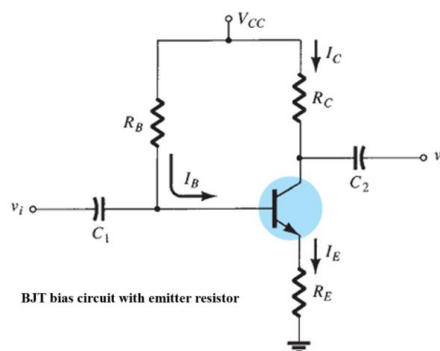
$$\begin{aligned} \text{d) } V_{BC} &= V_B - V_C = 0.7 \text{ V} - 6.83 \text{ V} \\ &= -6.13 \text{ V} \end{aligned}$$

The negative sign revealing that the junction is reversed-biased, as it should be for linear

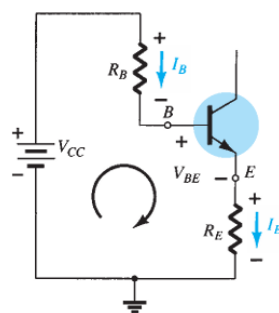
amplification.

## 2. Emitter-Bias Configuration

The DC bias network of fig below contains an emitter resistor to improve the stability level over that of the fixed bias configuration.



### Base-Emitter Loop



Base-emitter loop

Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction results in the following equation:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

Since  $I_E = (\beta + 1)I_B$ , substitute in the above equation

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1)I_B R_E = 0$$

$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

Multiplying through by  $(-1)$ , we have

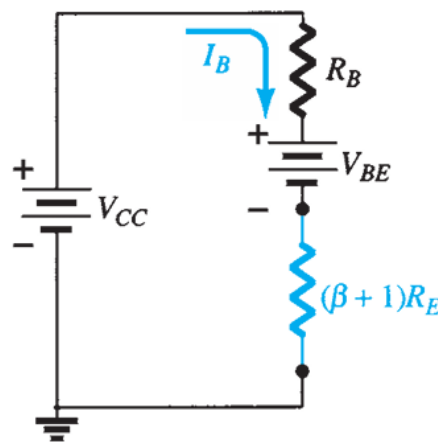
$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

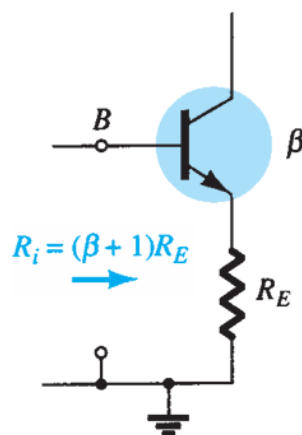
**Note:** that the only difference between this equation for  $I_B$  and that obtained for the fixed bias configuration is the term  $(\beta + 1)R_E$ .

The network derived from this  $I_B$  equation is shown below.

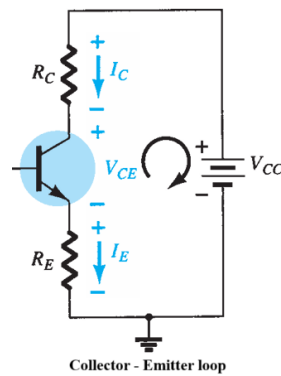


- Note that aside from the base-to-emitter voltage  $V_{BE}$ , the resistor  $R_E$  is reflected back to the input base circuit by a factor  $(\beta + 1)$ .
- In other words, the emitter resistor, which is a part of the collector-emitter loop, “appears as”  $(\beta + 1)R_E$  in the base-emitter loop.
- Thus, the reflected impedance level of  $R_E$  in the base circuit as shown in figure. Therefore, for this configuration the input impedance is given by

$$R_i = (\beta + 1)R_E$$



Collector–Emitter Loop



The collector-emitter loop appears as shown in figure. Applying Kirchhoff's voltage law for the indicated loop in the clockwise direction results in

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting  $I_E \cong I_C$  and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Voltage from emitter to ground is given by

$$V_E = I_E R_E$$

Voltage between collector and emitter is

$$V_{CE} = V_C - V_E$$

Voltage from collector to ground is given by

$$V_C = V_{CE} + V_E$$

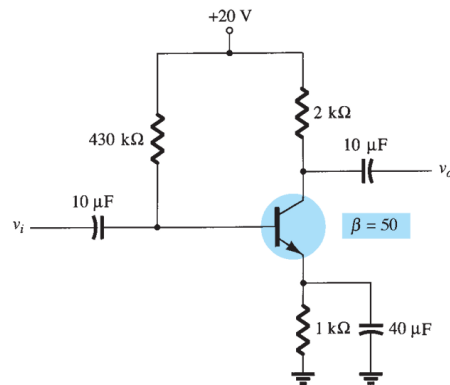
$$V_C = V_{CC} - I_C R_C$$

Voltage at base w.r.t to ground is given by

$$V_B = V_{CC} - I_B R_B$$

$$V_B = V_{BE} + V_E$$

**Numerical: For the emitter-bias network of Figure, determine the following**



- a.  $I_B$ .
- b.  $I_C$ .
- c.  $V_{CE}$ .
- d.  $V_C$ .
- e.  $V_E$ .
- f.  $V_B$ .
- g.  $V_{BC}$ .

**Answer:**

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20 \text{ V} - 0.7 \text{ V}}{430 \text{ k}\Omega + (51)(1 \text{ k}\Omega)}$$

$$= \frac{19.3 \text{ V}}{481 \text{ k}\Omega} = \mathbf{40.1 \mu A}$$

$$I_C = \beta I_B$$

$$= (50)(40.1 \mu A)$$

$$\cong \mathbf{2.01 \text{ mA}}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega + 1 \text{ k}\Omega) = 20 \text{ V} - 6.03 \text{ V}$$

$$= \mathbf{13.97 \text{ V}}$$

$$V_C = V_{CC} - I_C R_C$$

$$= 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega) = 20 \text{ V} - 4.02 \text{ V}$$

$$= \mathbf{15.98 \text{ V}}$$

$$V_E = V_C - V_{CE}$$

$$= 15.98 \text{ V} - 13.97 \text{ V}$$

$$= \mathbf{2.01 \text{ V}}$$

$$V_B = V_{BE} + V_E$$

$$= 0.7 \text{ V} + 2.01 \text{ V}$$

$$= \mathbf{2.71 \text{ V}}$$



$$\begin{aligned}
 V_{BC} &= V_B - V_C \\
 &= 2.71 \text{ V} - 15.98 \text{ V} \\
 &= -13.27 \text{ V (reverse-biased as required)}
 \end{aligned}$$

### Bias Stability in Emitter bias configuration

- The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature and transistor beta, change.
- The comparison table of the bias voltage and currents of the circuits of Fixed and emitter bias for the given value of beta= 50 and for a new value of beta = 100 is shown below.

Fixed bias configuration				Emitter bias configuration			
$\beta$	$I_B (\mu A)$	$I_C (mA)$	$V_{CE} (V)$	$\beta$	$I_B (\mu A)$	$I_C (mA)$	$V_{CE} (V)$
50	47.08	2.35	6.83	50	40.1	2.01	13.97
100	47.08	4.71	1.64	100	36.3	3.63	9.11

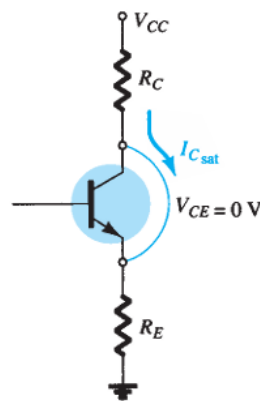
  

The collector current is seen to change by 100% due to the 100% change in the value of beta. The value of $I_B$ is the same, and $V_{CE}$ decreased by 76%				The collector current increases by about 81% due to the 100% increase in beta. $I_B$ decreased, maintain the value of $I_C$ —or at least reducing the overall change in $I_C$ due to the change in beta. The change in $V_{CE}$ has dropped to about 35%			
--	--	--	--	--	--	--	--

- Thus, the emitter – bias configuration is therefore more stable than that of fixed bias for the same change in beta.

### Saturation Level of Emitter Bias Configuration

- The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration
- Apply a short circuit between the collector–emitter terminals as shown in below and calculate the resulting collector current.



$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

### 3. Voltage- Divider Bias Configuration

- In the previous bias configurations, the bias current  $I_{CQ}$  and voltage  $V_{CEQ}$  were a function of the current gain  $\beta$  of the transistor.
- Since,  $\beta$  is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined it is necessary to develop a bias circuit that is less dependent on, or independent of, the transistor beta.
- Thus, Voltage divider bias configuration is preferred.

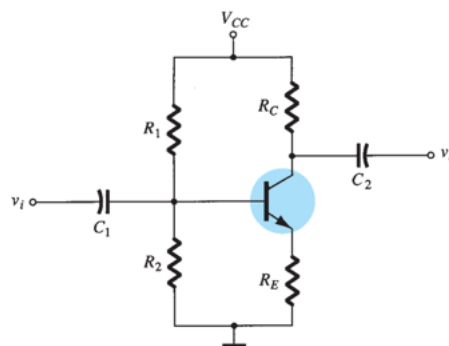
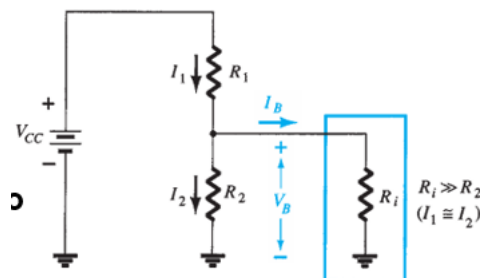


Figure: Voltage Divider Bias Configuration

Approximate Analysis: can be applied only if specific conditions are satisfied. The input section of the voltage-divider configuration can be represented by the network shown below.



- The  $R_i$  is the resistance between base and ground for the transistor with the emitter resistance, with the reflected resistance between the base and emitter, similar to the Emitter bias configuration and is given by  $R_i = (\beta + 1)R_E$ .
- If  $R_i$  is much larger than the resistance  $R_2$ , the current  $I_B$  will be much smaller than  $I_2$  and  $I_2$  will be approximately equal to  $I_1$ . Since,  $I_B \approx 0$ , the voltage drop across  $R_2$  is given by  $\frac{R_2}{R_1 + R_2} V_{CC}$  (using the voltage divider rule, hence the name of the configuration).
- **If  $\beta R_E \geq 10R_2$ , then the approximation method can be applied to determine the biasing current and voltage.**

#### Approximate Analysis:

- $V_E$  and  $I_E$  are calculated by  $V_E = V_B - V_{BE}$  and  $I_E = \frac{V_E}{R_E}$
- $I_{CQ} \cong I_E$
- The collector-to-emitter voltage is determined by  $V_{CE} = V_{CC} - I_C R_C - I_E R_E$
- Since

$$I_E \cong I_C,$$

$$V_{CEQ} = V_{CC} - I_C(R_C + R_E)$$

- In all the biasing voltage and current equation  $\beta$  does not appear and the Q-point (as determined by  $I_{CQ}$  and  $V_{CEQ}$ ) is therefore independent of the value of  $\beta$ .
- Transistor Saturation equation in Voltage- Divider Bias Configuration is given by

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E}$$

**Numerical: Determine the dc bias voltage  $V_{CE}$  and the current  $I_C$  for the voltage divider configuration of Fig.**

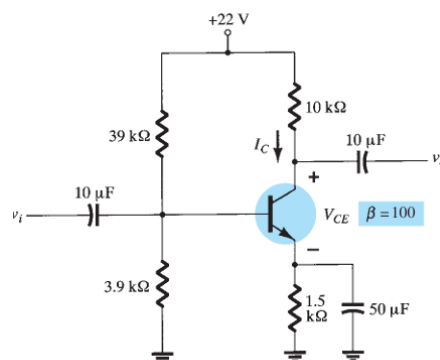


FIG. 4.35

**Answer:**

check the condition to apply approximate method

$$\beta R_E \geq 10R_2$$

$$(100)(1.5 \text{ k}\Omega) \geq 10(3.9 \text{ k}\Omega)$$

$$150 \text{ k}\Omega \geq 39 \text{ k}\Omega \text{ (satisfied)}$$

#### **I<sub>CQ</sub> calculation**

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$= \frac{(3.9 \text{ k}\Omega)(22 \text{ V})}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega}$$

$$= 2 \text{ V}$$

$$V_E = V_B - V_{BE}$$

$$= 2 \text{ V} - 0.7 \text{ V}$$

$$= 1.3 \text{ V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3 \text{ V}}{1.5 \text{ k}\Omega} = \mathbf{0.867 \text{ mA}}$$

#### **V<sub>CEQ</sub> Calculation**

$$V_{CEQ} = V_{CC} - I_C(R_C + R_E)$$

$$= 22 \text{ V} - (0.867 \text{ mA})(10 \text{ k}\Omega + 1.5 \text{ k}\Omega)$$

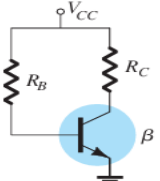
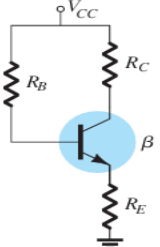
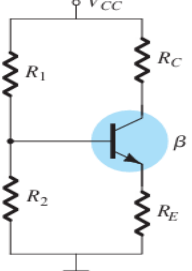
$$= 22 \text{ V} - 9.97 \text{ V}$$

$$= \mathbf{12.03 \text{ V}}$$

### **Summary Table of biasing circuits**

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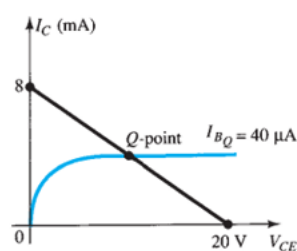
## Dept. of Electronics and Communication Engineering

Type	Configuration	Pertinent Equations
Fixed-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C R_C$
Emitter-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $R_i = (\beta + 1)R_E$ $V_{CE} = V_{CC} - I_C (R_C + R_E)$
Voltage-divider bias		<p>APPROXIMATE: <math>\beta R_E \geq 10R_2</math></p> $V_B = \frac{R_2 V_{CC}}{R_1 + R_2}, V_E = V_B - V_{BE}$ $I_E = \frac{V_E}{R_E}, I_B = \frac{I_E}{\beta + 1}$ $V_{CE} = V_{CC} - I_C (R_C + R_E)$

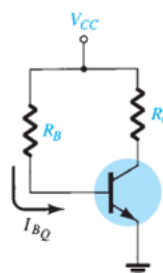
### DESIGN OPERATIONS

- The design process is one where a current and/or voltage may be specified and the elements required to establish the designated levels must be determined.
- This synthesis process requires a clear understanding of the characteristics of the device, the basic equations for the network, and a firm understanding of the basic laws of circuit analysis, such as Ohm's law, Kirchhoff's voltage law, and so on.

**Numerical:** Given the device characteristics of Fig, determine  $V_{CC}$ ,  $R_B$ , and  $R_C$  for the fixed-bias configuration of Fig below.



(a)



(b)

**Answer:**

**R<sub>C</sub> calculation:**

$$V_{CC} = 20 \text{ V}$$

$$I_C = \frac{V_{CC}}{R_C} \Big|_{V_{CE}=0 \text{ V}}$$

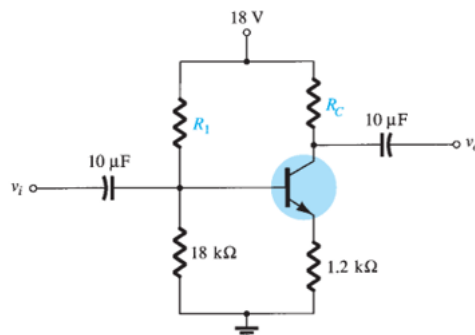
$$R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{8 \text{ mA}} = 2.5 \text{ k}\Omega$$

**R<sub>B</sub> calculation:**

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$\begin{aligned} R_B &= \frac{V_{CC} - V_{BE}}{I_B} \\ &= \frac{20 \text{ V} - 0.7 \text{ V}}{40 \mu\text{A}} = \frac{19.3 \text{ V}}{40 \mu\text{A}} \\ &= 482.5 \text{ k}\Omega \end{aligned}$$

**Numerical: Given that  $I_{CQ} = 2 \text{ mA}$  and  $V_{CEQ} = 10 \text{ V}$ , determine  $R_1$  and  $R_C$  for the network of Fig.**



Answer:

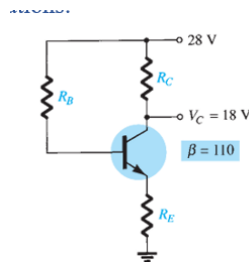
**R1 calculation**

$$\begin{aligned}
 V_E &= I_E R_E \cong I_C R_E \\
 &= (2 \text{ mA})(1.2 \text{ k}\Omega) = 2.4 \text{ V} \\
 V_B &= V_{BE} + V_E = 0.7 \text{ V} + 2.4 \text{ V} = 3.1 \text{ V} \\
 V_B &= \frac{R_2 V_{CC}}{R_1 + R_2} = 3.1 \text{ V} \\
 \frac{(18 \text{ k}\Omega)(18 \text{ V})}{R_1 + 18 \text{ k}\Omega} &= 3.1 \text{ V} \\
 324 \text{ k}\Omega &= 3.1 R_1 + 55.8 \text{ k}\Omega \\
 3.1 R_1 &= 268.2 \text{ k}\Omega \\
 R_1 &= \frac{268.2 \text{ k}\Omega}{3.1} = \mathbf{86.52 \text{ k}\Omega}
 \end{aligned}$$

**Rc Calculation**

$$\begin{aligned}
 R_C &= \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_C}{I_C} \\
 V_C &= V_{CE} + V_E = 10 \text{ V} + 2.4 \text{ V} = 12.4 \text{ V} \\
 R_C &= \frac{18 \text{ V} - 12.4 \text{ V}}{2 \text{ mA}} \\
 &= \mathbf{2.8 \text{ k}\Omega}
 \end{aligned}$$

**Numerical:** The emitter-bias configuration of Fig. 4.61 has the following specifications:  $I_{CQ} = 1/2 I_{C_{sat}}$ ,  $I_{C_{sat}} = 8 \text{ mA}$ ,  $V_C = 18 \text{ V}$ , and  $\beta = 110$ . Determine  $R_C$ ,  $R_E$ , and  $R_B$ .



Answer:

**Rc calculation**

$$\begin{aligned}
 I_{C_Q} &= \frac{1}{2} I_{C_{sat}} = 4 \text{ mA} \\
 R_C &= \frac{V_{R_C}}{I_{C_Q}} = \frac{V_{CC} - V_C}{I_{C_Q}} \\
 &= \frac{28 \text{ V} - 18 \text{ V}}{4 \text{ mA}} = \mathbf{2.5 \text{ k}\Omega}
 \end{aligned}$$



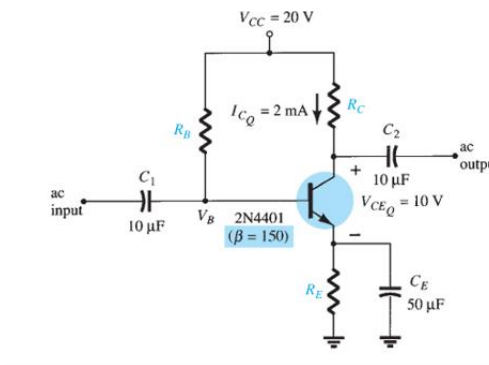
**$R_E$  calculation**

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$
$$R_C + R_E = \frac{V_{CC}}{I_{C_{sat}}} = \frac{28 \text{ V}}{8 \text{ mA}} = 3.5 \text{ k}\Omega$$
$$R_E = 3.5 \text{ k}\Omega - R_C$$
$$= 3.5 \text{ k}\Omega - 2.5 \text{ k}\Omega$$
$$= \mathbf{1 \text{ k}\Omega}$$

 **$R_B$  calculation**

$$I_{B_Q} = \frac{I_{C_Q}}{\beta} = \frac{4 \text{ mA}}{110} = 36.36 \mu\text{A}$$
$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$
$$R_B + (\beta + 1)R_E = \frac{V_{CC} - V_{BE}}{I_{B_Q}}$$
$$R_B = \frac{V_{CC} - V_{BE}}{I_{B_Q}} - (\beta + 1)R_E$$
$$= \frac{28 \text{ V} - 0.7 \text{ V}}{36.36 \mu\text{A}} - (111)(1 \text{ k}\Omega)$$
$$= \frac{27.3 \text{ V}}{36.36 \mu\text{A}} - 111 \text{ k}\Omega$$
$$= \mathbf{639.8 \text{ k}\Omega}$$

**Numerical: Determine the resistor values for the network of Fig for the indicated operating point and supply voltage.**



Answer:

$$V_E = \frac{1}{10} V_{CC} = \frac{1}{10} (20 \text{ V}) = 2 \text{ V}$$

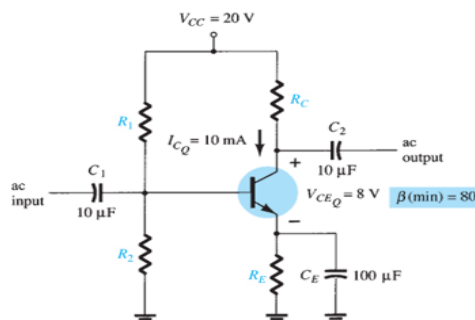
$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2 \text{ V}}{2 \text{ mA}} = \mathbf{1 \text{ k}\Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20 \text{ V} - 10 \text{ V} - 2 \text{ V}}{2 \text{ mA}} = \frac{8 \text{ V}}{2 \text{ mA}} = \mathbf{4 \text{ k}\Omega}$$

$$I_B = \frac{I_C}{\beta} = \frac{2 \text{ mA}}{150} = 13.33 \mu\text{A}$$

$$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V} - 2 \text{ V}}{13.33 \mu\text{A}} \cong \mathbf{1.3 \text{ M}\Omega}$$

**Numerical:** Determine the levels of  $R_C$ ,  $R_E$ ,  $R_1$ , and  $R_2$  for the network of Figure for the operating point indicated.



Answer:

$$V_E = \frac{1}{10} V_{CC} = \frac{1}{10} (20 \text{ V}) = 2 \text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2 \text{ V}}{10 \text{ mA}} = 200 \Omega$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20 \text{ V} - 8 \text{ V} - 2 \text{ V}}{10 \text{ mA}} = \frac{10 \text{ V}}{10 \text{ mA}} = 1 \text{ k}\Omega$$

$$V_B = V_{BE} + V_E = 0.7 \text{ V} + 2 \text{ V} = 2.7 \text{ V}$$

Using  $\beta R_E \geq 10 R_2$ ,

#### **R<sub>2</sub> calculation**

$$R_2 \leq \frac{1}{10} \beta R_E$$

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$R_2 \leq \frac{1}{10} (80) (0.2 \text{ k}\Omega) = 1.6 \text{ k}\Omega$$

#### **R<sub>1</sub> calculation**

$$V_B = 2.7 \text{ V} = \frac{(1.6 \text{ k}\Omega)(20 \text{ V})}{R_1 + 1.6 \text{ k}\Omega}$$

$$2.7 R_1 + 4.32 \text{ k}\Omega = 32 \text{ k}\Omega$$

$$2.7 R_1 = 27.68 \text{ k}\Omega$$

$$R_1 = 10.25 \text{ k}\Omega \quad (\text{use } 10 \text{ k}\Omega)$$

### Single Stage CE Amplifier

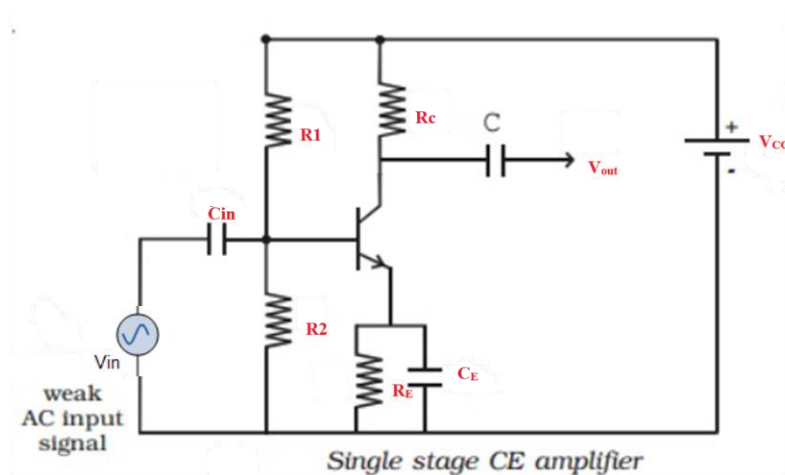


Figure shows a single stage CE amplifier. The different circuit elements and their functions are described as follows:

**(i) Biasing circuit :**

The resistances  $R_1$ ,  $R_2$  and  $R_E$  form the biasing and stabilization circuit.

**(ii) Input capacitance  $C_{in}$  :**

This is used to couple the signal to the base of the transistor.

If this is not used, the signal source resistance will come across

$R_2$  and thus changes the bias condition of the transistor.

The capacitor  $C_{in}$  allows only a.c. signal to flow.

**(iii) Emitter bypass capacitor  $C_E$  :**

This is connected in parallel with  $R_E$  to provide a low reactance path to the amplified a.c. signal. If it is not used, then amplified a.c. signal flowing through  $R_E$  will cause a voltage drop across it, thereby shifting the output voltage.

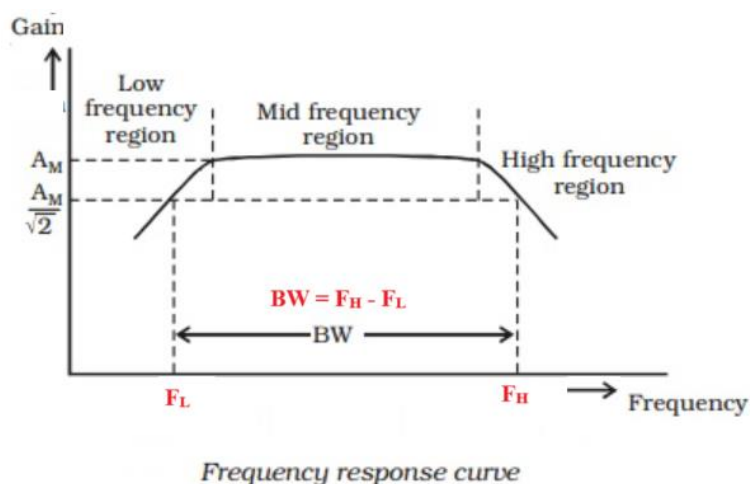
**(iv) Coupling capacitor  $C$  :**

This is used to couple the amplified signal to the output device. This capacitor  $C$  allows only a.c. signal to flow.

**Working:**

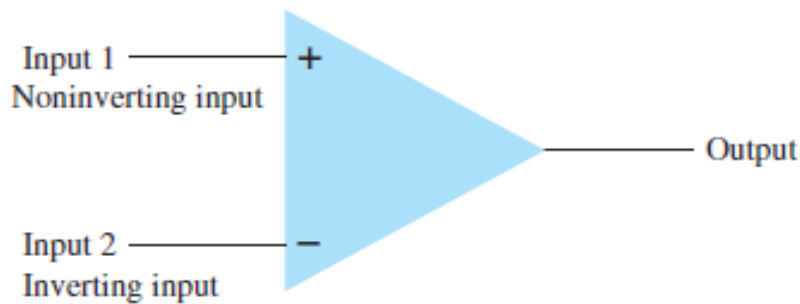
- When a weak input a.c. signal is applied to the base of the transistor, a small base current flows.
- Due to transistor action, a much larger a.c. current flows through collector load  $R_C$ , a large voltage appears across  $R_C$  and hence at the output.
- Therefore, a weak signal applied to the base appears in amplified form at the collector of circuit.
- Voltage gain ( $A_v$ ) of the amplifier is the ratio of the amplified output voltage to the input voltage.

**Frequency response and bandwidth**



## Operational Amplifier

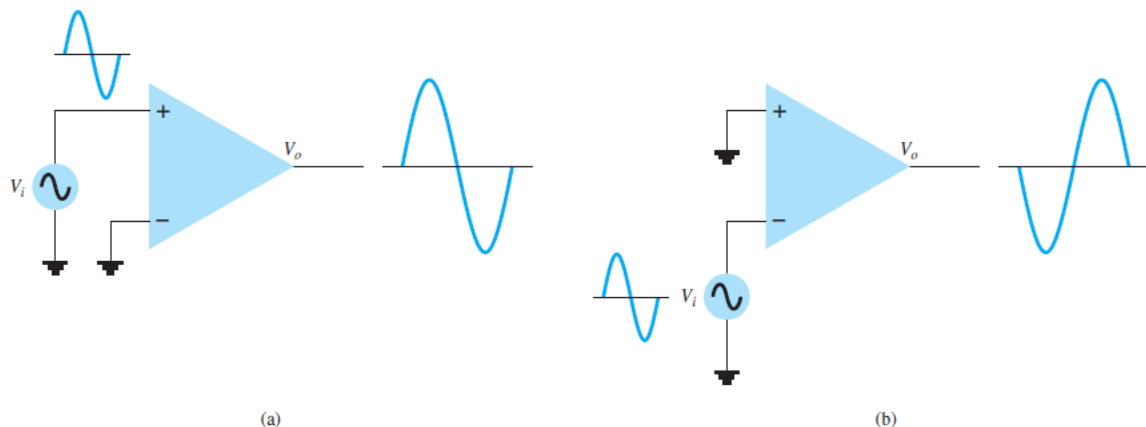
### Introduction:



**FIG. 10.1**  
*Basic op-amp.*

- ❖ Operational Amplifier or op-amp is a very high gain differential amplifier.
- ❖ It has very high input impedance. Ideally its value is infinity
- ❖ It has a low output impedance. Ideally its value is zero
- ❖ It finds applications in filters and oscillators

### Single-ended input operation:



**FIG. 10.2**  
*Single-ended operation.*

- ❖ **Single-ended input operation** results when the input signal is connected to one input with the other input connected to the ground.
- ❖ When the input signal is applied to the minus input, the output is phase-shifted by  $180^\circ$

## Double-Ended (Differential) Input

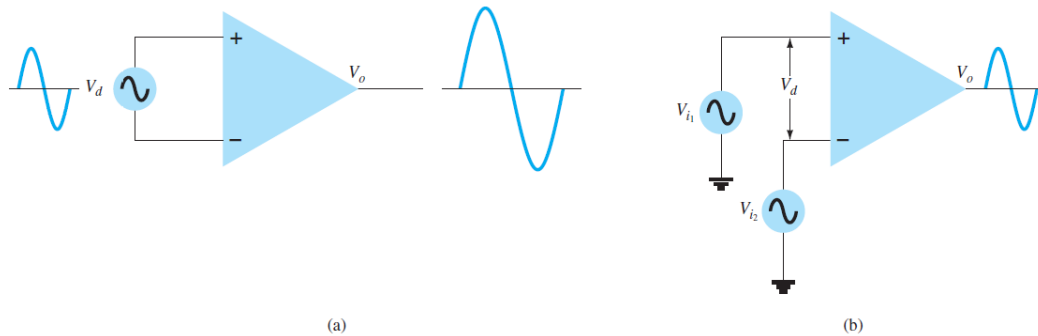


FIG. 10.3

Double-ended (differential) operation.

- ❖ Double-ended operation is shown in Fig.10.3(a) one where an input,  $V_d$  is applied between the two input terminals (recall that neither input is at ground), with the resulting amplified output in phase with that applied between the plus and minus inputs.
- ❖ Fig.10.3(b) shows the same action resulting when two separate signals are applied to the inputs, the difference signal being  $V_{i1} - V_{i2}$

## Double Ended Output:

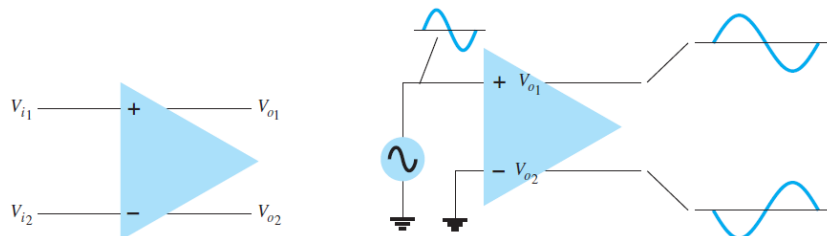


FIG. 10.4

Double-ended input with double-ended output.

FIG. 10.5

Single-ended input with double-ended output.

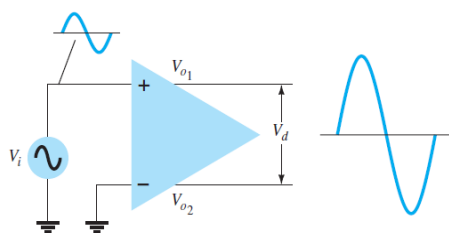


FIG. 10.6

Differential-output.

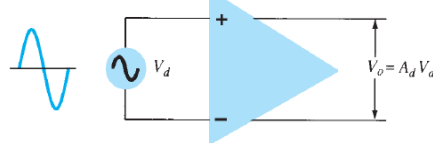


FIG. 10.7

Differential-input, differential-output operation.

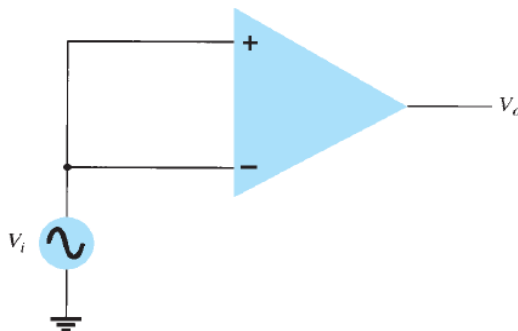
- ❖ **Double Ended Output:** An input applied to either input will result in outputs from both output terminals, these outputs always being opposite in polarity.
- ❖ Figure 10.5 shows a single-ended input with a double-ended output. As shown, the signal applied to the plus input results in two amplified outputs of opposite polarity.
- ❖ Figure 10.6 shows the same operation with a single output measured between output

terminals

This difference output signal is  $V_{o1} - V_{o2}$ . The difference output is also referred to as a *floating signal* since neither output terminal is the ground (reference) terminal. The difference output is twice as large as either  $V_{o1}$  or  $V_{o2}$  because they are of opposite polarity and subtracting them results in twice their amplitude.

- ❖ Figure 10.7 shows a differential input, differential output operation. The input is applied between the two input terminals, and the output is taken from between the two output terminals. This is a fully differential operation.

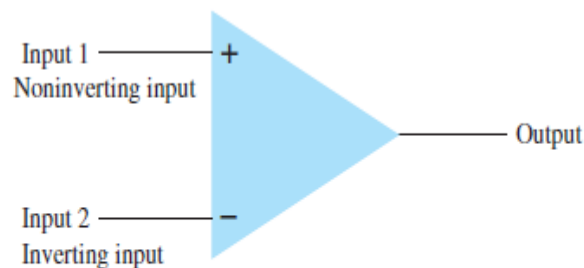
## Common Mode Operation:



**FIG. 10.8**

*Common-mode operation.*

When the same input signals are applied to both inputs, common-mode operation results, as shown in Fig. Ideally, the two inputs are equally amplified, and since they result in opposite-polarity signals at the output, these signals cancel, resulting in 0-V output. Practically, a small output signal will result.

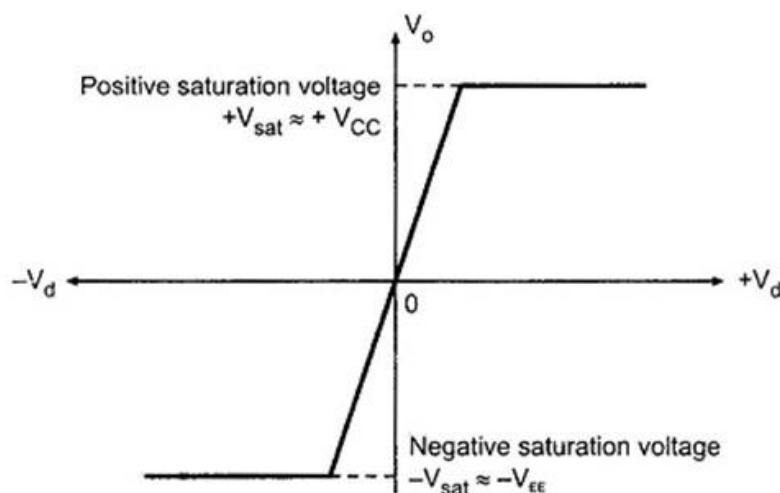


**FIG. 10.1**

*Basic op-amp.*

- ❖ Op-Amp has two inputs as shown in the figure
- ❖ Input1=Non-inverting input
- ❖ Input2= Inverting input





**Ideal voltage transfer curve**

- ❖  $V_d$  = Differential Voltage
- ❖  $+V_{sat}$  = +Ve Saturation Voltage
- ❖  $-V_{sat}$  = - Ve Saturation Voltage

It rises linearly between  $+V_{sat}$  and  $-V_{sat}$

### Op-Amp Parameters

**Input Offset Voltage:** The **input offset voltage** is the differential DC voltage that must be applied between the input terminals (inverting and non-inverting) of the op-amp to make the output voltage zero. Ideally its value is 0v. Its value is 1 mv to 6mv for 741.

**Output offset voltage :** The **output offset voltage** operational amplifier refers to the small DC voltage that appears at its output even when the input terminals are shorted together and no input signal is applied. This offset is caused by internal mismatches in the op-amp, such as differences in the transistor parameters or imbalances in the internal circuitry. Ideally its value is 0v.

**Input Resistance:** The **input resistance** of an operational amplifier (op-amp) refers to the effective resistance seen at its input terminals. It is generally measured in open-loop condition. Ideally its value is infinity. Its value of 2M ohms for 741 under open loop condition

**Output resistance:** The **output resistance** of the operational amplifier is the resistance seen at the output terminal when the op-amp is configured in an open-loop condition. Ideally, its value is 0 ohm. Its value is 75 ohms for 741.

**Gain Bandwidth:** The frequency at which the gain drops by 3 dB is known as the cutoff frequency  $f_c$  of the Op-Amp. The unity-gain frequency  $f_1$  and cutoff frequency are related by

$$f_1 = A_{VD} f_c$$

Unity-gain frequency may also be called the gain-bandwidth product of the op-amp. Ideally its value is infinity. Its value is 1MHz for 741

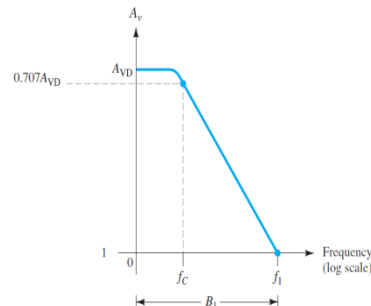


FIG. 10.47

Gain versus frequency plot.

**Slew rate:** The maximum rate at which amplifier output can change in volts per microsecond is known as **Slew rate**. The slew rate provides a parameter specifying the maximum rate of change of the output voltage when driven by a large step-input signal. Ideal value of slew rate is infinity. It is 0.5 V/ $\mu$  seconds for 741

$$SR = \frac{\Delta V_o}{\Delta t} \text{ V}/\mu\text{s} \quad \text{with } t \text{ in } \mu\text{s}$$

**Common Mode Rejection Ratio:** It is the ratio of differential gain to the common mode gain of the amplifier. Ideally CMRR is infinity. Typically its value is 90 dB for 741.

$$CMRR = \frac{A_d}{A_c}$$

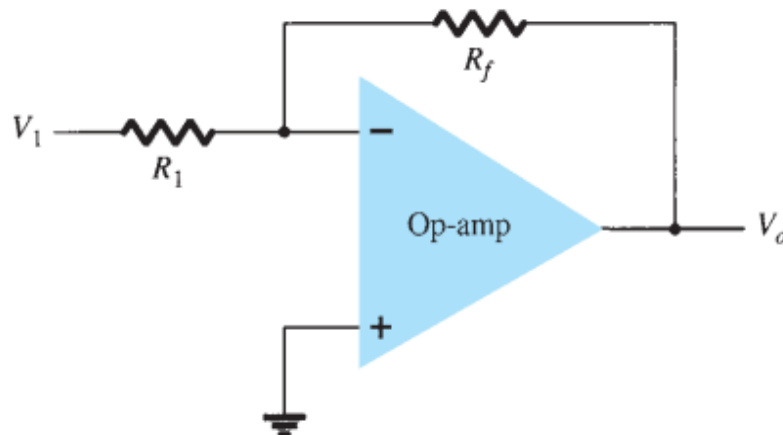
Where  $A_d$  = Differential gain of the amplifier

$A_c$  = Common mode gain of the amplifier

The value of CMRR can also be expressed in logarithmic terms

$$CMRR(\log) = 20 \log_{10} \left\{ \frac{A_d}{A_c} \right\} \text{ dB}$$

**Virtual Ground Concept:**



The output voltage is limited by the supply voltage of, typically, a few volts. As stated before, voltage gains are very high. If, for example,  $V_o = -10\text{ V}$  and  $A_v = 20,000$ , the input voltage is

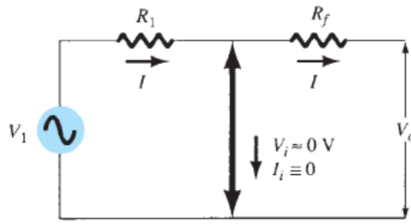
$$V_1 = \frac{-V_o}{A_v} = \frac{10}{20000} = 0.5\text{mV}$$

If the circuit has an overall gain ( $V_o > V_1$ ) of, say, 1, the value of  $V_1$  is 10 V. Compared to all other input and output voltages, the value of  $V_i$  is then small and may be considered zero volt. Note that although  $V_i = 0\text{ V}$ , it is not exactly 0 V. (The output voltage is a few volts due to the very small input  $V_i$  times a very large gain  $A_v$ .) The fact that  $V_i = 0\text{ V}$  leads to the concept that at the amplifier input there exists a virtual short-circuit or virtual ground. The concept of a virtual short implies that although the voltage is nearly 0 V, there is no current through the amplifier input to ground. Below figure depicts the virtual ground concept. The heavy line is used to indicate that we may consider that a short exists with  $V_i$  approximately equal to 0 V but that this is a virtual short so that no current goes through the short to ground. Current goes only through resistors  $R_1$  and  $R_f$  as shown. Using the virtual ground concept, we can write equations for the current  $I$  as follows:

$$I = \frac{V_1}{R_1} = -\frac{V_o}{R_f}$$

Which can be solved for

$$\frac{V_o}{V_1} = -\frac{R_f}{R_1}$$

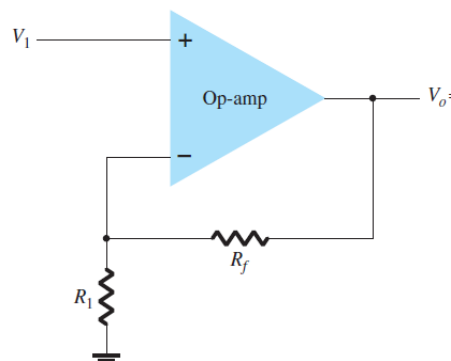


Virtual ground in an op-amp.

1) **Problem:**

Calculate the output voltage of a noninverting amplifier shown in figure

**Solution:**

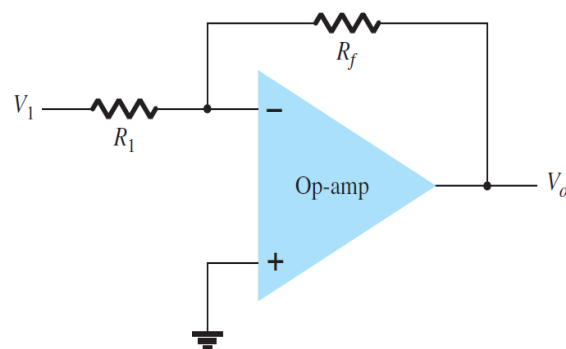


$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_1 = \left(1 + \frac{500 \text{ k}\Omega}{100 \text{ k}\Omega}\right) (2 \text{ V}) = 6(2 \text{ V}) = +12 \text{ V}$$

2) **Problem:**

If the circuit of the figure has  $R_1=100\text{K}$  Ohms and  $R_f=500\text{K}$  Ohms, What is the output voltage if  $V_1=2\text{V}$ ?

**Solution:**



$$V_o = -\frac{R_f}{R_1} V_1 = -\frac{500 \text{ k}\Omega}{100 \text{ k}\Omega} (2 \text{ V}) = -10 \text{ V}$$

3) **Problem:**

What is the Output voltage in the Circuit shown in Figure?

**Solution:**

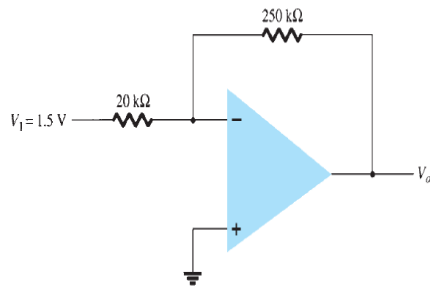


FIG. 10.62

$$V_o = -\frac{R_F}{R_1} V_1 = -\frac{250 \text{ k}\Omega}{20 \text{ k}\Omega} (1.5 \text{ V}) = -18.75 \text{ V}$$

**4) Problem**

What is the range of voltage gain adjustment in the circuit of the figure shown

**Solution:**

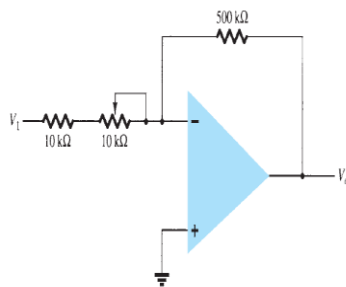


FIG. 10.63

$$A_v = \frac{V_o}{V_i} = -\frac{R_F}{R_1}$$

For  $R_1 = 10 \text{ k}\Omega$ :

$$A_v = -\frac{500 \text{ k}\Omega}{10 \text{ k}\Omega} = -50$$

For  $R_1 = 20 \text{ k}\Omega$ :

$$A_v = -\frac{500 \text{ k}\Omega}{20 \text{ k}\Omega} = -25$$

**5) Problem:**

**Solution:**

What is the input voltage that results in an output of 2V in circuit shown in Figure

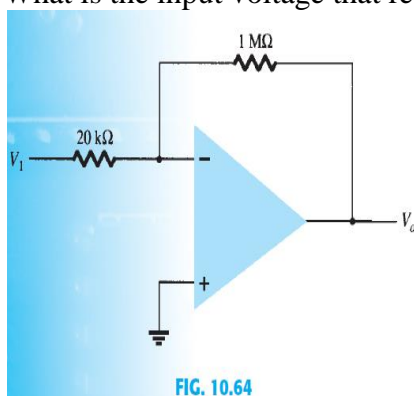


FIG. 10.64

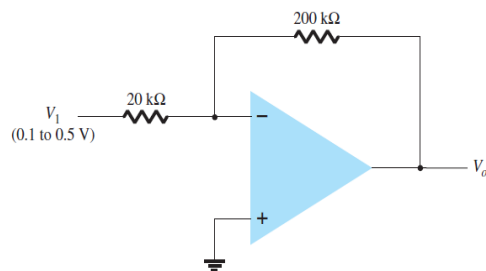
$$V_o = -\frac{R_f}{R_1} V_1 = -\left(\frac{1 \text{ M}\Omega}{20 \text{ k}\Omega}\right) V_1 = 2 \text{ V}$$

$$V_1 = \frac{2 \text{ V}}{-50} = -40 \text{ mV}$$

**6) Problem:**

What is the range of output voltage in the circuit shown in the figure if the input can vary from 0.1 to 0.5 V?

**Solution:**



**FIG. 10.65**

$$V_o = -\frac{R_F}{R_1} V_1 = -\frac{200 \text{ k}\Omega}{20 \text{ k}\Omega} V_1 = -10 V_1$$

For  $V_1 = 0.1 \text{ V}$ :

$$V_o = -10(0.1 \text{ V}) = -1 \text{ V}$$

For  $V_1 = 0.5 \text{ V}$ :

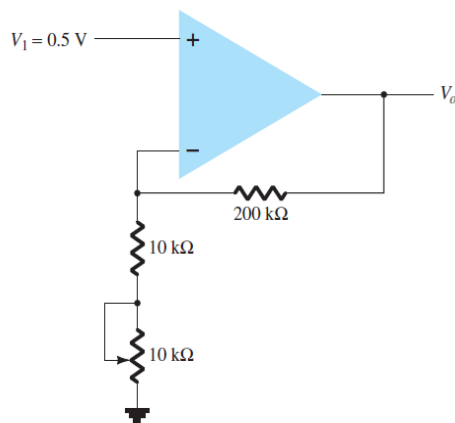
$$V_o = -10(0.5 \text{ V}) = -5 \text{ V}$$

$V_o$  ranges from  
-1 V to -5 V

**7) Problem:**

What is the range of output voltage developed in the circuit shown in the figure

**Solution:**



**FIG. 10.67**  
Problem 7.

$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_1$$

For  $R_1 = 10 \text{ k}\Omega$ :

$$V_o = \left(1 + \frac{200 \text{ k}\Omega}{10 \text{ k}\Omega}\right) (0.5 \text{ V}) = 21(0.5 \text{ V}) = 10.5 \text{ V}$$

For  $R_1 = 20 \text{ k}\Omega$ :

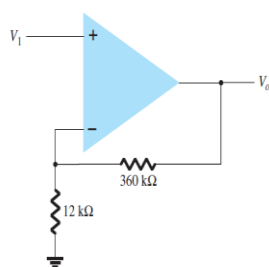
$$V_o = \left(1 + \frac{200 \text{ k}\Omega}{20 \text{ k}\Omega}\right) (0.5 \text{ V}) = 11(0.5 \text{ V}) = 5.5 \text{ V}$$

$V_o$  ranges from 5.5 V to 10.5 V.

**8) Problem:**

What is the results in the circuit shown if the input for an input of  $V_1 = -0.3 \text{ V}$ ?

**Solution:**



**FIG. 10.66**

$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_1 = \left(1 + \frac{360 \text{ k}\Omega}{12 \text{ k}\Omega}\right) (-0.3 \text{ V})$$

$$= 31(-0.3 \text{ V}) = -9.3 \text{ V}$$

**9) Problem:**

What input must be applied to the input of the circuit shown in the figure to result in an output of 2.4 V?

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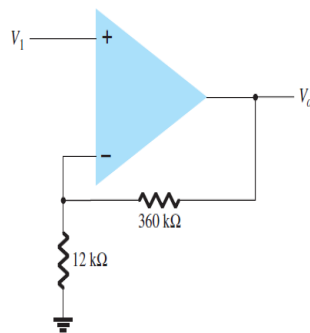


FIG. 10.66

$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_1 = \left(1 + \frac{360 \text{ k}\Omega}{12 \text{ k}\Omega}\right) V_1 = 2.4 \text{ V}$$

$$V_1 = \frac{2.4 \text{ V}}{31} = 77.42 \text{ mV}$$

**10) Problem**

What output voltage results in the circuit shown in the figure for  $V_1 = +0.5\text{V}$ ?

**Solution:**

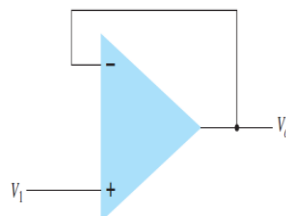


FIG. 10.70

$$V_o = V_1 = +0.5 \text{ V}$$

**11) Problem**

Calculate the output voltage of a non-inverting amplifier for values of  $V_1 = 2\text{V}$ ,  $R_f = 500 \text{ k}$ , and  $R_1 = 100\text{k}$ .

**Solution:**

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_1 = \left(1 + \frac{500 \text{ k}\Omega}{100 \text{ k}\Omega}\right) (2 \text{ V}) = 6(2 \text{ V}) = +12 \text{ V}$$

**12) Problem:**

Calculate the output voltage of an op-amp summing amplifier for the following sets of voltages and resistors. Use  $R_f = 1 \text{ M}$  in all cases.

- $V_1 = +1 \text{ V}$ ,  $V_2 = +2 \text{ V}$ ,  $V_3 = +3 \text{ V}$ ,  $R_1 = 500 \text{ k}$ ,  $R_2 = 1 \text{ M}$ ,  $R_3 = 1 \text{ M}$ .
- $V_1 = -2 \text{ V}$ ,  $V_2 = +3 \text{ V}$ ,  $V_3 = +1 \text{ V}$ ,  $R_1 = 200 \text{ k}$ ,  $R_2 = 500 \text{ k}$ ,  $R_3 = 1 \text{ M}$ .

**Solution:**

Using Summing Amplifier Equation

$$a. V_o = - \left[ \frac{1000 \text{ k}\Omega}{500 \text{ k}\Omega} (+1 \text{ V}) + \frac{1000 \text{ k}\Omega}{1000 \text{ k}\Omega} (+2 \text{ V}) + \frac{1000 \text{ k}\Omega}{1000 \text{ k}\Omega} (+3 \text{ V}) \right]$$

$$= -[2(1 \text{ V}) + 1(2 \text{ V}) + 1(3 \text{ V})] = -7 \text{ V}$$

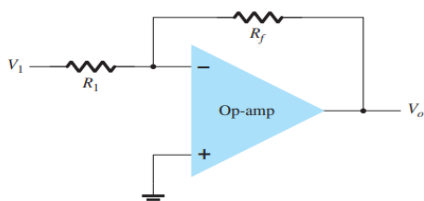
$$b. V_o = - \left[ \frac{1000 \text{ k}\Omega}{200 \text{ k}\Omega} (-2 \text{ V}) + \frac{1000 \text{ k}\Omega}{500 \text{ k}\Omega} (+3 \text{ V}) + \frac{1000 \text{ k}\Omega}{1000 \text{ k}\Omega} (+1 \text{ V}) \right]$$

$$= -[5(-2 \text{ V}) + 2(3 \text{ V}) + 1(1 \text{ V})] = +3 \text{ V}$$

**13) Problem:**

For the circuit shown,  $R_1 = 100 \text{ k}$  and  $R_f = 500 \text{ k}$ , what output voltage results for an input of  $V_1 = 2 \text{ V}$ ?

**Solution:**

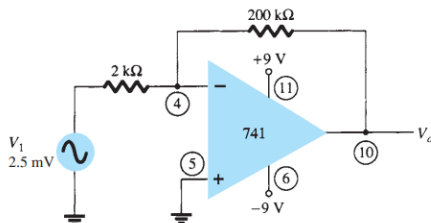


$$V_o = -\frac{R_f}{R_1} V_1 = -\frac{500 \text{ k}\Omega}{100 \text{ k}\Omega} (2 \text{ V}) = -10 \text{ V}$$

**14) Problem:**

Determine the output voltage for the circuit of Fig with a sinusoidal input of  $2.5 \text{ mV}$ .

**Solution:**



$$A = -\frac{R_f}{R_1} = -\frac{200 \text{ k}\Omega}{2 \text{ k}\Omega} = -100$$

The output voltage is then

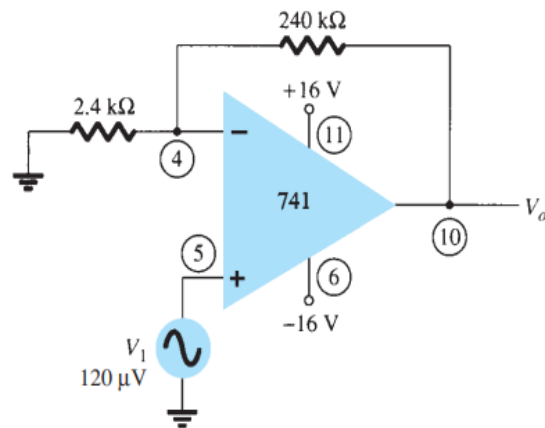
$$V_o = AV_i = -100(2.5 \text{ mV}) = -250 \text{ mV} = -0.25 \text{ V}$$

**15) Problem:**

Calculate the output voltage from the circuit of Fig for an input of  $120 \text{ mV}$ .

**Solution:**





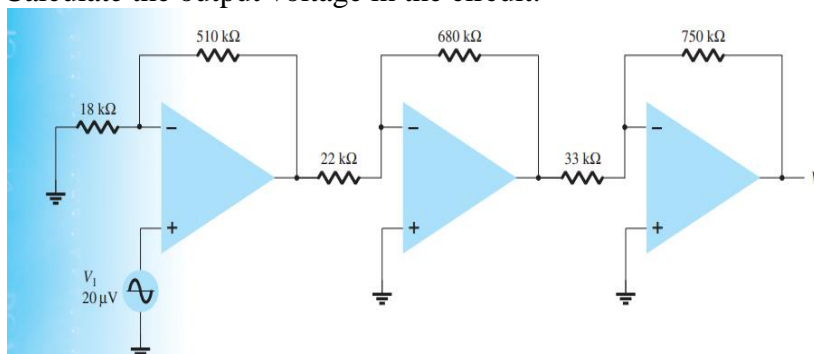
$$A = 1 + \frac{R_f}{R_1} = 1 + \frac{240 \text{ k}\Omega}{2.4 \text{ k}\Omega} = 1 + 100 = 101$$

The output voltage is then

$$V_o = AV_i = 101(120 \mu\text{V}) = \mathbf{12.12 \text{ mV}}$$

**16) Problem:**

Calculate the output voltage in the circuit.



**Solution:**

$$\begin{aligned} V_o &= \left(1 + \frac{510 \text{ k}\Omega}{18 \text{ k}\Omega}\right)(20 \mu\text{V}) \left[-\frac{680 \text{ k}\Omega}{22 \text{ k}\Omega}\right] \left[-\frac{750 \text{ k}\Omega}{33 \text{ k}\Omega}\right] \\ &= (29.33)(-30.91)(-22.73)(20 \mu\text{V}) \\ &= \mathbf{412 \text{ mV}} \end{aligned}$$

### Negative Feedback Amplifier

An op-amp with negative feedback is called feedback amplifier or closed loop amplifier.

There are 4 types of feedback configuration, and the most commonly used configurations are:

1. Voltage series (NON- INVERTING FEEDBACK AMPLIFIER) and
2. Voltage shunt. (INVERTING FEEDBACK AMPLIFIER)

### VIRTUAL GROUND AND VIRTUAL SHORT:

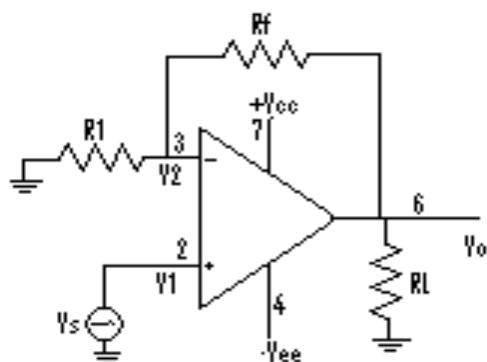
- ✓ We have  $A = (V_o/V_{id})$  or  $V_{id} = (V_o/A)$   
 Since  $A$  is very large  $V_{id} \approx 0$  i.e.  $V_1 - V_2 = 0$  or  $V_1 = V_2$   
 Therefore the voltages at the inv. and non inv. terminal are equal which implies a Virtual Short between the two input terminals.
- ✓ If in the inverting configuration the non inverting terminal is grounded, i.e.  $V_1 = 0$ . But since  $V_1 = V_2$  it implies the voltage at the inverting terminal is also zero. Thus known as Virtual Gnd.

### Basic properties of an op-amp:

1. Op-amp input terminal draws no current because of high input resistance.
2. Due to high open loop gain the voltage across op-amp input terminal is zero i.e. inv. terminal voltage equal to voltage at non inv. terminal.
3. In the inv. configuration the inverting input terminal is at virtual ground.

### VOLTAGE SERIES FEEDBACK OR NON- INVERTING FEEDBACK AMPLIFIER:

Input is applied to the non inverting terminal



### **DERIVATION of Voltage gain: ( $A_f$ ):**

From the above figures;

$V_1 = V_s$  (Voltage between non inv. terminal and GND)

$V_2 = V_f$  (Voltage between inv. terminal and GND)

But  $V_f = V_2 = V_s$ .

Current through  $R_1$ ,  $I = V_s / R_1$ .

$V_o$  = voltage drop across  $R_f$  and drop across  $R_1$

Since op-amp input terminal do not draw current due to high input impedance, the current through  $R_1$  and  $R_f$  will be same.

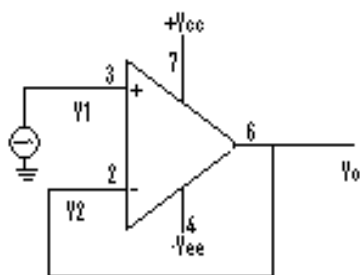
$$V_o = IR_1 + IR_f = V_s + (V_s/R_1) \cdot R_f$$

Therefore,  $A_f = V_o / V_s = 1 + (R_f/R_1)$ .

Gain of the amplifier is dependent on the ratio of the two resistors  $R_1$  and  $R_f$ .

### UNITY GAIN OR VOLTAGE FOLLOWER:

The main application of the non inverting amplifier is unity gain buffer. The circuit is as shown below:



Here  $R_f$  is short and  $R_1$  is open.

$$A_f = 1 + (R_f/R_1) = 1$$

$$A_f = (V_o/V_s) = 1$$

$$V_o = V_s$$

This means that output voltage is equal and in phase with input voltage and in this ckt  $\beta = 1$ .

### INPUT RESISTANCE:

$$R_{if} = (1 + A\beta)R_i$$

$$\beta = 1 \text{ and } 1 + A \approx 1$$

$$\text{Thus } R_{if} = AR_i$$

Similarly,

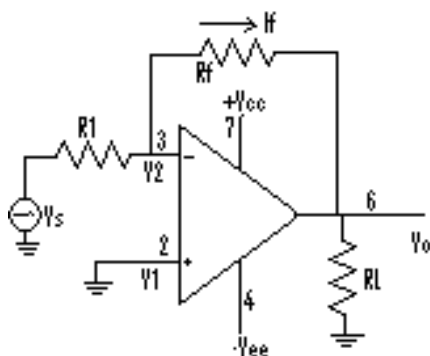
### OUTPUT RESISTANCE:

$$R_{of} = R_o / (1 + A\beta)$$

$$R_{of} = R_o / A$$

Since input resistance is very high and output resistance is very low, this ckt is used as a buffer ckt between a high resistance source and a low resistance load.

### VOLTAGE SHUNT FEEDBACK OR INVERTING AMPLIFIER WITH FEEDBACK:



The input terminal is connected to the inverting terminal through the resistor  $R_1$ . The amplified as well as inverted output is also applied to the inverting input via the feedback resistor  $R_f$ . This ckt is a negative feedback ckt because any increase in the input signal results in a feedback to the inverting input, reducing the output signal.

#### VOLTAGE GAIN:

Applying KCL at node 2

We get  $i_s = i_f + i$

Since input resistance is very high  $i$  is very low and thus  $i_s = i_f$

$$(V_s - V_2)/R_1 = (V_2 - V_0)/R_f \rightarrow 1$$

$$V_2 = 0$$

Thus finally we get

$$A_f = - (R_f/R_1)$$

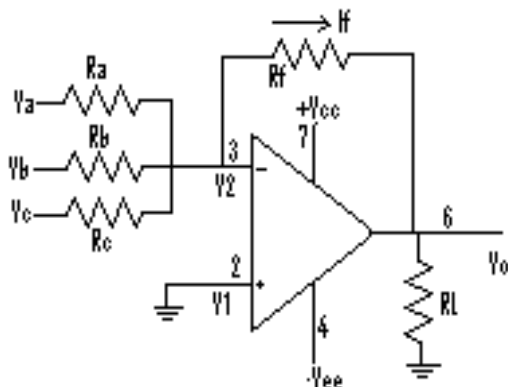
#### APPLICATIONS OF INVERTING AMPLIFIER:

##### ➤ INVERTER OR SIGN CHANGER:

$A_f = -(R_f/R_1)$  if  $R_f = R_1$  then we get  $A_f = -1$  then  $V_0 = -V_s$

Thus output is equal in magnitude but opposite in phase with the input voltage, thus acts as an inverter. If 2 stages are connected in cascade, then the output from second stage equals the input at the first stage without any change in sign.

##### SUMMER (INVERTING CONFIGURATION):



$V_a, V_b, V_c$  are the 3 inputs to inverting terminal through resistor  $R_a, R_b$  and  $R_c$ .

Applying KCL at node  $V_2$

$$I_a + I_b + I_c = I_f$$

$$(V_a/R_a) + (V_b/R_b) + (V_c/R_c) = - (V_0/R_f)$$

$$V_0 = -R_f \{ (V_a/R_a) + (V_b/R_b) + (V_c/R_c) \}$$

$$\text{If } R_a = R_b = R_c = R_f$$

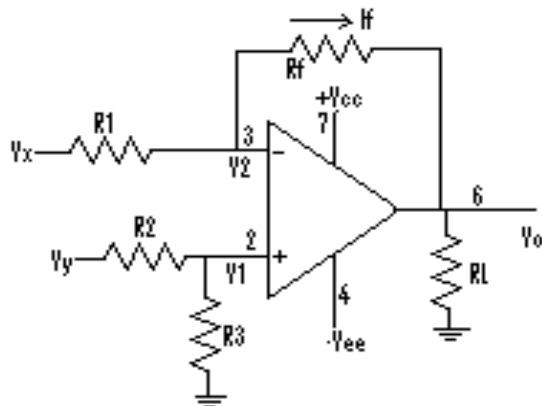
$$V_0 = V_a + V_b + V_c$$

$$\text{If } R_a = R_b = R_c = R$$

Then  $(R_f/R) = (1/N)$  where N are the no. of inputs.

Thus  $V_0 = (V_a + V_b + V_c)/3$ . Thus it is an averaging amplifier.

#### SUBTRACTOR (INVERTING CONFIGURATION):



The circuit has 2 inputs  $V_x$  and  $V_y$  applied to non inv. and inv. respectively.

Using super position theorem the output voltage  $V_o$  is

Due to  $V_y$ :

$$V_{oy} = - (R_f/R_1) V_y \rightarrow 1$$

$$V_{ox} = \{ 1 + (R_f/R_1) \} V_1$$

$$\text{But } V_1 = V_x R_3 / (R_2 + R_3)$$

$$\text{Therefore } V_{ox} = \{ R_3 / (R_2 + R_3) \} \{ 1 + (R_f/R_1) \} V_x$$

$$\text{Let } R_2 = R_1 \text{ and } R_f = R_3$$

$$V_{ox} = V_x (R_f/R_1) \rightarrow 2$$

$$\text{The total voltage } V_o = V_{ox} + V_{oy}$$

From 1 & 2,

$$V_o = (V_x - V_y) (R_f/R_1)$$

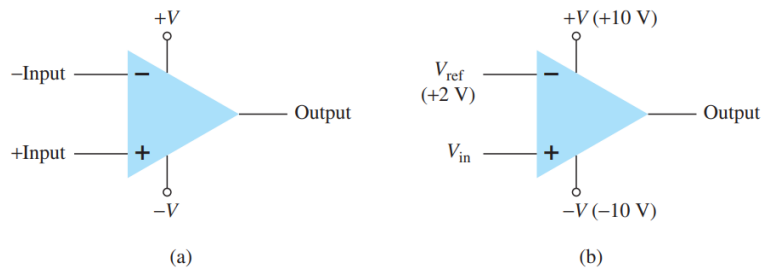
$$\text{If } R_f = R_1 \text{ then } V_o = (V_x - V_y)$$

Output voltage is equal to voltage at (non inv.) minus (inv.) terminal.

#### **Comparator**

A comparator circuit accepts input of linear voltages and provides a digital output that indicates when one input is less than or greater than the second.

A basic comparator circuit can be represented as in Fig. 13.1. since the input voltage is applied to the Non-inverting terminal and the known positive reference voltage is applied to the inverting terminal, the circuit is called as Non-inverting comparator with positive reference voltage.



**FIG. 13.1**

*Comparator unit: (a) basic unit; (b) typical application.*

The output is a digital signal that stays at a high voltage level ( $+V_{sat}$ ) when the noninverting (+) input is greater than the voltage at the inverting (-) input and switches to a lower voltage level ( $-V_{sat}$ ) when the noninverting input voltage goes below the inverting input voltage. Figure 13.1 b shows a typical connection with one input (the inverting input in this example) connected to a reference voltage of 2 V, the non-inverting input terminal connected as the input signal voltage. As long as  $V_{in}$  is less than the reference voltage level of 2 V, the output remains at a low voltage level (near -10 V). When the input rises just above 2 V, the output quickly switches to a high-voltage level (near 10 V). Thus the high output indicates that the input signal is greater than 2 V

**Zero crossing detector:** if the reference voltage is Zero, then it is called zero crossing detector and the circuit and waveforms is as shown in the figure below.

