PES UNIVERSITY
Dept of Electronics and Communication Engineering

UE25EC141A - Electronic Principles and Devices (4-0-0-4-4)
Unit3: Transistors and Operational Amplifier

1) Obtain the relationship between α and β

Ans: A relationship can be developed between α and β using basic relationship.

$$I_E = I_C + I_B$$

We know that $I_C / \alpha = I_E$ and $I_C / \beta = I_B$. Using this relation in the above equation we get

$$I_C / \alpha = I_C + I_C / \beta$$

Dividing the above equation by I_C, we get

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

$$\alpha = \frac{\beta}{1+\beta} \quad \text{or} \quad \beta = \frac{\alpha}{(1-\alpha)}$$

2) **Write a note on effects of temperature on Q-point**

Ans: Effect of temperature on Q-point:

a) Temperature causes the device parameters like transistor current gain (β) and the transistor leakage current (I_{CEO}) to change.
b) As temperature increases, I_{CEO} increases, resulting in changing the Q-point. Thus the network design must also consider temperature stability to reduce the changes in Q-point.
c) The variation of operating point due to variation in temperature is indicated by stability factor (S). Higher the stability of the circuit, better is the circuit.

3) With mathematical interpretations explain Fixed bias Configuration.

Ans: Fixed bias Configuration is also called as simple biasing.

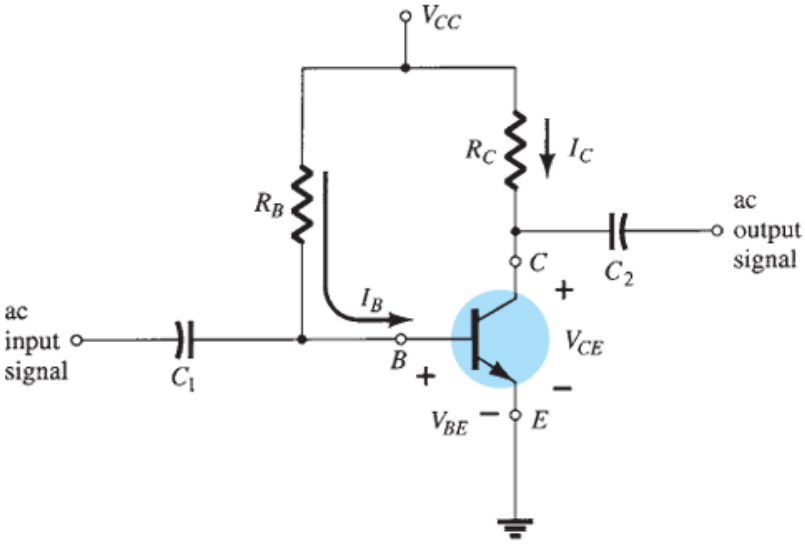


Fig: Fixed Bias Configuration Circuit

For DC, frequency f=0 and $X_C = \frac{1}{2\pi fc} = \frac{1}{2\pi 0c} = \square\wedge$.

Forward Bias of Base–Emitter:

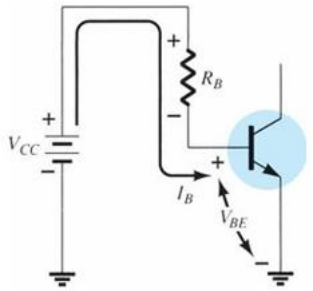


Fig: Base-Emitter Loop

$I_C = \beta * I_B$

Applying KVL to base emitter loop,

$V_{CC} - I_B R_B - V_{BE} = 0$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

The supply voltages V_{CC} and V_{BE} are constants.

The selection of a base resistor sets the level of base current for the operating point.

Collector–Emitter Loop :

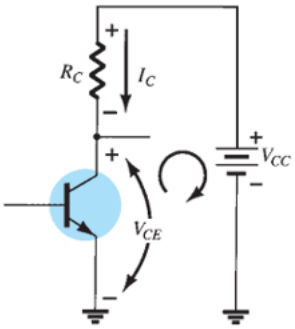


Fig: Collector-Emitter Loop

The collector–emitter section of the network appears in above figure with the indicated direction of current I_C and the resulting polarity across R_C.

$I_C = ®*I_B$

Changing RC to any level will not affect the level of IB or IC as long as the device in the active region.

The level of R_C will determine the magnitude of V_{CE}.

Applying KVL toCollector-Emitter Loop,

$V_{CE}+I_CR_C-V_{CC}=0$

$V_{CE}=V_{CC}-I_CR_C$

$V_{CE}=V_C-V_E = V_C$ (As emitter is grounded)

$V_{BE}=V_B-V_E=V_B$

4. **Explain Single Stage CE Amplifier.**

Ans:

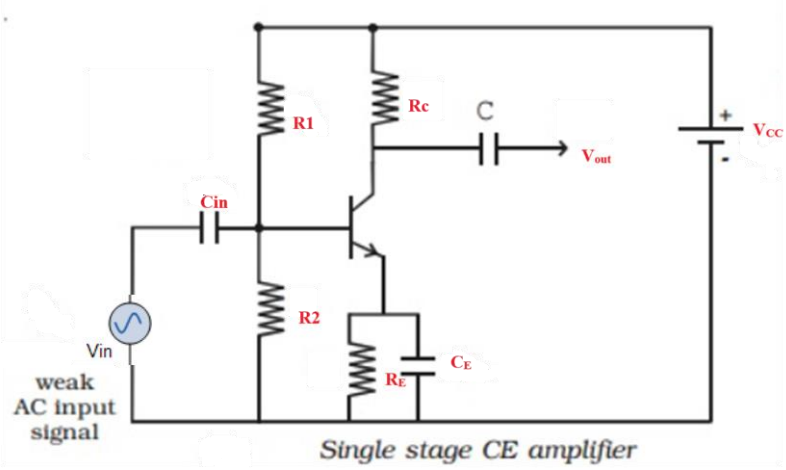


Figure shows a single stage CE amplifier. The different circuit elements and their functions are described as follows:

(i) Biasing circuit :

The resistances R_1, R_2 and R_E form the biasing and stabilization circuit.

(ii)Input capacitance C_{in} :

This is used to couple the signal to the base of the transistor.
If this is not used, the signal source resistance will come across
R_2 and thus changes the bias condition of the transistor.
The capacitor C_{in} allows only a.c. signal to flow.

(iii) Emitter bypass capacitor C_E :

This is connected in parallel with R_E to provide a low reactance path to the amplified a.c. signal. If it is not used, then amplified a.c. signal flowing through R_E will cause a voltage drop across it, thereby shifting the output voltage.

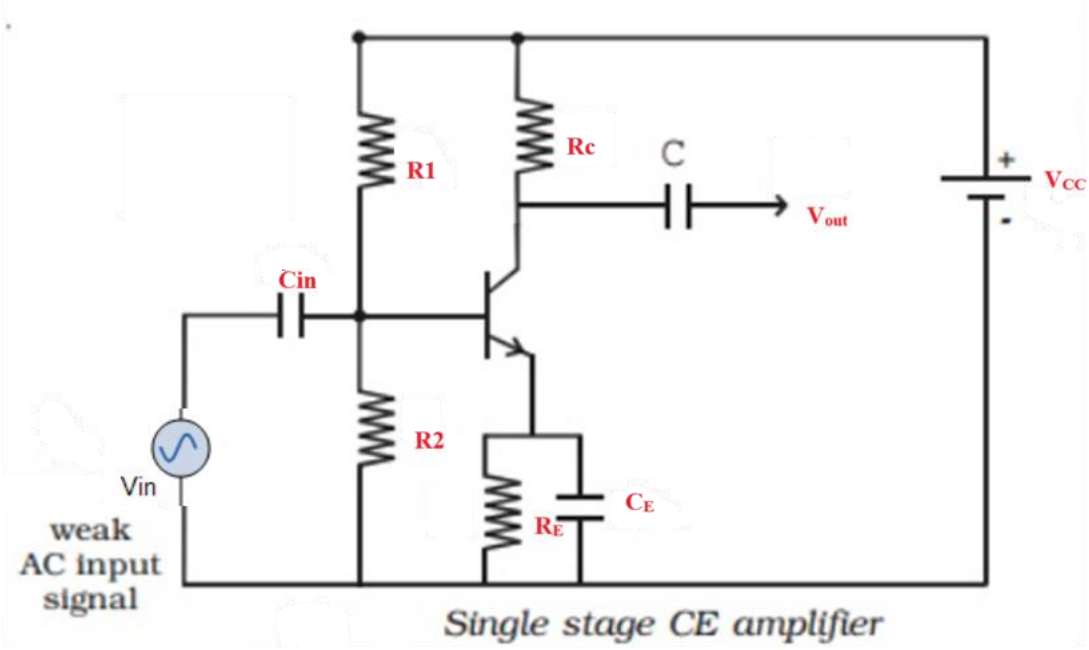
(iv)Coupling capacitor C :

This is used to couple the amplified signal to the output device. This capacitor C allows only a.c. signal to flow.

Working:

- When a weak input a.c. signal is applied to the base of the transistor, a small base current flows**.**
- Due to transistor action, a much larger a.c. current flows through collector load R_C, a large voltage appears across R_C and hence at the output.
- Therefore, a weak signal applied to the base appears in amplified form at the collector of circuit.
- Voltage gain (A_v) of the amplifier is the ratio of the amplified output voltage to the input voltage.

4) Explain Single Stage CE Amplifier.



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5) **Why biasing is required?**

Transistor Biasing:

Biasing is the process of providing DC voltage which helps in the functioning of the circuit. A transistor is based in order to make the base- emitter junction forward biased and base-collector junction reverse biased, so that it maintains in active region, to work as an amplifier.

Need for DC biasing:

If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.

- The input voltage should exceed cut-in voltage for the transistor to be ON.
- The BJT should be in the linear / active region, to be operated as an amplifier.

DC biasing:

- The operating point is a fixed point on the characteristics and is also called quiescent point, denoted by Q-point. The term biasing means the application of dc voltages used to setup a fixed level of current and voltage. Called “dc basing” or “biasing analysis”

6) With a neat diagram explain the Common Mode operation in Operational Amplifier [Op-Amp]
Answer

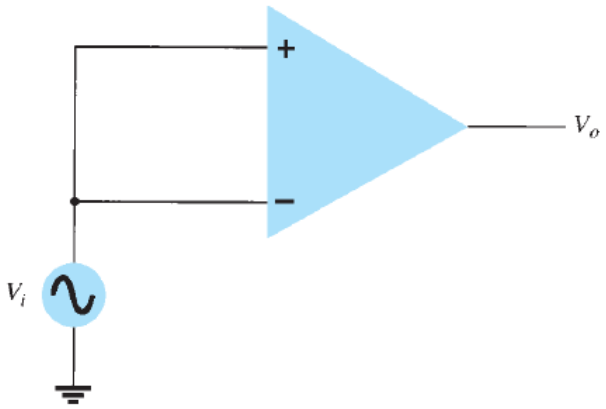


FIG. 10.8
Common-mode operation.

When the same input signal is applied to both inputs, common-mode operation results, as shown in Fig. Ideally, the two inputs are equally amplified. Since they result in opposite-polarity signals at the output, these signals cancel, resulting in 0-V output. Practically, a small output signal will result

7) Define the following with respect to Op-Amps
(i) Input offset Voltage
(ii) Output offset Voltage
(iii) Input resistance
(iv) Output resistance

Answer
Input Offset Voltage: It is the differential DC voltage that must be applied between the input terminals (inverting and non-inverting) of the op-amp to make the output voltage zero. Ideally its value is 0v. Its value is 1 mv to 6mv for IC 741.
Output offset voltage: This refers to the small DC voltage that appears at its output even when the input terminals are shorted together and no input signal is applied. This offset is caused by internal mismatches in the op-amp, such as differences in the transistor parameters or imbalances in the internal circuitry. Ideally its value is 0v.
Input Resistance: The input resistance of an op-amp refers to the effective resistance seen at its input terminals. It is generally measured in open-loop condition. Ideally its value is infinity. Its value is 2MΩ for IC 741 under open loop condition

Output resistance: The output resistance of the op-amp is the resistance seen at the output terminal when the op-amp is configured in an open-loop condition. Ideally, its value is 0. Its value is 75Ω IC 741.

8) With a neat diagram explain Gain Bandwidth
Answer:

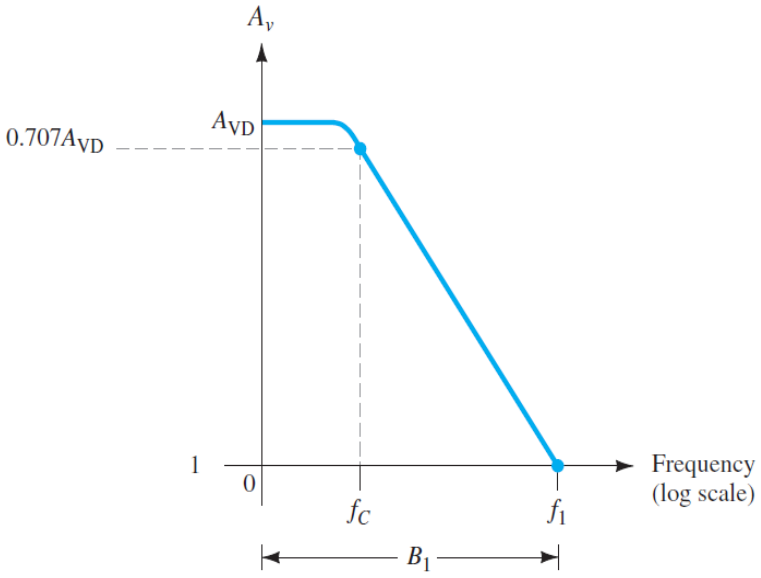


FIG. 10.47
Gain versus frequency plot.

Gain Bandwidth: The frequency at which the gain drops by 3 dB is known as the cutoff frequency f_c of the Op-Amp. The unity-gain frequency f_1 and cutoff frequency are related by

$$f_1 = A_{VD} f_c$$

Unity-gain frequency may also be called the gain–bandwidth product of the op-amp. Ideally its value is infinity. Its value is 1MHz for IC741

9) Determine the cut-off frequency of an-amp having specified values B1=1MHz, A_{VD}= 200 V/mV
Answer:

Since $f_1 = B_1 = 1$ MHz, we can use Eq. (10.23) to calculate

$$f_C = \frac{f_1}{A_{VD}} = \frac{1\text{ MHz}}{200\text{ V/mV}} = \frac{1 \times 10^6}{200 \times 10^3} = \mathbf{5\ Hz}$$

10) Define the following with respect to op-amp

(i) Slew rate
(ii) Common mode rejection ratio

Answer:

(i) **Slew rate:** The maximum rate at which amplifier output can change in volts per microsecond is known as Slew rate. The slew rate provides a parameter specifying the maximum rate of change of the output voltage when driven by a large step-input signal. Ideal value of slew rate is infinity. It is 0.5 V/μs for IC741

$$\text{SR} = \frac{\Delta V_o}{\Delta t}\ \text{V}/\mu\text{s} \quad \text{with } t \text{ in } \mu\text{s}$$

(ii)Common Mode Rejection Ratio: It is the ratio of differential gain to the common mode gain of the amplifier. Ideally, CMRR is infinity. Typically, its value is 90 dB for IC741

$$CMRR = \frac{A_d}{A_c}$$

$$A_d = Differential\ gain\ of\ the\ amplifier$$

$$A_c = Common\ mode\ gain\ of\ the\ amplifier$$

The value of CMRR can also be expressed in logarithmic terms

$$CMRR(log) = 20log_{10}\left\{\frac{A_d}{A_c}\right\}\ dB$$

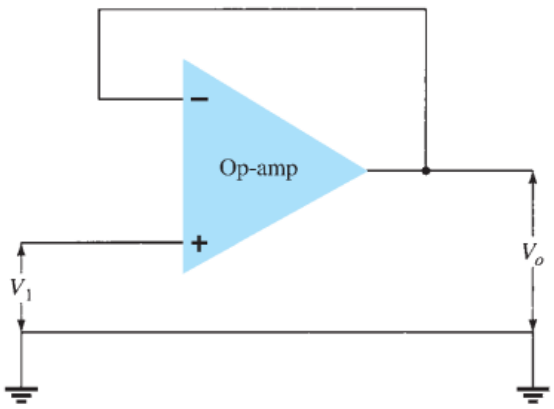
11) Why negative feedback is necessary in Op-Amps?

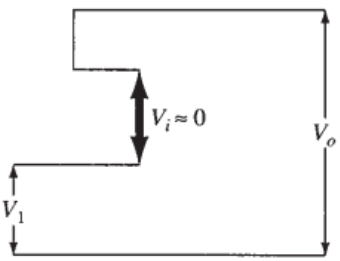
Answer:

Op-amps are normally used with negative feedback for the following reasons:

1. The open-loop gain of the op-amp is very high. It is typically 2 x10^5 for IC 741. Such large gain is unsuitable for linear applications. Negative feedback decreases the gain and makes it suitable for linear applications such as an amplifier.
2. The open-loop gain is not stable and varies with temperature, supply voltage and frequency whereas the gain with feedback is stable.
3. The open-loop BW is very small making it unsuitable for any practical application. With negative BW increases.

12) Explain unity follower or voltage follower using Op-Amp



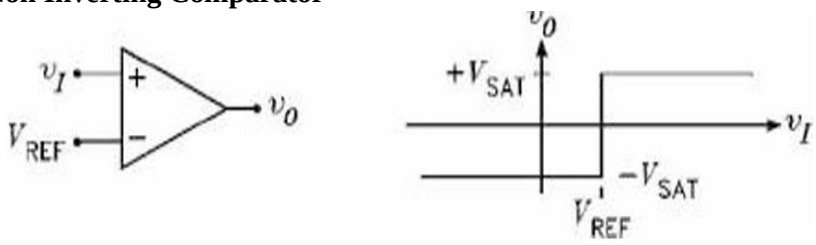


The unity-follower circuit provides a gain of unity with no polarity or phase reversal as shown in fig a. From the equivalent circuit as in fig b, Vo = V1.It has a very high input resistance and a very low output resistance. It is used as a buffer circuit for impedance matching purposes.

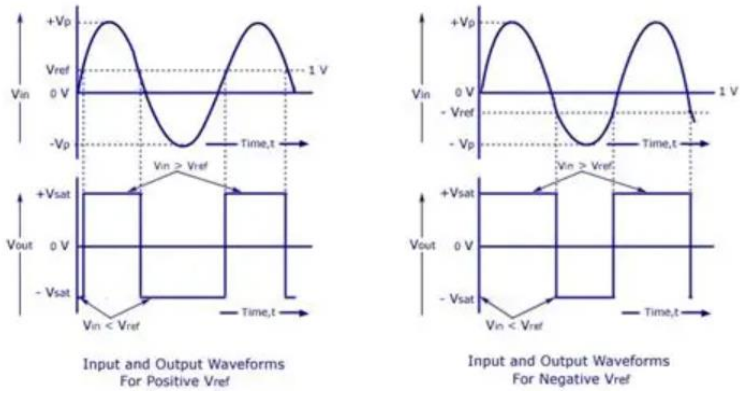
13. Define comparator. Explain the working of the Non inverting Comparator.

Solution: Comparator is an electronic circuit which compares two voltages or currents and outputs a digital signal indicating which is larger.

Non Inverting Comparator



A fixed reference voltage(Vref) is applied to inverting input and a time varying signal vi is applied to Non-inverting input.The output voltage is at –Vsat for vi< Vref and goes to +Vsat for vi>Vref.

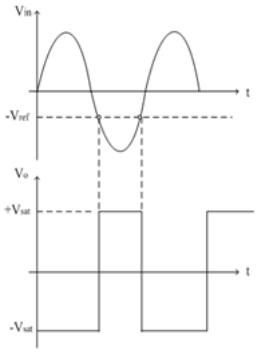


14. An instantaneous input change of 10v is applied to a unity-gain inverting amplifier. If the op-amp is 741, how long will it take for the output voltage to change by 10v?

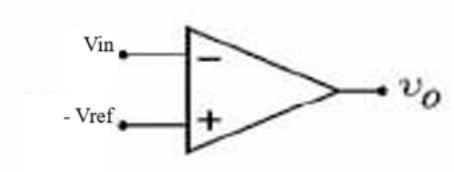
Solution:

SR = output voltage change/ time, SR of 741 is 0.5V/us.
Time = 10V / (0.5V/⌈s) = 20⌈s

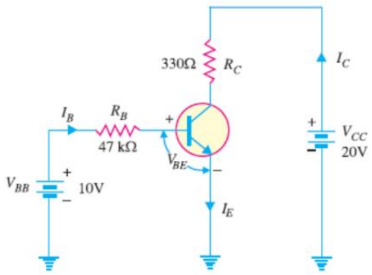
15. Identify the circuit for the given waveforms and draw the circuit diagram for the same.



Solution: Inverting Comparator with negative reference.



16. Determine the Q point of the transistor circuit shown in Fig below. Given β = 200 and V_{BE} = 0.7V.



Solution:

$$V_{BB} - I_B R_B - V_{BE} = 0$$

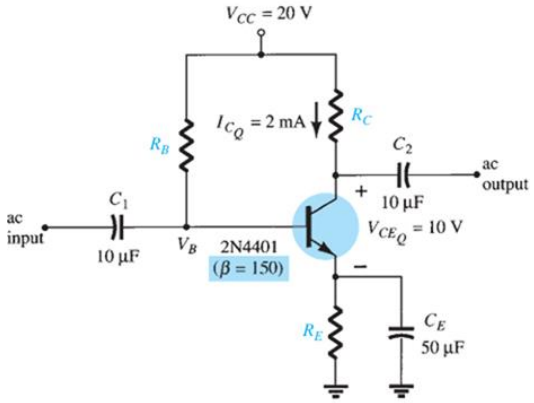
$$\therefore \quad I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10V - 0.7V}{47\,k\Omega} = 198\ \mu A$$

Now $I_C = \beta I_B = (200)(198\ \mu A) = 39.6\ mA$

Also $V_{CE} = V_{CC} - I_C R_C = 20V - (39.6mA)(330\ \Omega) = 20V - 13.07V = 6.93V$

Therefore, the Q-point is $I_C = 39.6\ mA$ and $V_{CE} = 6.93V$.

17. Determine the resistor values for the network of Fig. for the indicated operating point and supply voltage



Solution:

$$V_E = \frac{1}{10}V_{CC} = \frac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{2\text{ mA}} = \mathbf{1\,k\Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 10\text{ V} - 2\text{ V}}{2\text{ mA}} = \frac{8\text{ V}}{2\text{ mA}}$$

$$= \mathbf{4\,k\Omega}$$

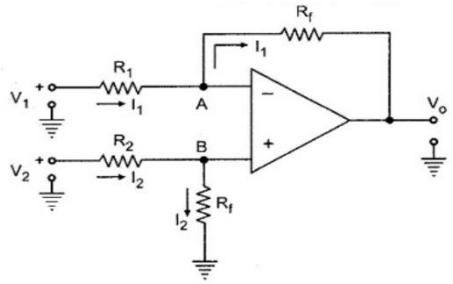
$$I_B = \frac{I_C}{\beta} = \frac{2\text{ mA}}{150} = 13.33\,\mu\text{A}$$

$$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20\text{ V} - 0.7\text{ V} - 2\text{ V}}{13.33\,\mu\text{A}}$$

$$\cong \mathbf{1.3\,M\Omega}$$

18. Explain how an Op-Amp works as subtractor.

Solution:



By applying Superposition principle

- Let V_{o1} be the output, with input V_1, assuming V_2 to be zero. And V_{o2} be the output, with input V_2 , assuming V_1 to be zero.With V_2 zero, the circuit acts as an inverting amplifier and the output equation is

$$V_{o1} = -\frac{R_f}{R_1} V_1 \quad \text{------(1)}$$

While with V_1 as zero, the circuit acts as an non-inverting amplifier.

$$V_B = \frac{R_f}{R_2 + R_f} V_2 \quad \text{-----(2)}$$

$$I = \frac{V_A}{R_1} = \frac{V_B}{R_1} \quad \text{------(3)}$$

$$I = \frac{V_{o2} - V_A}{R_f} = \frac{V_{o2} - V_B}{R_f} \quad \text{------(4)}$$

Equating the equations (3) and (4),

$$\frac{V_B}{R_1} = \frac{V_{o2} - V_B}{R_f}$$

$$V_{o2} = \frac{R_1 + R_f}{R_1} V_B$$

$$V_{o2} = \left[1 + \frac{R_f}{R_1}\right] V_B \qquad \text{-----(5)}$$

Substituting V_B from (2) in (5) we get,

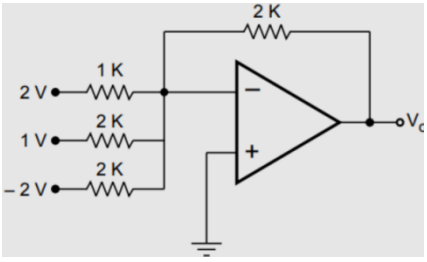
$$V_{o2} = \left[1 + \frac{R_f}{R_1}\right]\left[\frac{R_f}{R_2 + R_f}\right] V_2$$

Hence using Superposition principle,

$$V_o = V_{o1} + V_{o2}$$

$$= -\frac{R_f}{R_1} V_1 + \left[1 + \frac{R_f}{R_1}\right]\left[\frac{R_f}{R_2 + R_f}\right] V_2$$

19. Determine the output voltage for the following circuit.



Solution:

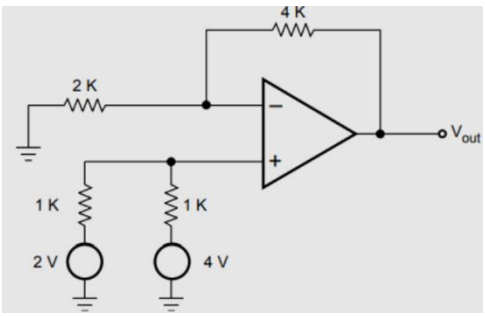
$R_f = 2\ k\Omega, \quad R_1 = 1\ k\Omega, \quad R_2 = 2\ k\Omega, \quad R_3 = 2\ k\Omega,$

$V_1 = 2\ V, \quad V_2 = 1\ V, \quad V_3 = -2\ V$

$$\therefore \quad V_o = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right]$$

$$= -\left[\frac{2}{1} \times 2 + \frac{2}{2} \times 1 + \frac{2}{2} \times (-2)\right] = -3\ V$$

20. ***Determine the output voltage for the circuit shown in Fig.***



Solution : Use Superposition principle. Consider 4 V alone, short 2 V source.

Using potential divider rule,

$$\therefore \quad V_B = \frac{4}{(1\,k\Omega + 1\,k\Omega)} \times 1\,k\Omega$$

$$= 2\ V$$

$$\therefore \quad V_{o1} = \left(1 + \frac{R_f}{R_1}\right) V_B$$

$$= \left(1 + \frac{4}{2}\right) \times 2 = \mathbf{6\ V}$$

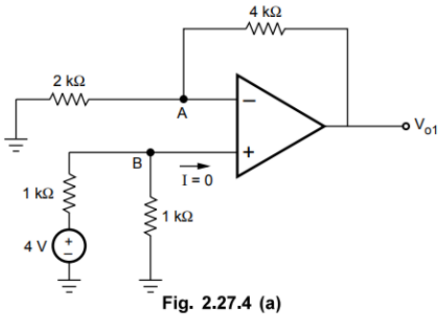


Fig. 2.27.4 (a)

Now consider 2 V source short 4 V.

$$V_B = \frac{2}{(1\,k\Omega + 1\,k\Omega)} \times 1\,k\Omega = 1\ V$$

$$\therefore \quad V_{o2} = \left(1 + \frac{R_f}{R_1}\right) V_B$$

$$= \left(1 + \frac{4}{2}\right) \times 1 = \mathbf{3\ V}$$

$$\therefore \quad V_{out} = V_{o1} + V_{o2} = \mathbf{9\ V}$$

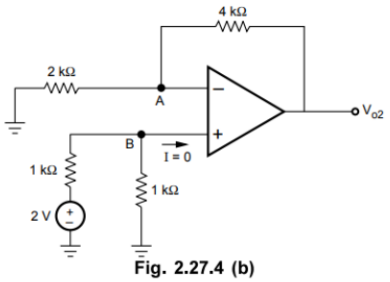


Fig. 2.27.4 (b)