COEP TECHNOLOGICAL UNIVERSITY, PUNE
Wellesly Road, Shivajinagar, Pune - 411 005

DLO - Lab 3

Aim. To study and verify a full adder using basic logic gates and design and verify a full adder using IC 7483.

$S = X'Y'Z + X'Z'Y + XYZ + XY'Z'$

Carry out (Cout) = $XY + YZ + XZ$

Theory: According to functions of a full carry adder a Cin (Carry in) with two inputs X and Y with generate a sum bit and carry out bit

Truth table

X	Y	C in	S	C-out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

From here

$$S = x'y'z + x'yz' + xyz + xy'z'$$
$$C = xy + yz + xz$$

In theory :

$$S = (x \oplus y \oplus z)$$

$$C = \cancel{x} + xy + z \cdot (x \oplus y)$$

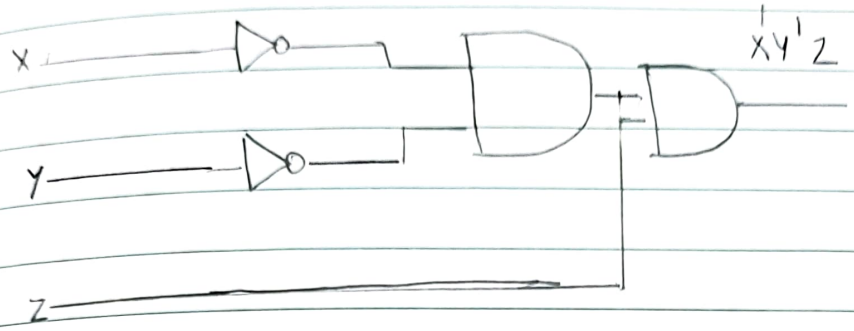
To prove S and C ~~in~~ ~~o~~ in (I) and (II) are s
as in theory.

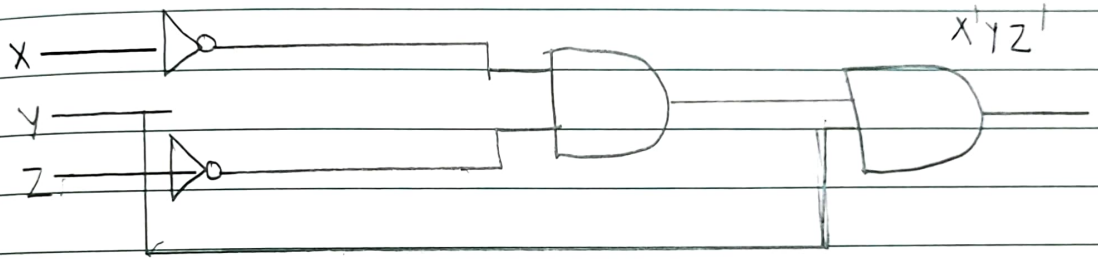
Truth table

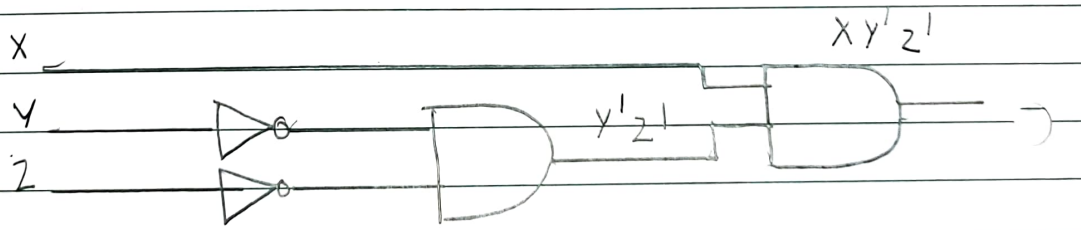
$S = x'y'z + x'yz' + xyz + xy'z'$ $\quad Cout = xy + yz + xz$

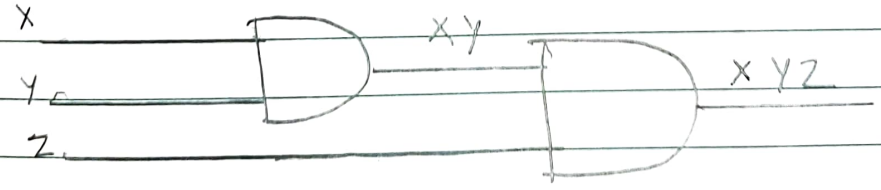
x	y	z	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

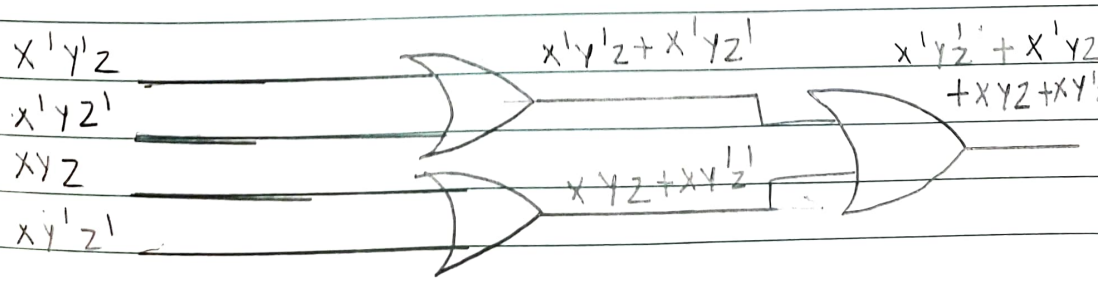
Circuit diagram



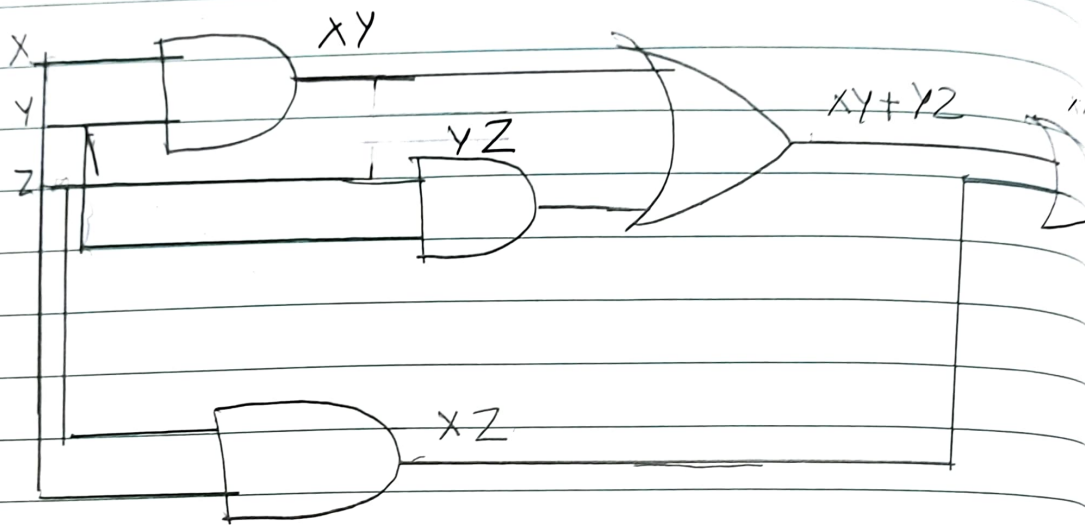








Carry



Theory

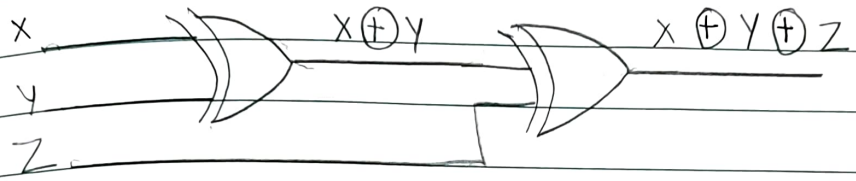
$S = X \oplus Y \oplus Z$

$C = XY + Z(X \oplus Y)$

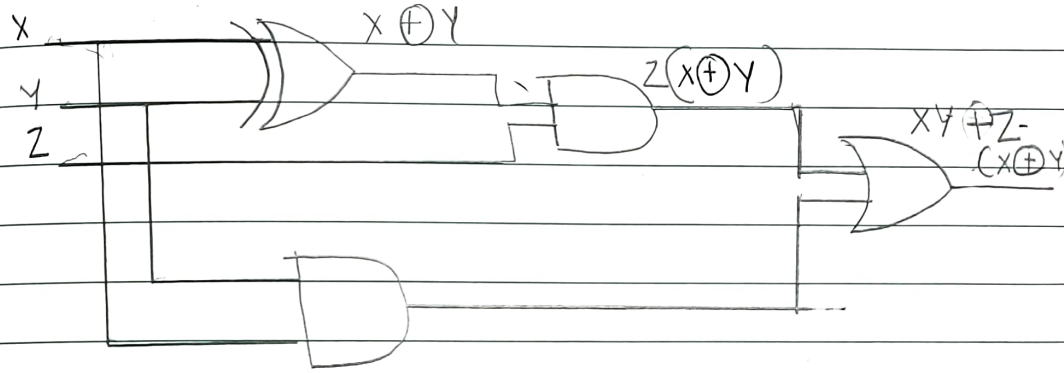
X	Y	Z	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Circuit diagram

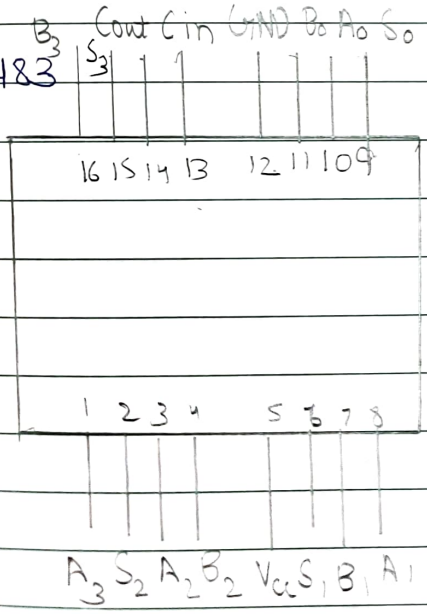
S — Sum



Carry



IC-7483



Conclusion :- Truth table of ~~Hat~~ Full adde
verified and both circuits made. Full add
designed using IC 7483 along with using ba
gates.

Date 11/10.