The internal architecture of 8085 consist of.

- ALU
- Timing and control unit
- Instruction Register & decoder
- Register set
- Interrupt control
- Serial I/O control

ALU (Arithmetic & Logic Unit)

Performs arithmetic and logical operations
Includes:

accumulator
temporary register
arithmetic & logic circuits
5 flags.

Timing and control unit-

is a section of CPU. It generates timing and control signals which are necessary for the execution of instructions. It synchronizes all microprocessor operations with the clock. It provides status control and timing signals which are required for the operation of memory and I/O devices. It controls the entire operations of the MP and peripherals connected to it.

Instruction Register and decoder

→ When an instruction is fetched from memory, it is loaded in the instruction register (IR)
→ Instruction decoder decodes the instruction and encodes into various machine cycle

Register set-

Intel 8085 µp has the following registers

i) 8 bit accumulator (A)
ii) six 8 bit general purpose registers (B, C, D, E, H, L)
iii) 16 bit stack pointer (SP)
iv) 16 bit program counter
v) Instruction register (IR)
vi) Temporary register (W & Z)
vii) Address / data buffer (MAR, MDR)
viii) Flag Register (5 flipflops)

Accumulator

It is an 8 bit register associated with ALU. It is used to hold one of the operands of an arithmetic or logical operation. Final result of an operation is placed in accumulator register.

General purpose Registers

→ contains 6 8 bit general purpose registers. They are B, C, D, E, H, L. To hold 16 bit data or address, a combination of 2 8 bit registers can be used. The combination of 2 8 bit registers is called 'Register pair' valid register pairs are B-C, D-E & H-L.
general purpose registers & accumulator are accessible to the programmer.

Stack pointer (SP)

It is a 16 bit special function register
The stack is a sequence of memory locations set aside by a programmer. Any portion of the memory can be used as stack. Stack works as LIFO principle.

Stack pointer Register (SP) holds the address of top of stack

Program Counter (PC)

16 bit special function register. It is used to hold the memory address of next instruction to be executed. So it will keep track of program execution

Instruction Register (IR)

The instruction register holds the opcode (operation code) the instruction, which is being decoded and executed. It follows FIFO principle.

Temporary Registers

These are 8 bit registers associated with ALU. It holds data during an arithmetic / logic operation. It is not accessible to the programmer.

Address Buffer (memory Address Register MAR)

It holds the addresses received from PC used for temporary storage of address.

Data buffer (memory Data Register MDR)

A register which stores data temporarily before written into memory

Flag Register of 8085

8085 up contains 5 flipflops to serve as status flags. The flipflops are set or reset according to the conditions which arise during arithmetic/logic operations.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z	X	AC	X	P	X	C

X – undefined bit

Carry Flag (C)

After the execution of an arithmetic instruction, if a carry is produced, carry flag is set to 1. carry flag holds the carry out of most significant bit (D_7) resulting from execution of an arithmetic operation

Parity Flag (P)

The parity status flag is set to 1, if the result of an arithmetic/logical operation contains EVEN number of 1's.

Eg. data byte 0000 0011 has even parity.

Auxiliary Carry Flag (AC)

In an arithmetic operation, when a carry is generated by digit D_3 and passed on to digit D_4, then the auxiliary carry flag is set. counting of bits starts from 0, and hence bit no 8 is actually 4th bit from LSB (D_0)

Zero flag (Z)

The zero flag is set to 1, if the result of an arithmetic / logic operation is zero.

Sign Flag (S)

The sign flag is set to 1, if the result of an arithmetic or logic operation is negative; if the result is positive sign flag will be zero. The sign flag has its significance

only when signed arithmetic is performed
If the number is negative, sign bit (D_7) will be 1.

PSW (Program status word)

Five flag bits indicates 5 status flags and 3 bits are undefined. The combination of these 8 bits is called PSW.

PSW and accumulator are treated as a 16 bit unit for stack pointer.

Serial I/O control

It is used for controlling serial data transmission

Interrupt control

It is used for handling interrupts, INTR, TRAP, RST7.5, RST6.5, RST5.5 are interrupt lines.

Increment-er - Decrementer address latch

It is used to make the address next required on the systems bus available to it and to increment/decrement addresses or register contents as required.