INSTRUCTION SET OF 8085

Sebry

The following notations are used in the descriptions of 8085 instructions

R - (A, B, C, D, E, H, L)
M - Memory location
R_s - Source Register
R_d - Destination Register
R_p - Register pair (BC, DE, HL)
RH - high order Register of Register pair
RL - low order Register of Register pair.
CS - carry status
[ ] - content of
PSW - program status word.
PC - Program counter
SP - stack pointer.

The 8085 instruction set is classified into the following 3 groups according to word size or byte size

1). 1 byte instruction
2) 2 - byte instruction
3) 3 - byte instruction

One byte instructions

→ includes the opcode and operand in the same byte.

	opcode	operand	Binary code	hexcode
Eg:	MOV	C, A	0100 1111	4FH.
	ADD	B	1000 000	80H.
	CMA		0010 1111	2FH

Two byte instructions

→ The first byte specifies the operation code and second byte specifies the operand.

				hex code
Eg	MVI	A, 32H	0011 1110	3E
			0011 0010	32.
	MVI	B, F2H	0000 0110	06
			1111 0010	F2.

Three byte Instructions

first byte specifies the opcode and the following 2 bytes specifies the 16bit address (second byte → low order address
third byte → higher-order address)

Eg.	LDA	2050 H	0011 1010	3A
			0101 0000	50
			0010 0000	20
	JMP	2085H.	1100 0011	C3
			1000 0101	85
			0010 0000	20

Instruction types

1. Data transfer (copy) Instruction
2. Arithmetic Instructions
3. Logical & bit manipulation instructions
4. Branching Instructions
5. Restart Instructions
6. machine control Instructions / stack, I/O Instructions

I. Data Transfer / Data copy Instructions

1. MOV Rd, Rs

Copy data from source Register R_s into destination Register Rd. R_s & Rd can be any one of the Registers A, B, C, D E, H & L.

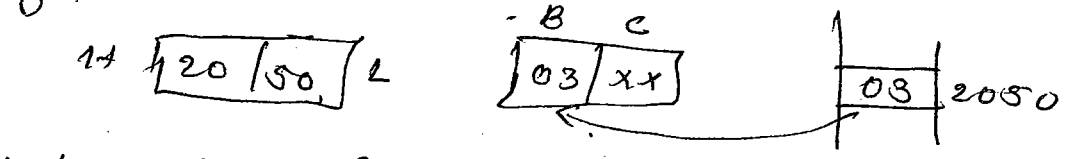
m/c cycle : 1 (F)
T State : 4
Flags : No flags
Length : 1 byte.

Eg : MOV A, B

2. MOV R, M

The contents of memory location, whose address is in H-L pair, is moved to register R.

Eg. MOV B, M



m/c cycle : 2 (F, MR)

States : 7

Flags : none

Length : 1 byte

3. MOV M, R.

The content of register R is moved to memory location addressed by H-L pair.

m/c cycle : 2 (F, MW)

States : 7

Flags : none

Length : 1 byte

Eg : MOV M, C.

4. MVI R, 8 bit data (move immediate data to register)

Load 8 bit data (byte) in a register.

m/c : 2 (F, MR)

State : 7

Flag : none

Length: 2 byte

Eg : MVI B, 08H

5. MVI M, 8 bit data (move Immediate data to memory)

The data is moved to memory location whose address is in H-L pair

M/c : 3 (OF, MR, MW)

Status : 10

Flag : None

Length : 2 bytes

Eg : MVI M, 25H.

H L

| 24 | 00 |

Then | 28 | 2400

6. LXI Rp, 16 bit data. (Load register pair with immediate data.)

This instruction is for Register pair, only high order register is mentioned in the ~~Regist~~ instruction.

M/c : 3 (OF, MR, MR)

Status : 10

Flags : None.

Length : 3 byte

1H 2.

Eg : LXI H, 4500H. | 45 | 00 |

7. LDA 16 bit address. (Load accumulator direct.)

copy the data byte into accumulator from the memory location specified by 16 bit address

M/C cycle : 4 (OF, MR, MR) MR.

Status : 13

Flags : None

Length : 3 byte

A

Eg : LDA ~~#~~, 4500 4500 | F8 | → | F8 |

8. STA 16 bit address. (Store accumulator direct.)

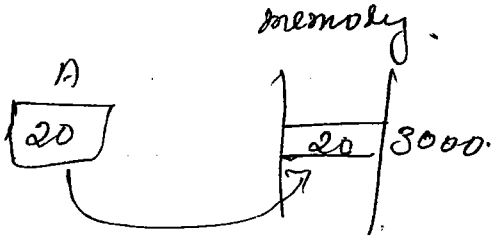
The content of accumulator is stored into memory location specified in the instruction.

m/c = 4 (F, MR, MR, MW)

States : 13

Flags : none

Length : 3 bytes.



Eg: STA 3000H.

9. LDAX Rp (Load accumulator Indirect)

The content of memory location, whose address is in register pair Rp is loaded into accumulator. This instruction is used only for BC & DE pairs.

m/c = 2 (F, MR)

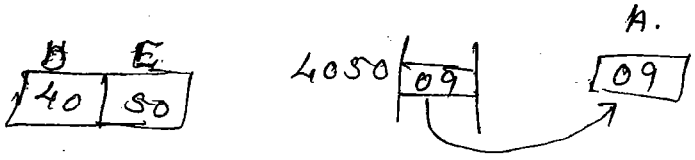
State : 7

Flags : none

Length : 1 byte.

Eg. LDAX D

If the content of DE pair is 4050, then this instruction will load the content of 4050H to accumulator.



10. STAX Rp (Store accumulator Indirect)

The content of accumulator is stored in the memory location whose address is in register pair Rp. This instruction also uses BC & DE pairs.

m/c : 2 (F, MW)

State : 7

Flags : none

Length : 1 byte.

Eg: STAX B

11. LHLD 16 bit address (Load HL pair Direct)

The content of memory location specified in the instruction is loaded to register L. The content of next memory location is loaded into register H.

M/c : 5 (F, MR, MR, MR, MR)

States : 16

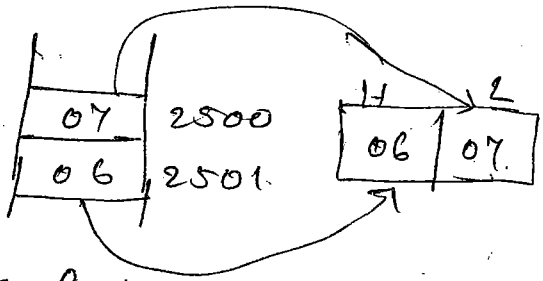
Flags : none

Length : 3 bytes.

Eg: LHLD 2500 H

L ← [2500]

H ← [2501]



12. SHLD 16 bit address (store HL pair Direct)

The content of L register is stored in memory location specified in instruction and content of H is stored in next location.

M/c : 5 (F, MR, MR, MW, MW)

states : 16

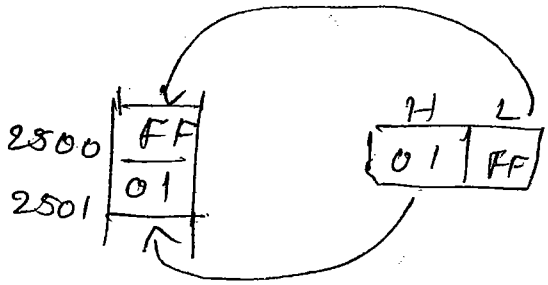
Flags : none

Length : 3 byte

Eg: SHLD 2500

2500 ← [L]

2501 ← [H]



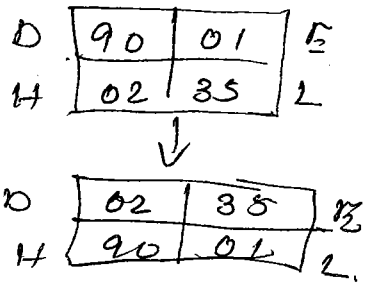
13. XCHG (Exchange HL pair with DE)

M/c : 1 (F)

State : 4

Flag : none

Length : 1 byte.



Eg. XCHG.

14. OUT 8 bit port address

Send or write data byte from accumulator to an O/p. device. The content of accumulator is moved to port specified by 8 bit address. port address can range from 00-FF

M/c : 3 (F^{4}, MR^{3}, IW^{3})

State : 10

Flags : none.

Length : 2 bytes.

Eg : OUT 01H

15. IN 8 bit PORT address

Accept or read data byte from an input device and place it to accumulator

M/c : 3 (F, MR, IR)

State : 10

Flag : none

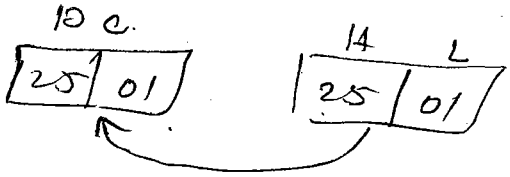
Length : 2 bytes

Eg : IN 0AH

16. PCHL (Load PC with HL)

The contents of HL pair are transferred to program counter. The contents of register H are moved to high order 8 bits of PC. The contents of L are transferred to low order 8 bits of PC.

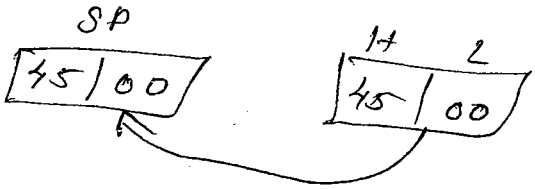
M/c = 1
States = 6
Flags : none
Length : 1 byte



17. SPHL. (Copy H&L to SP)

The contents of HC pair are transferred to the SP register.

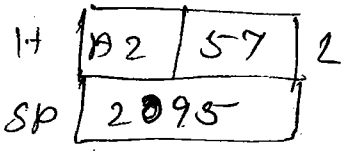
M/c - 1
States : 6
Flags : none
Length : 1 byte.



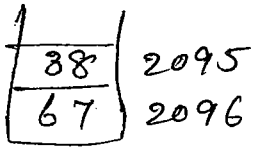
18. XTHL. (Exchange H&L with top of stack)

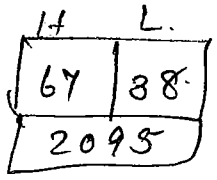
The contents of L register are exchanged with stack location pointed out by the contents of SP register. The contents of H-register are exchanged with next stack location (SP+1), however the contents of stack pointer register are not altered.

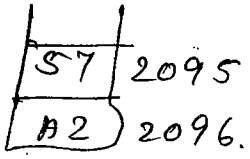
M/c : 5 (CF, MR, MR, MW, MW)
States : 16
Flags : none
Length : 1 byte

Eg: 

stack.



HTHL → 



Arithmetic Instructions.

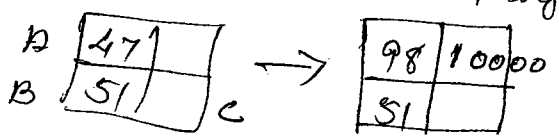
1. ADD R. (Add Register to accumulator)

The content of Register R. is added to the content of accumulator and sum is placed in the accumulator.

M/c : 1 (F)
States : 4
Flags : All
length : 1 byte.

0100 0111
0101 0001
1001 1000
9 8

Eg. ADD B



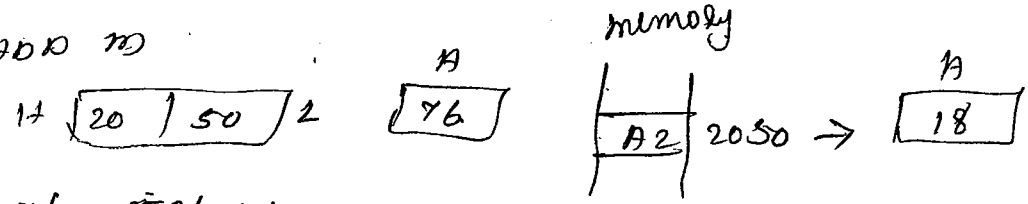
2. ADD M. (Add memory to accumulator)

The content of memory location addressed by HL pair is added to the content of accumulator. The sum is placed in accumulator.

M/c : 2 (F, MR.
States : 7
Flags : All
length : 1 byte.

76 0111 0110
A2 1010 0010
1 0001 1000

Eg. ADD M



Flag status: S=0, Z=0 AC=0 P=1 C=1.

3. ADC R. (Add Register with carry status to A)

The content of Register R and carry status are added to the content of accumulator. The sum is placed in accumulator.

M/c : 1 (F)

States : 4

Flags : All

Length : 1 byte.

A = 40 0100 0000
B = 70 0111 0000
Assume CS=1 0000 0001
0] 1011 0001

Eg : ADC B. S=1 Z=0, AC=0 P=1 C=0.

4. ADC M. (Add memory with carry status to A)

The content of memory location addressed by HL pair and carry status are added to the contents of A, and sum is placed in accumulator (A)

M/c = 2 (F, MR)

States : 7

Flags : All

Length : 1 byte.

Eg : ADC M.

5. ADI 8 bit data. (Add immediate data to accumulator)

The 8 bit data is added to the content of accumulator, result is placed in accumulator

M/c : 2 (F, MR)

States : 7

Flags : All

Length : 2 bytes

Eg. ADI 59H.

A
4A → A3

4A 0100 1010
59 0101 1001
1010 0011
A 3

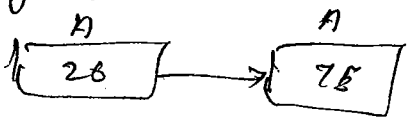
Flag S=1 Z=0, AC=1, P=1 C=0.

6. ACI 8 bit data. (Add immediate data with carry status to accumulator)

The 8 bit data and carry status are added to the contents of A, result is stored in A. commonly used for 16 bit addition

M/C : 2 (F, MA)
States : 7
Flags : All
Length : 2 bytes

eg: ACI 57H



A = 26	0010	0110
Data 57	0101	0111
CS = 1	0000	0001
	0111	1110 (7E)

Flags: S=0, Z=0, AC=0, P=1, C=0

8085 Subtraction

In order to perform Subtraction, 8085 follows:

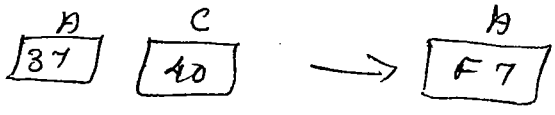
1) Find out 2's complement of subtrahend.
2) Add 2's complement with minuend.
3) Complement carry flag.

7. SUB R (Subtract Register from A)

The content of register R is subtracted from the content of A and result is placed in A.

M/C : 1 (F)
States : 4
Flags : All
Length : 1 byte

eg: SUB C



So A - C = 37 - 40

2's complement of 40	1100	0000
	0011	0111
	0 1111	0111

Complement carry so CS=1.

Flags S=1, Z=0, AC=0, P=0, C=1

8. SUB M (Subtract memory from A)

The content of memory location addressed by HL pair is subtracted from the content of A and result is placed in A.

M/c : 2 (F, MR)

States : 7

Flags : All

length : 1 byte

Eg SUB M

9. SUI 8 bit data. (Subtract immediate data from A)

The immediate data (2nd byte of the instruction) is subtracted from content of A. The result is placed in A.

M/c : 2

States : 7

Flags : All

Length : 2 bytes

Eg : SUI 87H.

A A

40 − 87H = 09

2's complement of 87 = 1100 1001

A = 40 = 0100 0000

1 1000 1001

Complement CS = 0.

Flags S=0, Z=0, AC=0, P=1, C=1

10. SBI 8 bit data. (Subtract Immediate data from A with borrow)

The 8 bit data and carry status are subtracted from the content of accumulator. The result is stored in A.

M/c : 2 (F, MR

States : 7

Flags : All

length : 2 bytes

Eg. SBI 26H.

2's com C