Master of Computer Applications

CAPOL403R01: Computer Organization & Architecture

Unit III: Lecture 4
Internal Memory

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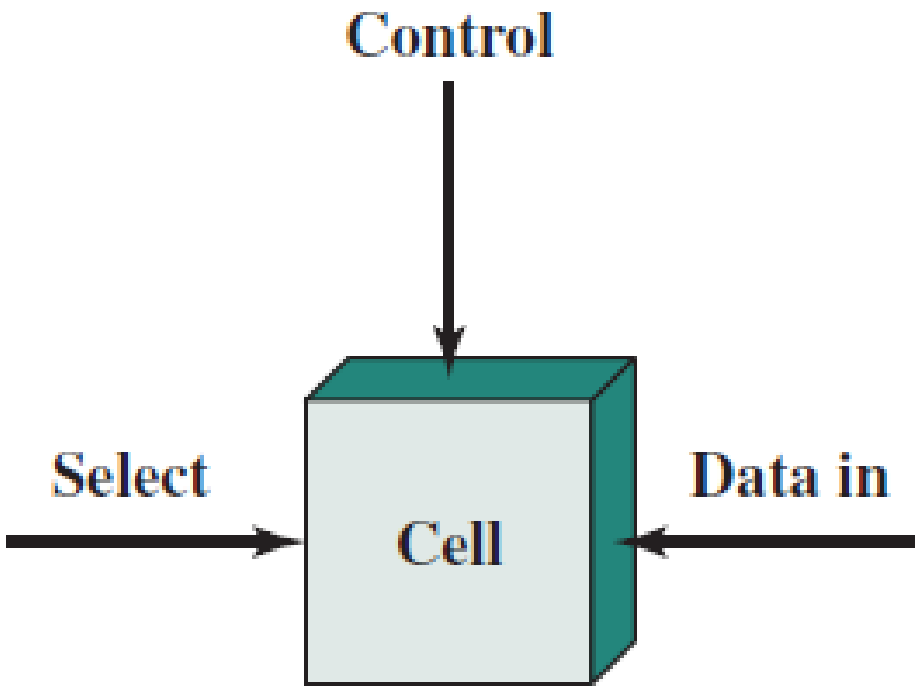
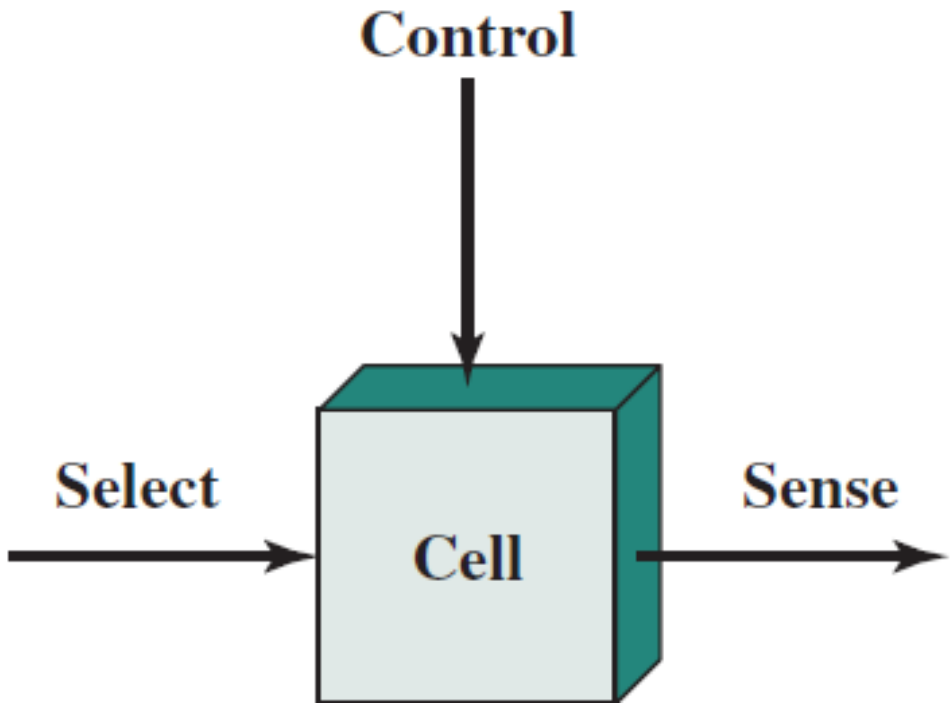
SASTRA Deemed to be University

Semiconductor main memory

Write operation



Read operation

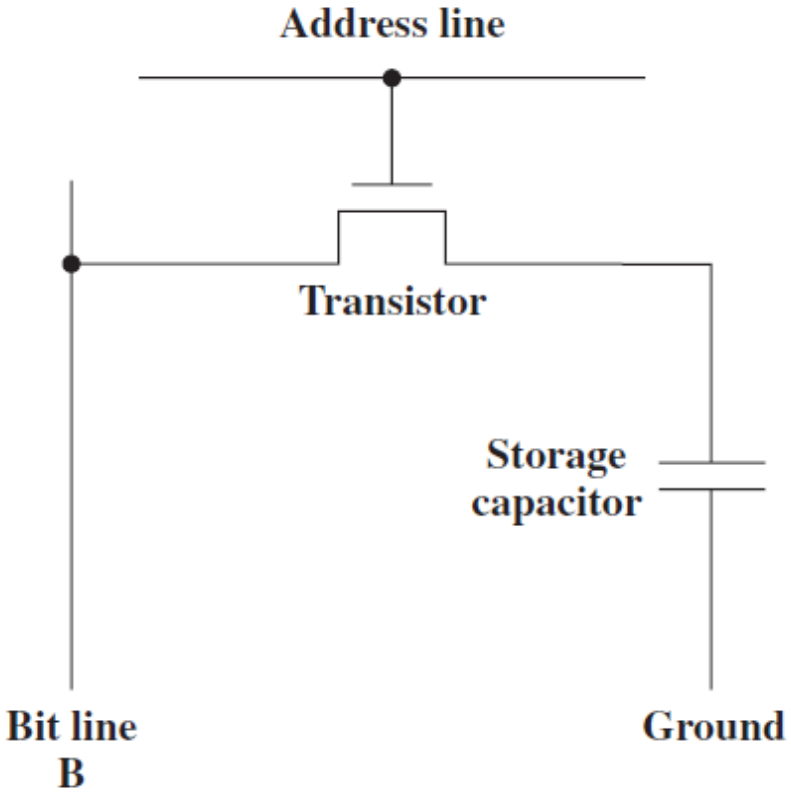


Semiconductor memory types

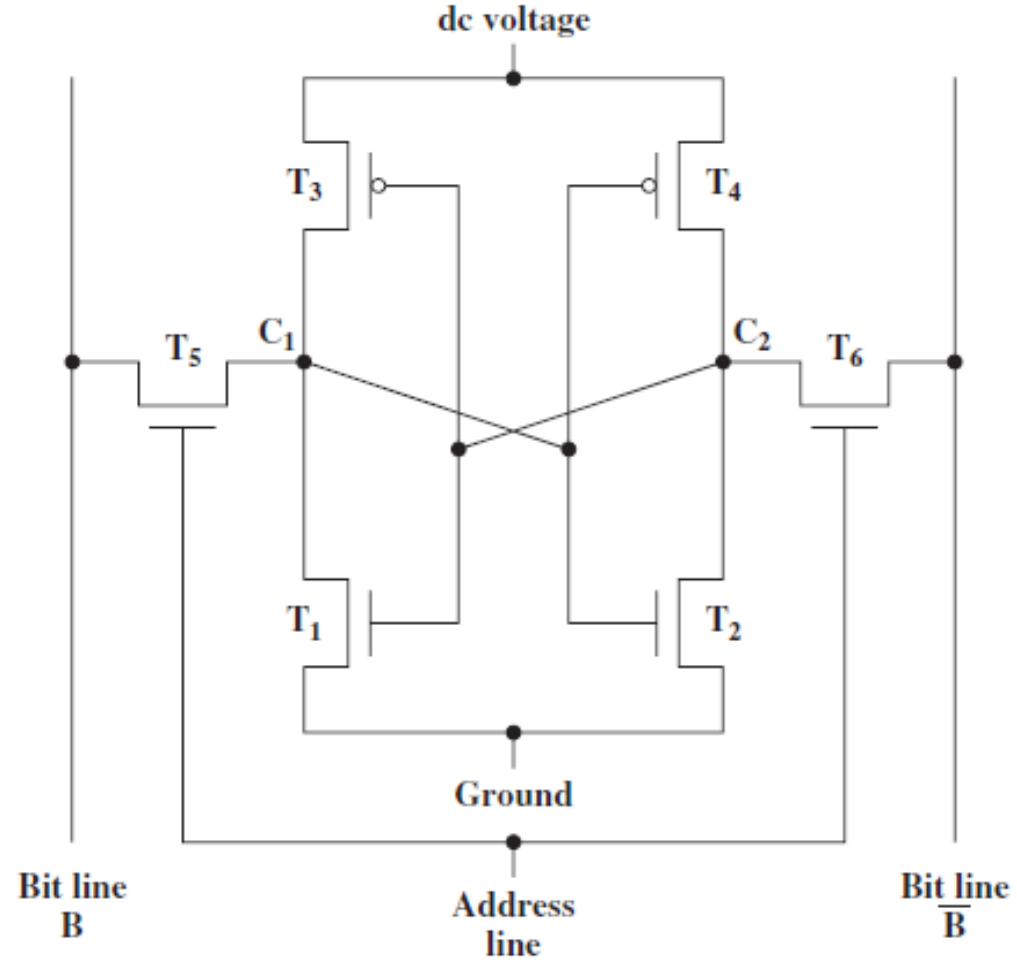
Memory type	Category	Erasure	Write Mechanism	Volatility
Random Access Memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory	Read – Only Memory	Not Possible	Mask	Nonvolatile
Programmable ROM (PROM)			Electrically	
Erasable PROM (EPROM)	Read-mostly memory	UV light, chip-level		
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		
Flash memory		Electrically, block-level		

RAM

DRAM



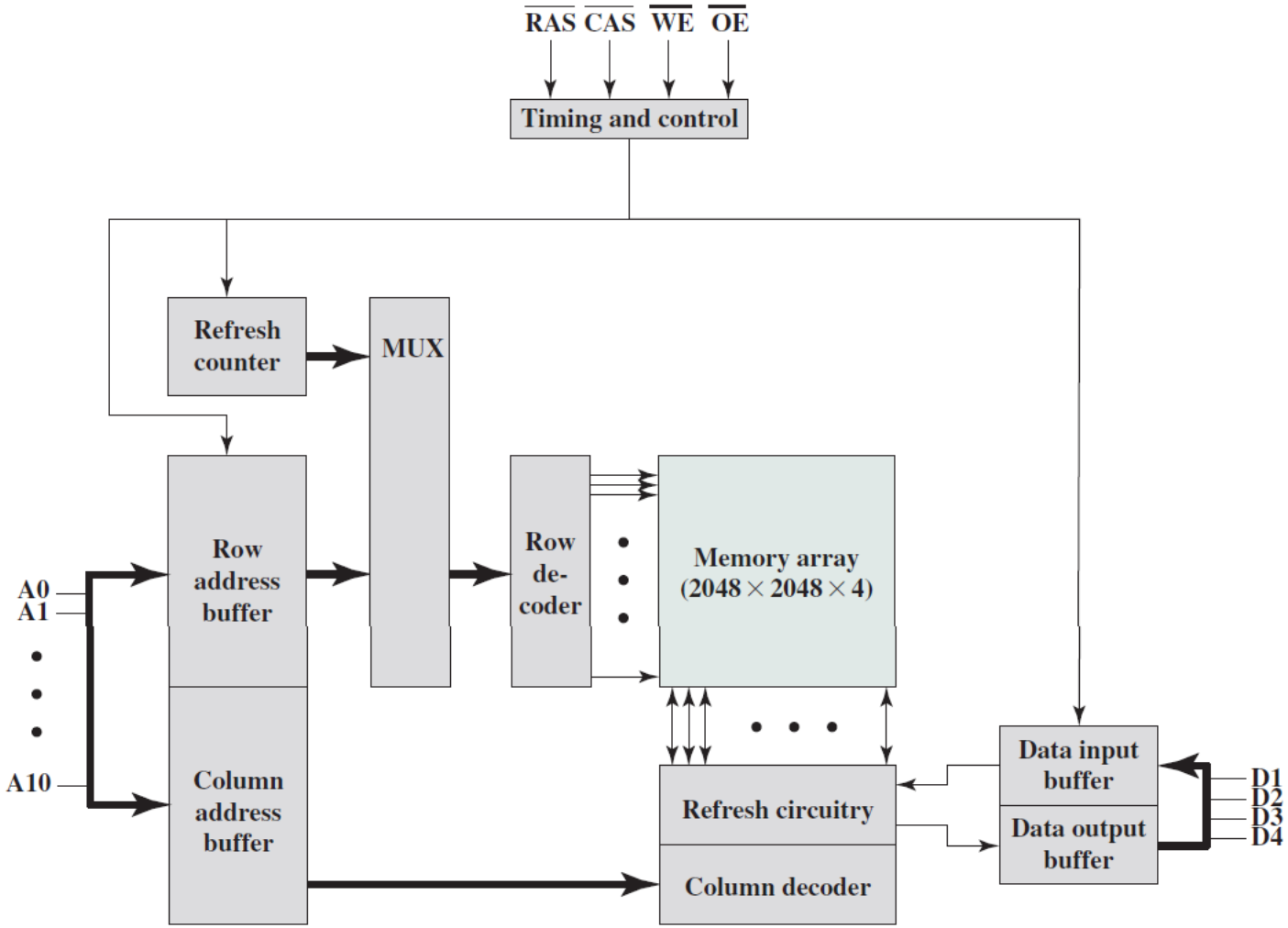
SRAM



Chip Logic

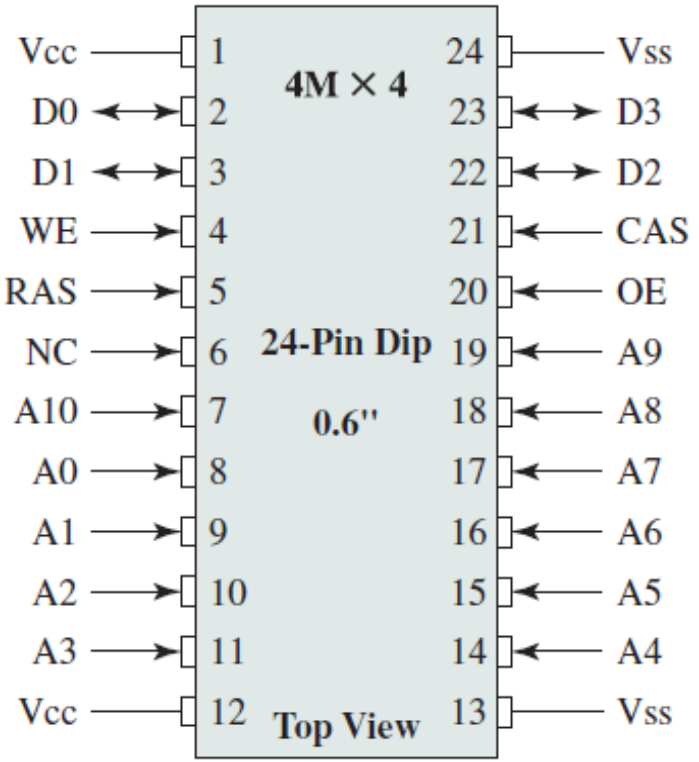
- One of the key issues of semiconductor memory is the number of bits of data that may be read/written at a time
- The memory with size S is organized as (S/B) words of B bits each
- At one extreme the B is the word size
- At the other extreme the B is one
- For example a 16M, 16bit word memory may be organized as 1 M, 16 bit words as one extreme (16 bits are read / write at the same time) and 16M, 1 bit organization (1 bit is read / write at a time)
- ROM and RAM organizations are almost same
  - ROM won't have write logic - so it is simpler

Chip logic – 16 M – 4 bit organization



Chip packaging

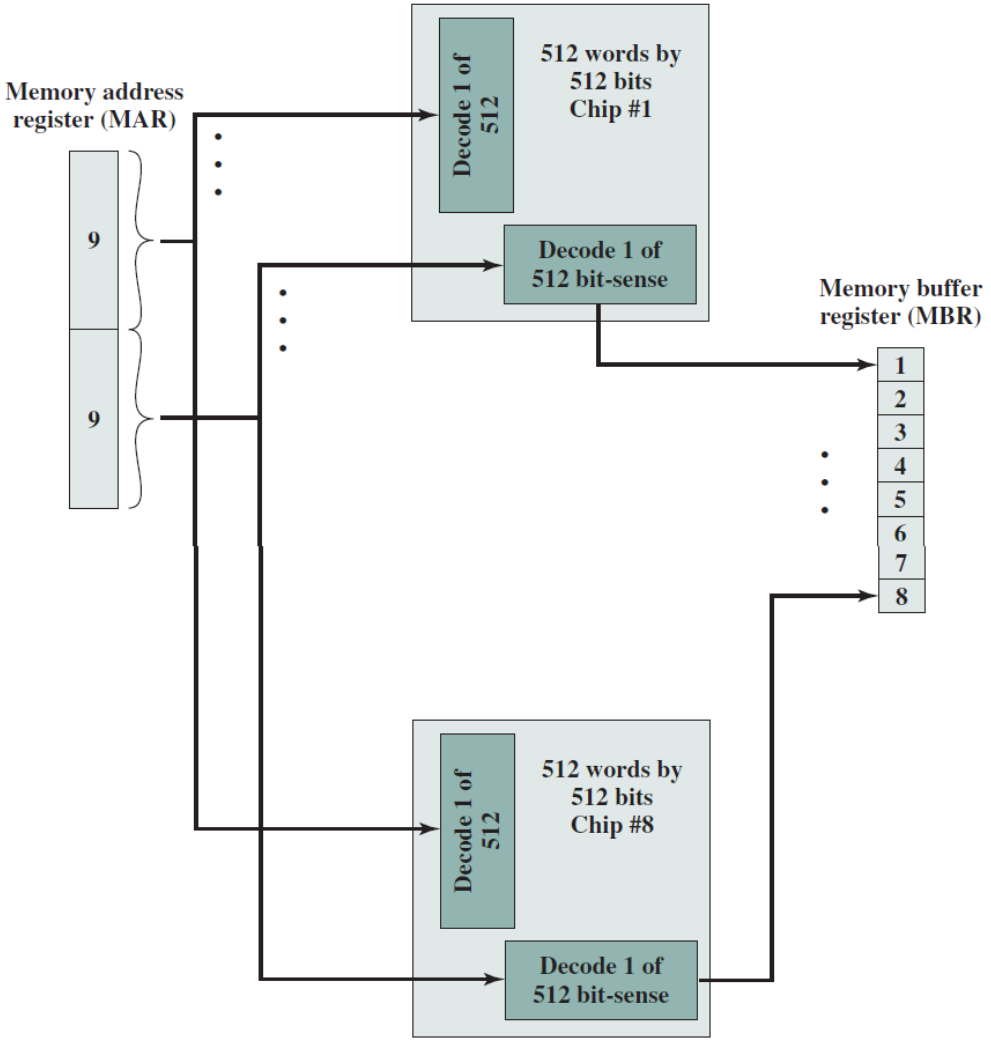
- The pins support the following signal lines
  - The address of the word to be accessed
    - For our example, 11 address lines (A0 to A10) are needed
  - Row address select and column address select signals
  - The data to be read out / write into
    - For our example, 4 data lines (D0 – D3) are needed
  - Read and write control signals
  - The power supply to the Chip (Vcc)
  - The ground pin (Vss)
  - A Chip enable pin
    - It is used to select a chip when multiple chips are connected to the address bus



Module organization

- If RAM chip has only one bit per address (word), then we need at least a number of such chips equal to the number of bits per word
- Question: Construct 256K x 8 bit word memory using 256K, 1-bit RAM chip
- To identify one address from 256K, 18 address bits are needed
  - 9 bits for row, 9 bits for column if the memory is organized in a matrix form
- Present the address to eight 256K, 1-bit RAM chip simultaneously
  - The chips are arranged in a column
- Save the data in MBR and access the data from MBR during READ
- Move the data to MBR, and write the data on these eight chips during write operation

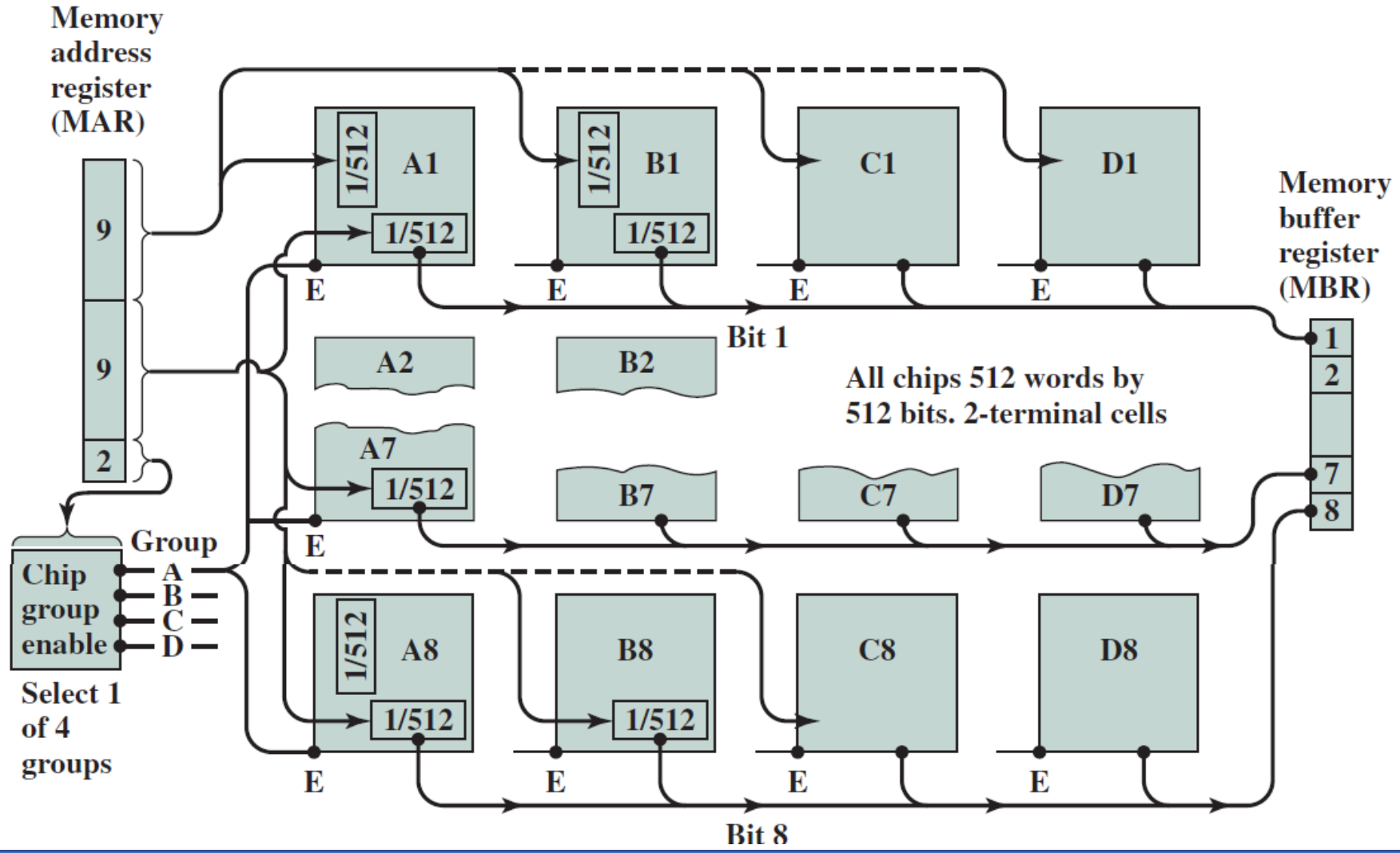
Module organization…



Module organization

- The organization works if the number of words are equal to the number of words per chip
- When the number of words are larger than the number of words of the chip, then the chips are arranged in a matrix format
- Example: Construct 1M X 8 bit memory using 256K X 1 bit memory
  - To get 8 bits from a single memory location, 8 chips are arranged in a column
  - To obtain 1M words, 1M/256=4 columns are needed
  - 1M word memory needs 20 bit address
  - 256K word memory requires 18 bit address
  - The remaining 2 bits are used to select one of the four columns
  - These two bits are connected to the CE pins

Module organization…



Thank you