Master of Computer Applications

CAPOL403R01: Computer Organization & Architecture

Unit V: Lecture 4

Direct Memory Access

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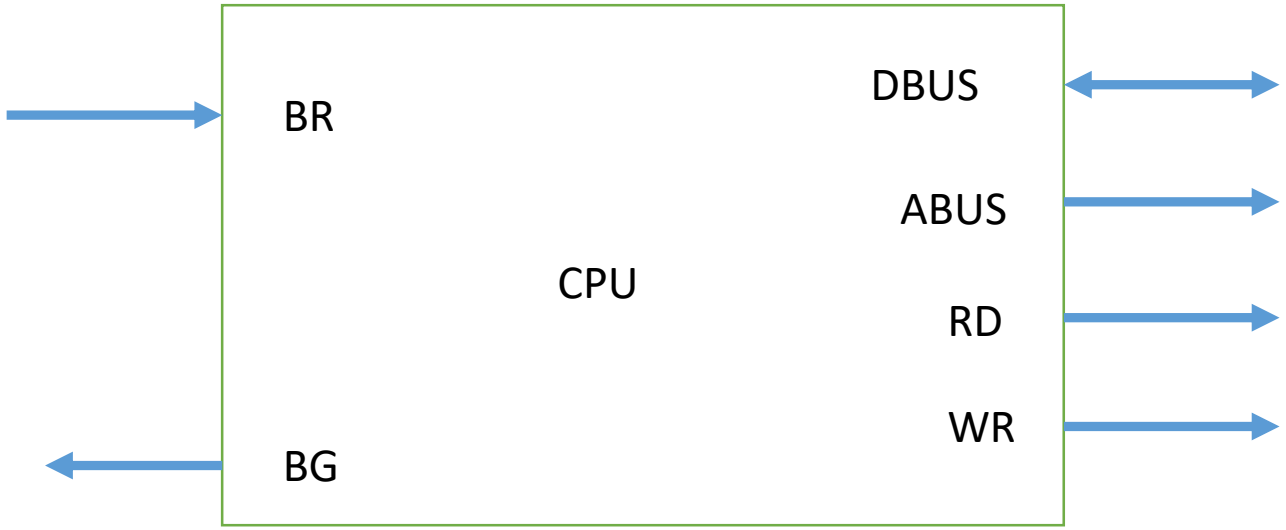
Modes of Transfer

- Programmed I/O
  - Processor is tied with the communication
- Interrupt initiated I/O
  - Processor has to do “house keeping” works
  - I/O transfer might be slow
- Direct Memory Access
  - CPU is removed from the communication
  - Peripherals are allowed to access memory without the intervention of the processor
  - Speed is enhanced

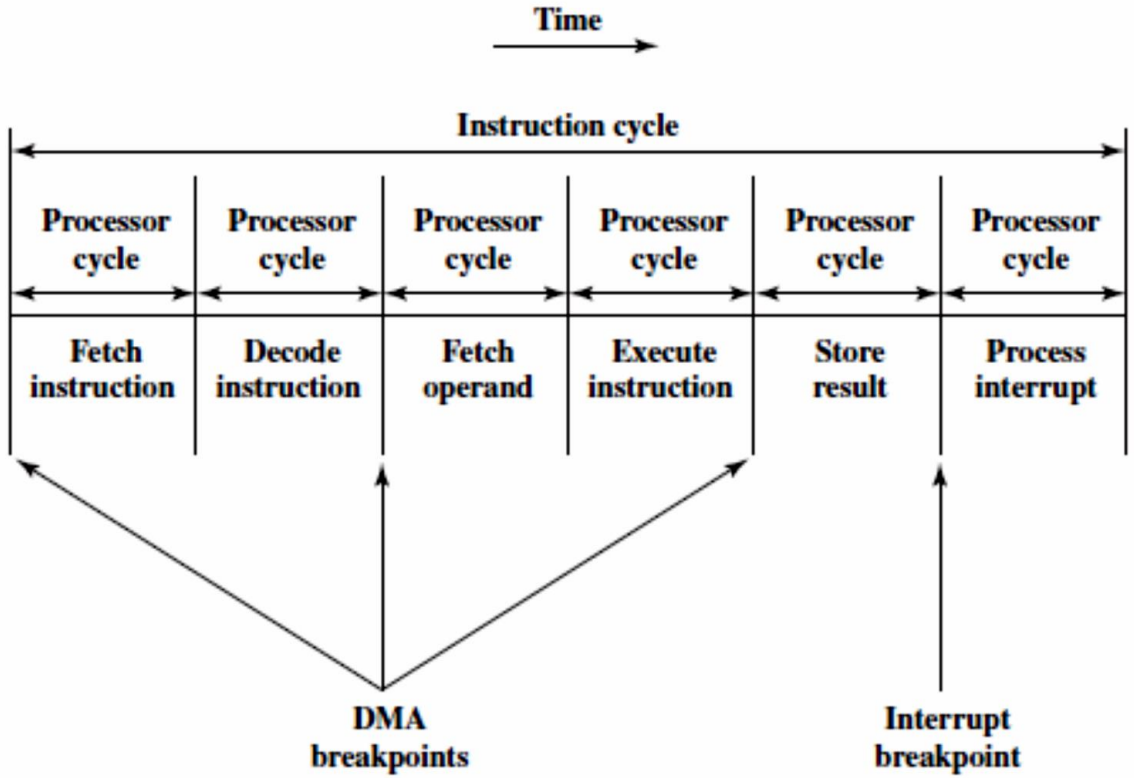
Direct Memory Access- CPU signals



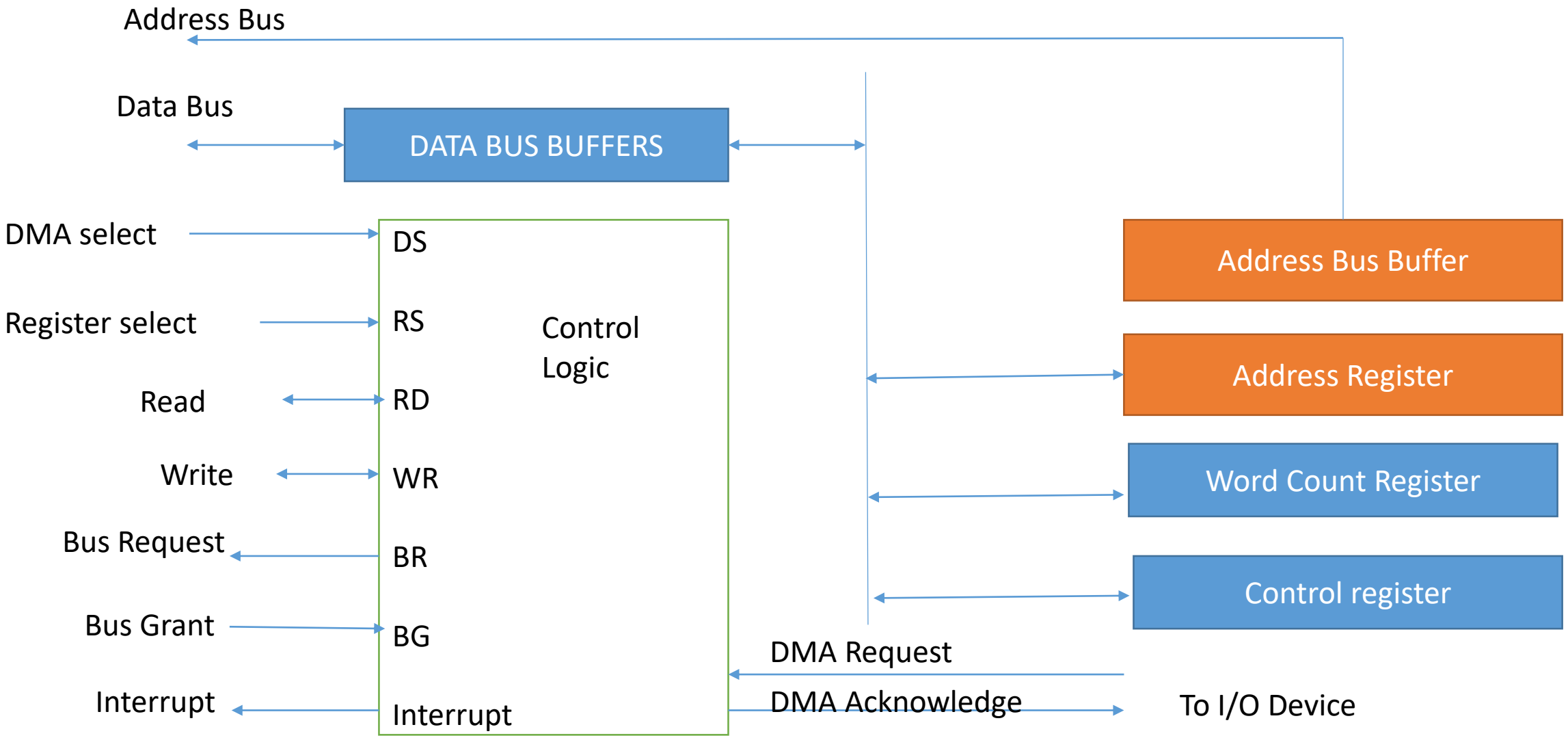
High Impedance when BG is enabled

DMA

- Burst mode of operation
- Cycle stealing mode of operation



Block diagram of DMA controller



DMA signals

- DMA is selected by the CPU using DS signal
- CPU selects the registers of DMA with RS signal
- Read / Write are bidirectional control signals
- Bus request / Grant is used with CPU
- DMA request / Grant is used with peripheral
- Address bus is handled by the DMA controller during DMA

DMA controller

- Address Register
  - It has direct communication with memory
- Count Register
  - It has the number of words to be transferred
  - It gets decremented after transferring a word
- Control Register
  - It is used to have the command

DMA Initialization

- The starting address of the memory block where data are available (for read) or where data are to be saved (for write)
- The word count, which is the number of words in the memory block
- Control to specify the mode of transfer such as read or write
- A control to start the DMA transfer

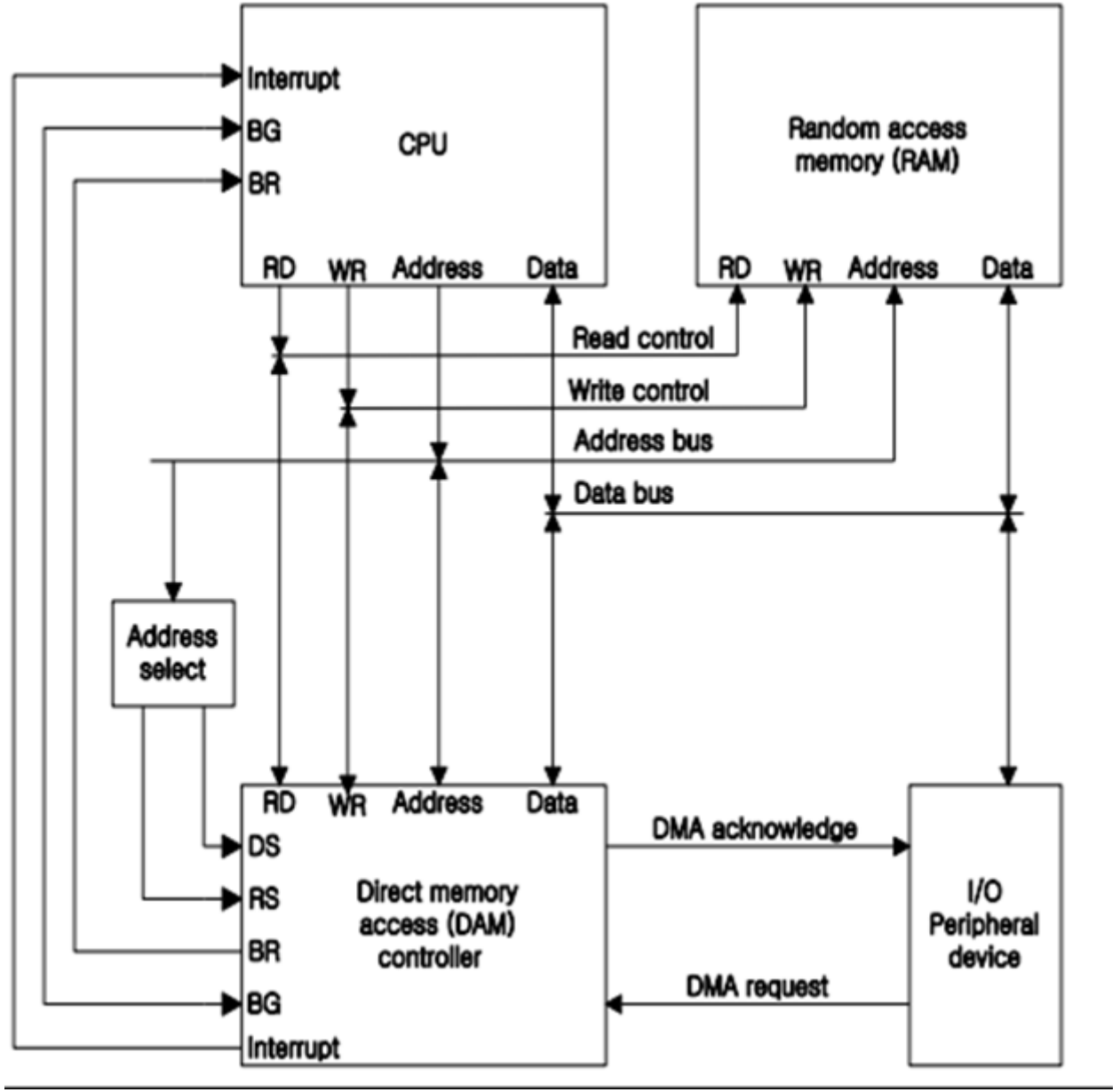
DMA transfer

- CPU communicates with the DMA as it communicates with interface
- DMA is initialized by the CPU through data bus
- Peripheral sends DMA request
- Bus request is enabled by DMA
- Bus grant is enabled by CPU
- Memory address is placed by DMA

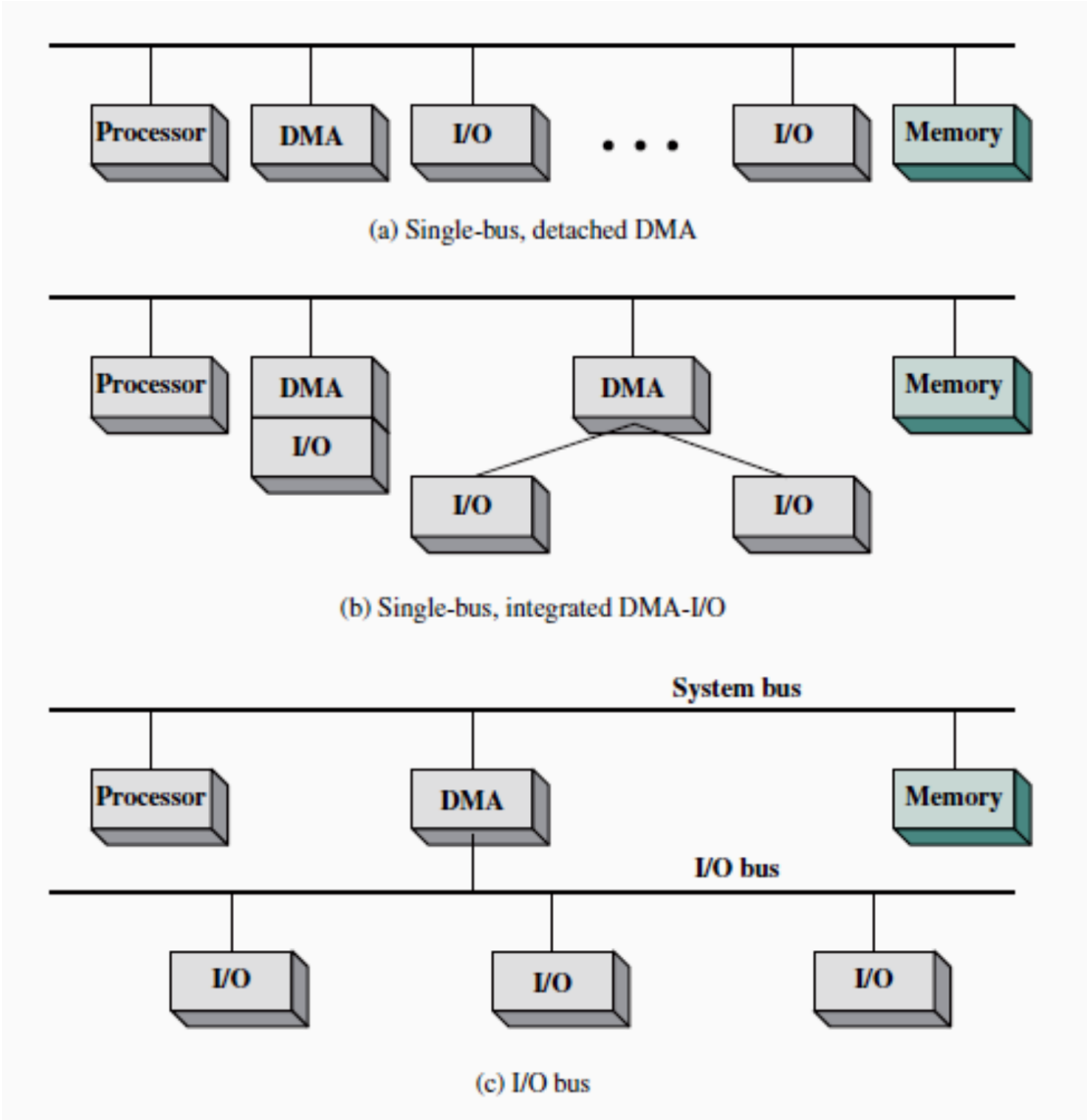
DMA transfer…

- DMA acknowledgement is enabled
- Data is transmitted / received by peripheral through data bus
- Word count is decremented and checked by DMA
  - If not zero, DMA request is checked
    - If enabled, address is incremented and acknowledgement is given
    - If disabled, bus request is removed
    - CPU gets its bus
  - If zero, bus request is removed
  - Processor is interrupted
    - Processor checks the word count to know the status of data transfer

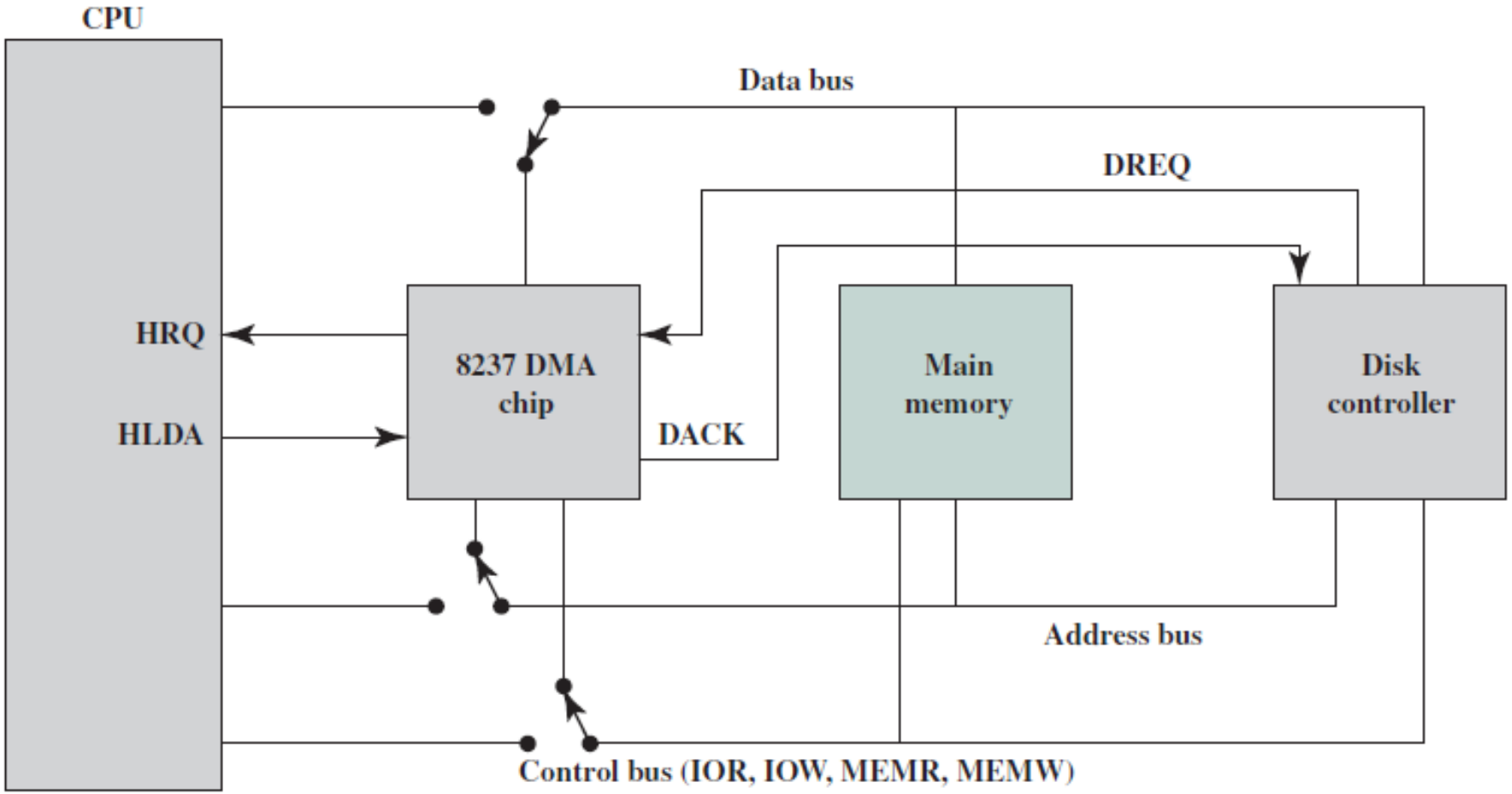
DMA transfer



Alternative DMA configurations



8237 – DMA controller



DACK = DMA acknowledge
DREQ = DMA request
HLDA = HOLD acknowledge
HRQ = HOLD request

Memory to disk transfer

1. The peripheral device will request the service of DMA by pulling DREQ high
2. The DMA will put a high on its HRQ (hold request), signalling the CPU through its HOLD pin that it needs to use the buses
   - HOLD must remain active high as long as DMA is performing its task.
3. The CPU will finish the present bus cycle (not necessarily the present instruction)
4. It responds to the DMA request by putting high on its HLDA

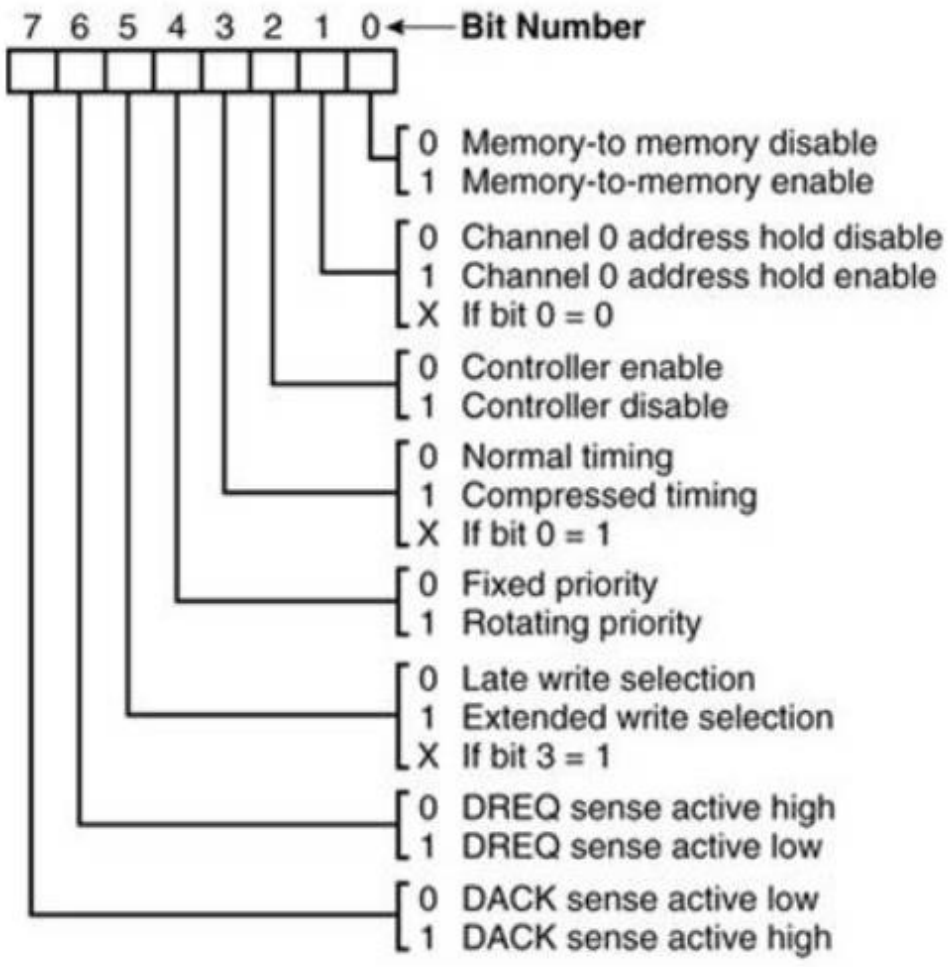
Memory to disk transfer…

5. DMA will activate DACK to tell the peripheral device that it will start to transfer the data
6. DMA transfer begins
   - 8237 puts the address of the first byte of the block on the address bus and activating MEMR
   - Memory puts the the byte from memory into the data bus
   - 8237 activates IOW to write it to the peripheral
   - DMA decrements the counter and increments the address pointer
   - It Repeats this process until the count reaches zero and the task is finished
7. 8237 has finished its job
   - It deactivates HRQ

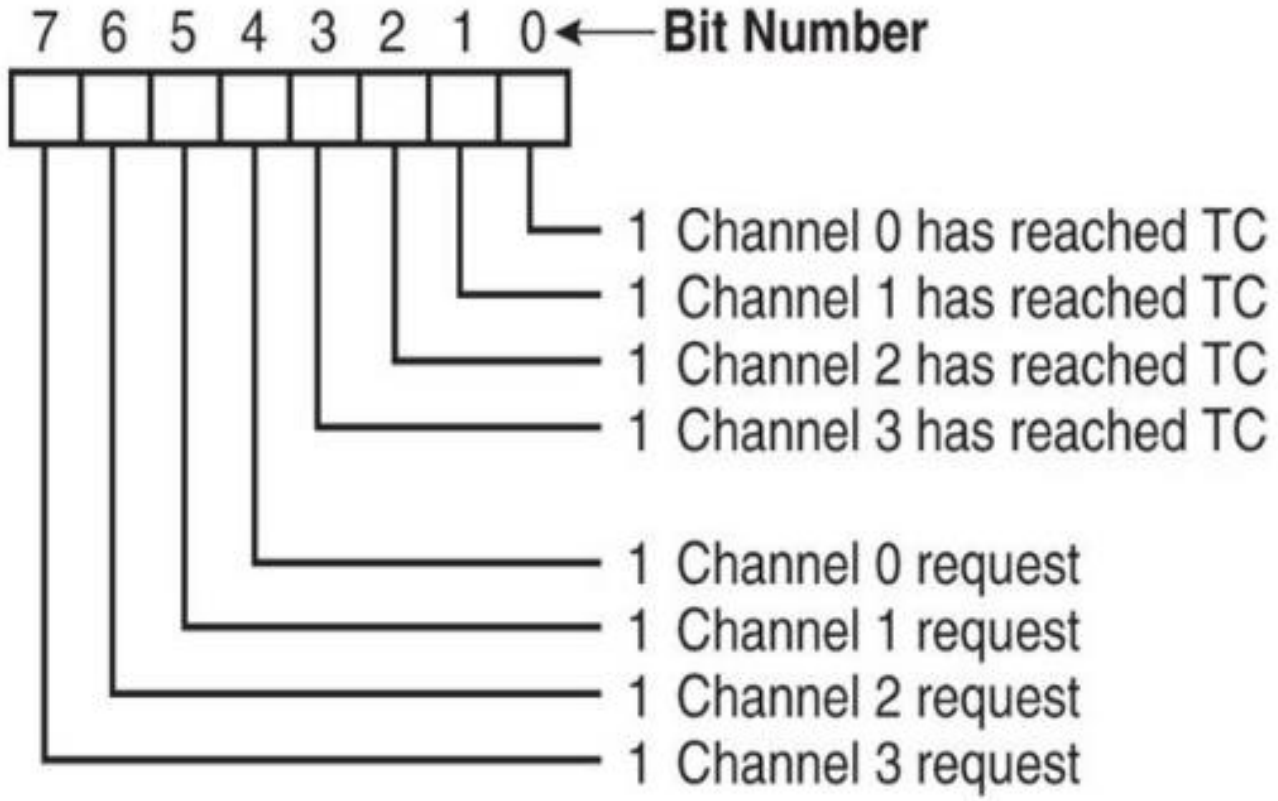
8237…

- The 8237 DMA is known as a *fly-by* DMA controller
  - The data being moved from one location to another does not pass through the DMA chip and is not stored in the DMA chip
- The 8237 contains four DMA channels
  - They can be programmed independently
  - Any one of the channels may be active at any moment
  - These channels are numbered as 0, 1, 2, and 3.

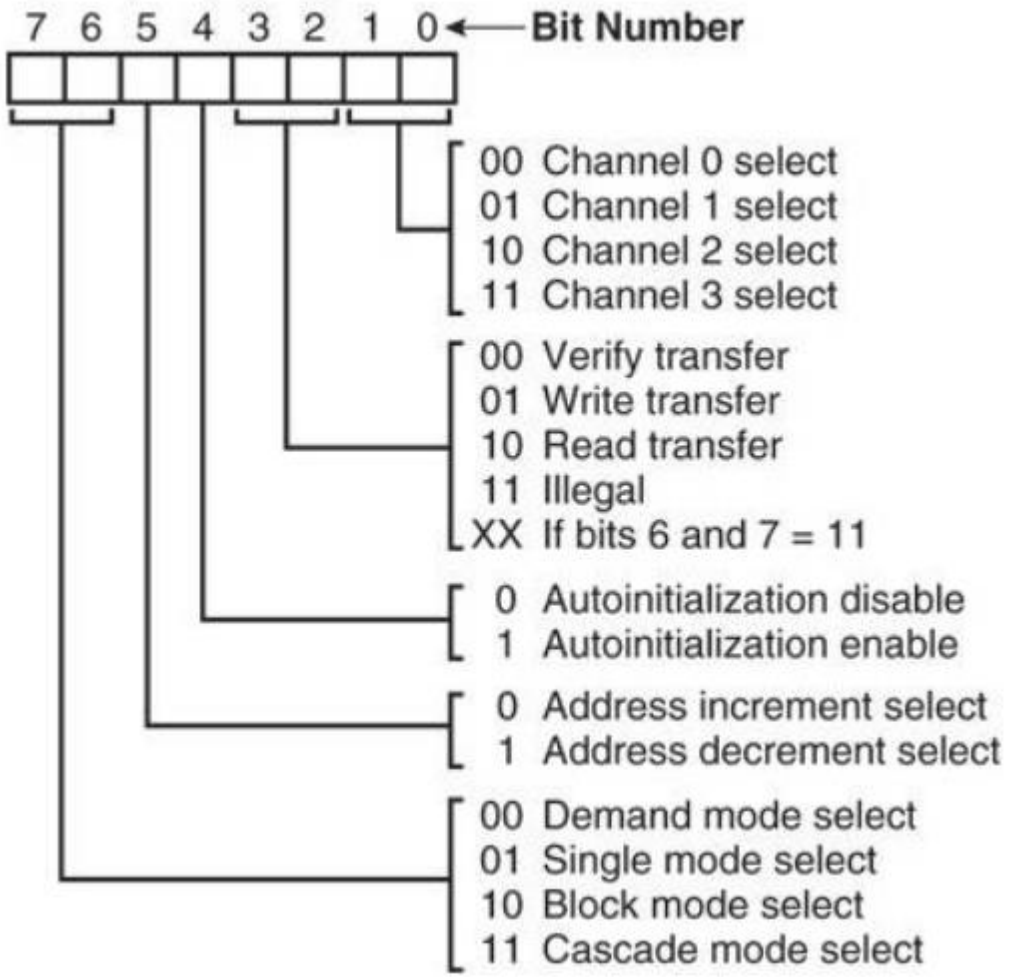
Registers of 8237 – Command register



Registers of 8237 – Status register

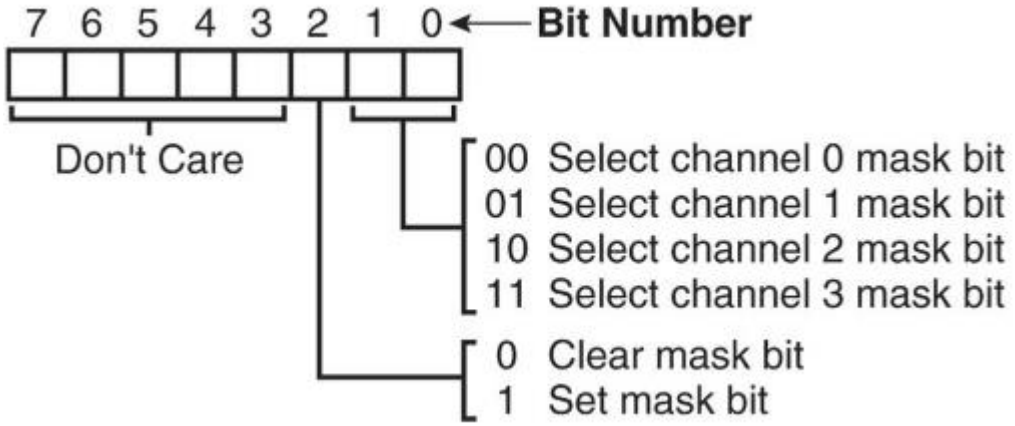


Registers of 8237 – Mode register

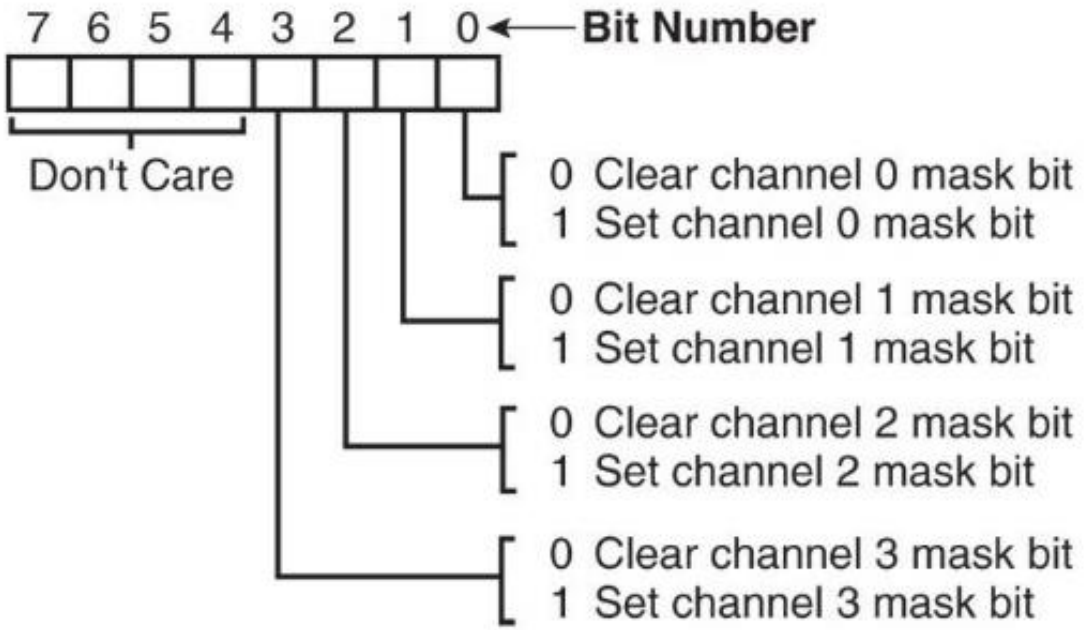


Registers of 8237 – Mask registers

Single mask register



All mask register



Registers of 8237

- 8237 has 8 data registers
  - 4 memory address registers for the 4 channels
  - 4 count registers for the 4 channels
- The processor sets these registers to indicate the location and size of main memory to be affected by the transfers

Thank You