**ReadMe\_State\_Machine\_X**

(Entity) Inputs and Outputs have been defined (in: "resetn", "sysclk" /   
out: "flag1").  
  
(Architecture) New type have been created to define signal "state" as this new type, when this type has states from s0 to s7 (in total 8 states).  
In the process we define the "starting state" (state <= s0; flag1 <= '0') when "resetn" equals to '0', when resetn equals to '1' every rising edge of sysclk the signal state will step forward to the next state from s0 to s7.  
In state s1 flag1 change to '1' and in s2 flag1 return to '0'.  
In state s5 flag1 change to '1' and in s7 flag1 return to '0'.  
After state s7, signal state will return to s0 in the next rising edge, and this loop will continue for a long time.