# CSC 347 LAB REPORT

## Lab #2 - DeMorgan's Theorem

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I pledge this work to be my own Vitaliy Prymak

# Objective:

*During this lab, the main goal is to build a circuit to verify DeMorgan's Laws.*

# Equipment and Chip used:

- *Elenco Digital/Analog Trainer X-150,*
- *Chips: 74HCT08 (AND gate), 74HCT32 (OR gate), 74HCT04 (inverter gate)*

# Design procedure:

*Design a circuit with AND, OR and NOT gates that will prove DeMorgan's Laws: (X+Y)' = X' Y' (XY)' = X' + Y'*

1. Derive the truth table:

| X | Y | F2=(X+Y)' | F2=X'Y' | F3=(XY)' | F4=X'+Y' |
|---|---|---|---|---|---|
| 0 | 0 | T | T | T | T |
| 0 | 1 | F | F | T | T |
| 1 | 0 | F | F | T | T |
| 1 | 1 | F | F | F | F |

*Table 1 Truth table of four circuits*

## 2. Logic diagram includes the four circuits (2 inputs and 4 outputs)

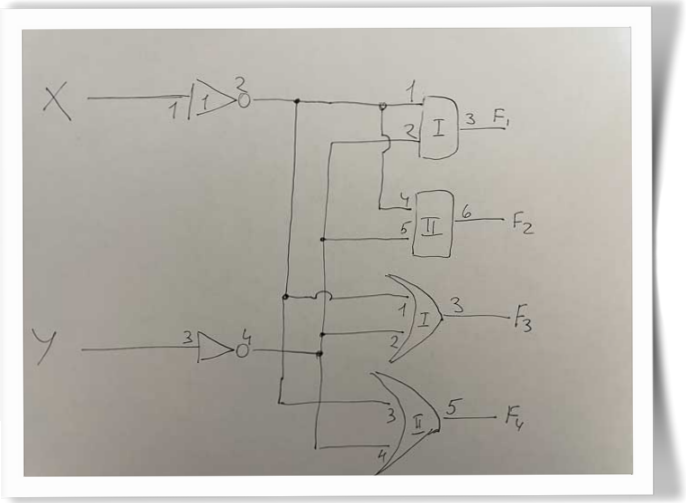



*Figure 1 Logic diagram with four circuits*

## 3. Circuit Construction

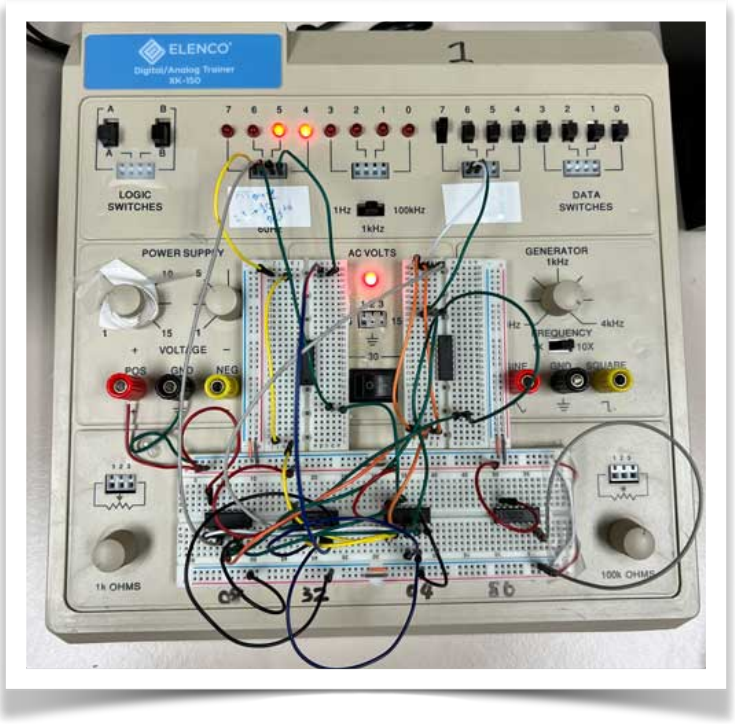



*Figure 2. Four circuits*

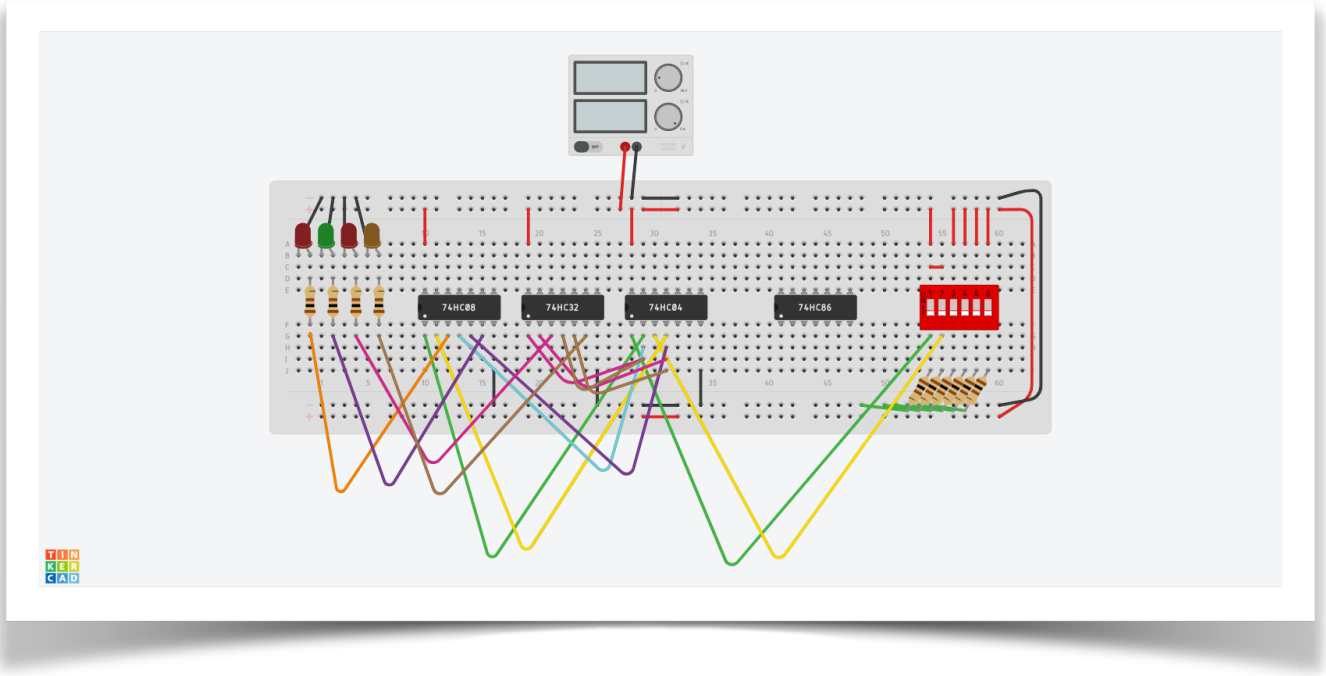



Figure 3. TinkerCad scheme of four circuits

## 4. The inputs and outputs from my experiment:

| X | Y | F2=(X+Y)' | F2=X'Y' | F3=(XY)' | F4=X'+Y' |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 |

*Table 2 Results of experiment*

## 5. Result and Conclusions:

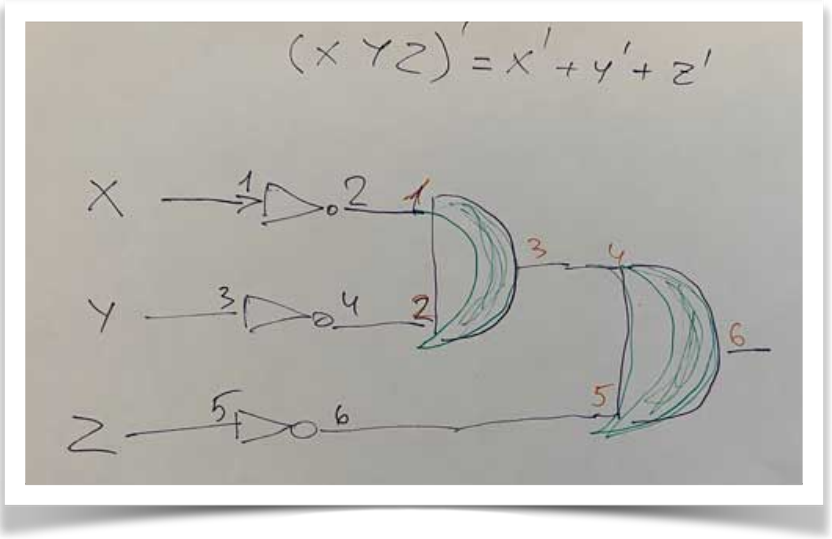
During experiment I've verified DeMorgan's Theorem by the help of Truth Table (Table 1) and Experiment's result (Table 2). Both tables match. Conclusion DeMorgan's Theorem, which apply negation for both operand and operator works.

## 6. Reference:

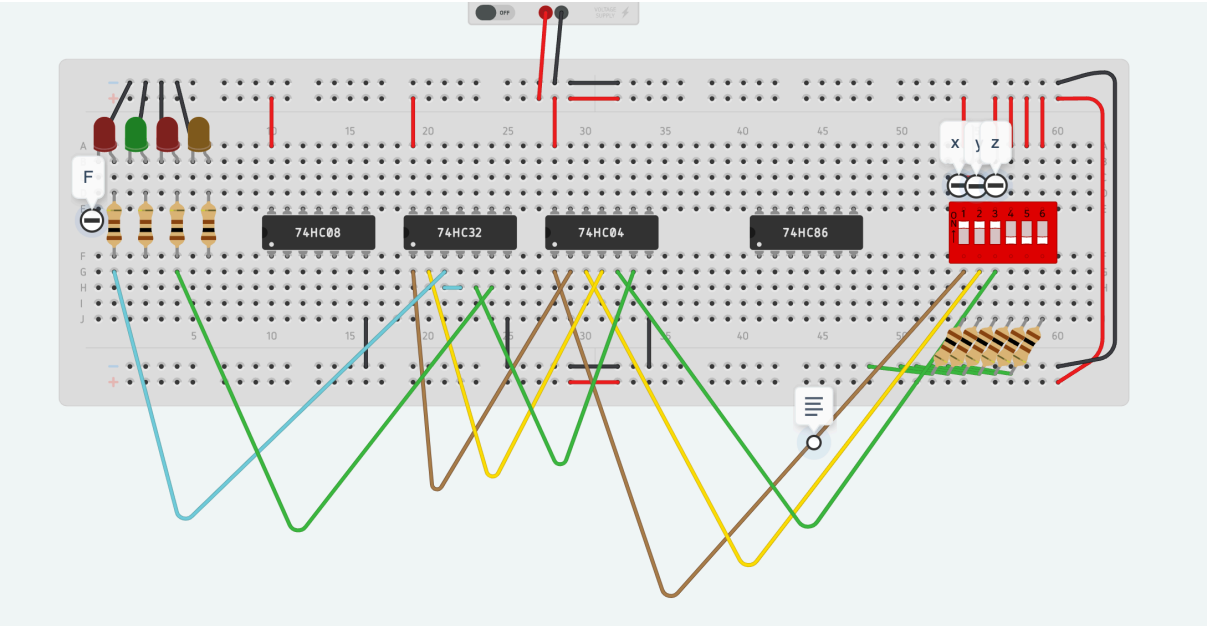
https://www.tinkercad.com/things/jKwa8XzdyxS-copy-of-csc-347-starter-kit/editel?sharecode=A2bZ3Tx0CrnGQ1eUVVa6vxHQ29hrIU5mrDGRdPEywrU

# HOMEWORK:

Design a circuit to prove the following DeMorgan's theorem for 3 variables(xyz)' = x' + y' + z'



| X | Y | Z | X’ | Y’ | Z’ | X’+Y’ | X’+Y’+Z’ |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |




https://www.tinkercad.com/things/lo8KyzLi4Ex-copy-of-csc-347-starter-kit/editel?sharecode=NheTpda-cJgPFvkfEEUw0WhNYhNkaJphD_MGzGe2DGc