HX710 (A / B)

24-bit analog output temperature measurement with digital / digital (A / D) converter chip (HX710A)

Measuring tape (DVDD-AVDD) the voltage difference between the 24-bit analog / digital (A / D) converter chip (HX710B)

Brief introduction

HX710 sea using integrated circuit core technology patents, is a specifically designed for high-precision electronic scale and 24-bit A / D converter chip. Compared with the same type of another chip, the chip having a high integration, fast response, strong anti-interference advantages. Reducing the overall cost of electronic scales, improve the overall performance and reliability.

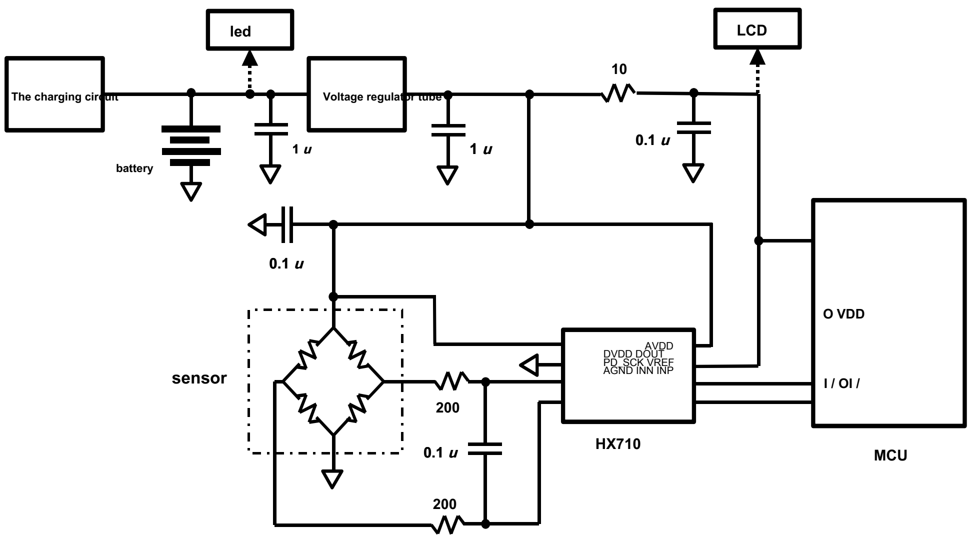
Input gain of the low noise amplifier 128, when the reference voltage VREF is 5V, the full amount of the differential input signal corresponding to the amplitude of ± 20mV. A clock oscillator in the chip without any external components. HX710A digital temperature sensor chip in the chip can be directly read out, i.e. the temperature within the system. HX710B may be used to detect the battery voltage detected by the voltage difference (DVDD-AVDD) a.

All control signals are driven by the pins, without programming the internal registers of the chip. MCU needs only two I / O ports can be controlled to achieve all of the ADC, including power-down control. Automatic power on reset initialization process simplifies the boot.

Feature

- Direct temperature measurement chip and a digital output (HX710A)
- (DVDD-AVDD) measuring the voltage difference (HX710B)
- Chip low noise amplifier gain 128
- Chip clock oscillator without any external devices
- Automatic power on reset circuit
- Simple digital serial communication and control: all controlled by input pins, without programming the chip register
- Optional output data rate of 10Hz and 40Hz
- Sync suppression of 50Hz and 60Hz power source interference
- Power consumption:

  Typical operating current: 1.2mA, off current: <1 μ A
- Voltage range: 2.6 ~ 5.5V
- Operating temperature range: -40 ~ + 85 ℃
- 8 pin SOP-8 or DIP-8 package



HX710 Scale Application Reference Schematic pricing

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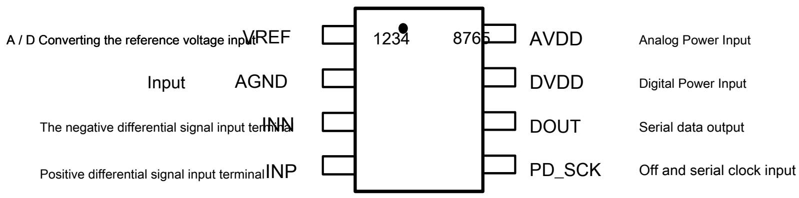
AVIA SEMICONDUCTOR

Pin Description



SOP-8 or DIP-8 Package

Pin Number	Name	performance	description
1	VREF	analog input	A / D converter reference voltage input (1.8V ~ AVDD)
2	AGND	input	Input
3	INN	analog inputs	The negative differential signal input terminal
4	INP	Analog input	Positive differential signal input terminal
5	PD_SCK	Digital input	Power-down control (active high) and serial clock input
6	DOUT	digital output	Serial data output
7	Power	input DVDD	Digital Power Input (2.6 ~ 5.5V)
8	Power	input AVDD	Analog Power Input (2.6 ~ 5.5V), AVDD voltage is not higher than the voltage DVDD

Pin description Table

The main electrical parameters

parameter	Conditions and instructions	Minimum	Typical values	Max	Unit
Full-scale differential input range (FSR)	V (inp) -V (inn)		± 0.5 (VREF / 128)		V
Input common mode voltage range		AGND + 0.9		AVDD-1.3 V	
VREF Input voltage range		1.8		AVDD	V
No noise digits (Noise-Free Bits) (1)	Vref = Avdd = 5V , Rate = 10Hz		17		Bits
	Vref = Avdd = 5V , Rate = 40Hz		16		Bits
The output data rate			10/40		Hz
Output data encoding	Twos complement	800 000		7FFFFF HEX	
Output settling time (2)			400/100		ms
Nonlinearity (INL)	Differential inputs, compared to full-scale gain		± 0.001		% Of FS
Enter zero drift (Input Offset)			0.01		mV
Input noise precision (Noise Free Resolution)			50		nV (rms)
Temperature Coefficient (Temperature Drift)	Enter zero drift (offset drift)		± 15		nV / ℃
	Gain drift (gain drift)		± 7		ppm / ℃
Digital Temperature Sensor (significance: 15 Bit)	Temperature measurement range	- 40		+ 85	℃
	Nonlinearity (- 40 ~ + 85 ℃)		0.5		℃
	Temperature measurement accuracy (15 Bit)		20.4		LSB / ℃
Input common mode signal rejection ratio	At DC, Δ VIN = 10mV		100		dB
Power Supply Rejection Ratio (PSSR)	At DC, Δ AVDD = 0.1V		100		dB
voltage	AVDD , DVDD	2.7		5.5 V	
Supply Current	normal work		1200		μ A
	Power outage		0.5		

(1) noise-digit (Noise-Free Bits) = ln (FSR / Peak-to-Peak Noise) / ln (2) .

(2) the output stabilization time is the time from power-up, reset, or the output data rate is changed to the time-efficient stable output data.

Table II list the main electrical parameters

Analog Input

Differential analog inputs can be engaged directly with the differential output of the bridge sensor. Since the bridge sensor output signal is small, to make full use of A / D converter input dynamic range, the input preamplifier gain as large as 128. When the reference voltage VREF is 5V, the gain corresponding to the full-scale differential input voltage ± 20mV.

Power supply

Digital power (the DVDD) should be the same MCU chip voltage supply voltage or less, the MCU serial data to ensure proper communication.

Analog power (the AVDD) digital power supply voltage is not higher than (the DVDD) voltage. MCU may use the same chip a digital power supply, if desired with appropriate isolation to reduce interference digital circuit analog circuit.

A / D converter reference voltage input (VREF) to be connected to the power supply sensor. The analog power supply voltage can be taken directly (AVDD). AVDD also be after dividing resistor is supplied with the sensor, in order to reduce the power consumption of the sensor.

Clock Select

HX710 chip clock from an internal clock oscillator chip, output data rate is typically 10Hz or 40Hz.

Temperature Measurement (HX710A)

HX710A inside the chip digital temperature sensor can be used directly in the readout chip, i.e., the temperature in the system. Effective (stable) with a median of 15. Typical measurement accuracy per degree temperature (℃) 20.4 Readings (15).

When using a digital temperature sensor, the temperature sensor should be noted that within the chip, greater zero and the gain difference between the chip and the chip. As used to measure the absolute temperature, and zero gain correction required. The system used for measuring the temperature of the temperature-related performance compensation, zero and gain correction is not required, as long as the linearity of the temperature measurement can meet the requirements.

(DVDD-AVDD) measuring the voltage difference (HX710B)

HX710B available for measuring the voltage (DVDD-AVDD) is poor. If DVDD is connected directly to the battery output, and AVDD is provided by the output regulator, the HX710B can be used to directly measure the battery voltage, without any external components.

Serial communication

Serial communication lines and the DOUT pin PD_SCK composition for outputting data, and selecting output data rate input signal.

When the data output pin DOUT is high, indicating that the A / D converter output data is not ready, then the serial clock input signal PD_SCK should be low. When DOUT goes low from high, PD_SCK enter ranging from 25 to 27 clock pulses (Figure 2). Wherein a rising edge of the clock pulse of the read out maximum 24-bit output data (the MSB), until the completion of the 24th clock pulse, the output data 24 bits up to the lowest bit by bit from the output completion. The first 25 to 27 for outputting clock pulses at selected time A / D conversion And input data rate Input signal, see Table III.

Selecting a rate input pulses PD_SCK		
25	Differential signal	10 Hz
26	Temperature measurement (HX710A)	40 Hz
26	DVDD-AVDD measured (HX710B) 40 Hz	
27	Differential signal	40 Hz

Table III input selection and outputs the selected data rate

Enter the number of clock pulses PD_SCK of not less than 25 or more than 27, otherwise it will cause serial communication error.

When the A / D converter input or output data rate change signal, A / D converter needs four cycles to stabilize a data output. After four data DOUT output from the high level period only goes low, the output of valid data.

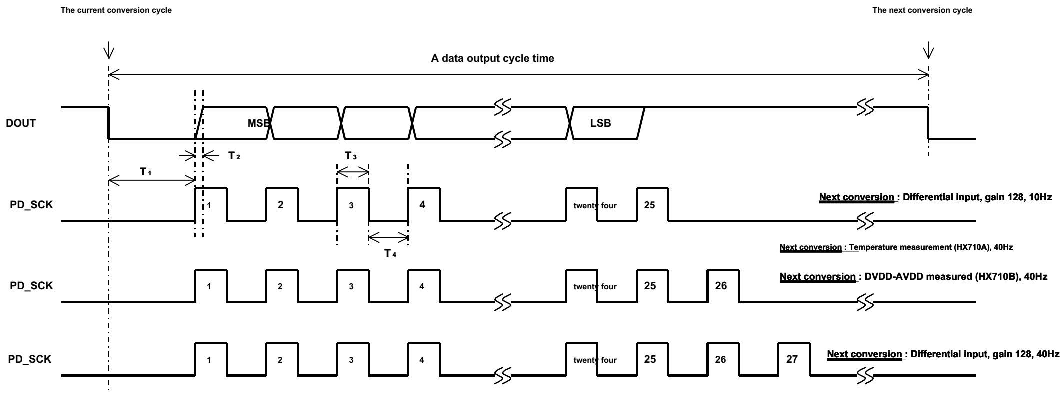


FIG second data Export , Gain select input channels and a timing chart

symbol	Explanation	Min Typ Max Units			
T_1	DOUT viceversa pulse PD_SCK	0.1			μ s
T_2	PD_SCK data valid pulse rising to DOUT			0.1	μ s
T_3	PD_SCK positive pulse level time	0.2		50	μ s
T_4	PD_SCK negative pulse level time	0.2			μ s

Reset and power-down

When power chip, automatic power on reset circuit will automatically reset the chip within the chip.

PD_SCK input pin is used to control power down HX710. When PD_SCK is low, the chip is in normal operation.

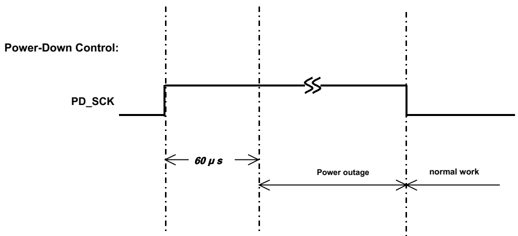


Figure III Off control

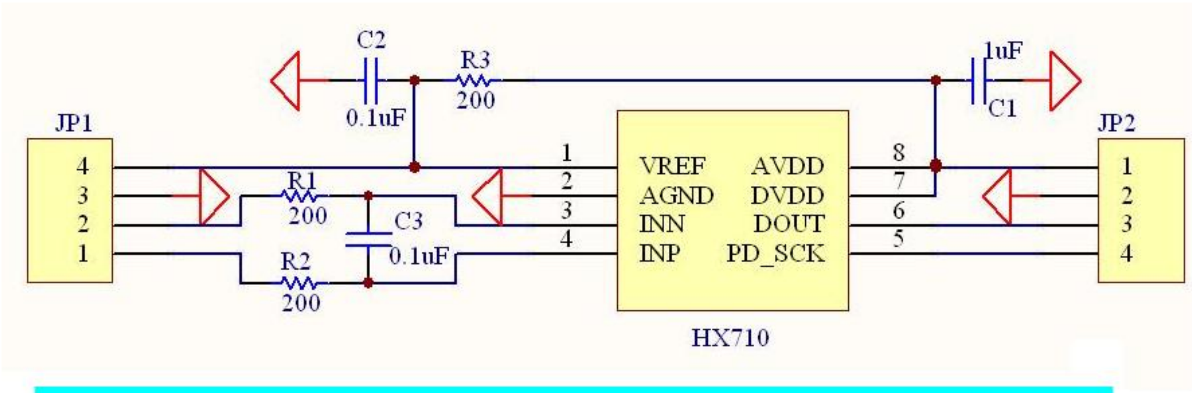
If PD_SCK goes high from low and remains at a high level over 60 μ s, HX710 i.e. enter the off state (Figure 3). When PD_SCK back low, the chip will Re-enter the normal working condition. Back to normal operation after the chip from the power-off state, to maintain the slew rate and the input signal power before the selection, the off current can not be performed in the data conversion cycle clock pulses changes. But it should be performed after the data conversion cycle or after a number of clock pulses is changed.

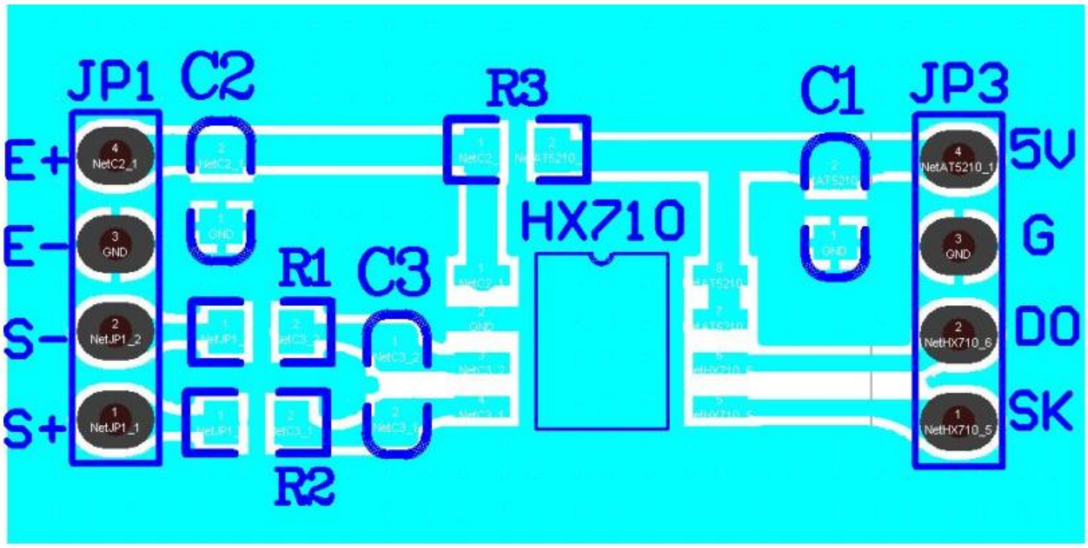
After the chip into the normal operating state from a reset or power-off state, A / D converter needs four cycles to stabilize a data output. After four data DOUT output from the high level period only goes low, the output of valid data.

Applications

It is applied to an electronic scale view of a typical embodiment of a chip HX710 FIG. The program uses a regulator at the same time to the ADC and the MCU supply, can be used for LED display, LCD display can also be used.

reference PCB Plate (single)





Reference driver (assembler)

```
/ * ------------------------------------------------- ------------------ call in ASM:
                                LCALL ReadAD
You can call in C:              extern unsigned long ReadAD (void);
                                  .
                                  .
                                unsigned long data; data =
                                ReadAD ();
                                  .
                                  .
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - * /
PUBLIC              ReadAD
HX710ROM            segment code
rseg                HX710ROM
```

```
sbit            ADDO = P1.5;
sbit            ADSK = P0.0;

/ * ------------------------------------------------ -OUT: R4, R5, R6, R7
                                        R7 => LSB
  If you call in C, you can not be modified R4, R5, R6, R7.
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - * /
ReadAD:
    CLR     ADSK                  // Enable AD (PD_SCK low position)
    SETB ADDO                     // 51CPU quasi-bidirectional I / 0 Input Enable
    JB      ADDO, $               // determine the AD conversion is completed, if not the end of the wait or start reading
    MOV     R4, # 24
ShiftOut:
    SETB ADSK                     // PD_SCK high (transmission pulses)
    NOP
    CLR     ADSK                  // PD_SCK set low
    MOV     C, ADDO               // read the data (one bit)
    XCH     A, R7                 // move data
    RLC     A
    XCH     A, R7
    XCH     A, R6
    RLC     A
    XCH     A, R6
    XCH     A, R5
    RLC     A
    XCH     A, R5
    DJNZ R4, ShiftOut              // determine whether the move 24BIT
    SETB ADSK NOP CLR

            ADSK
    RET END
```

Reference drivers (C)

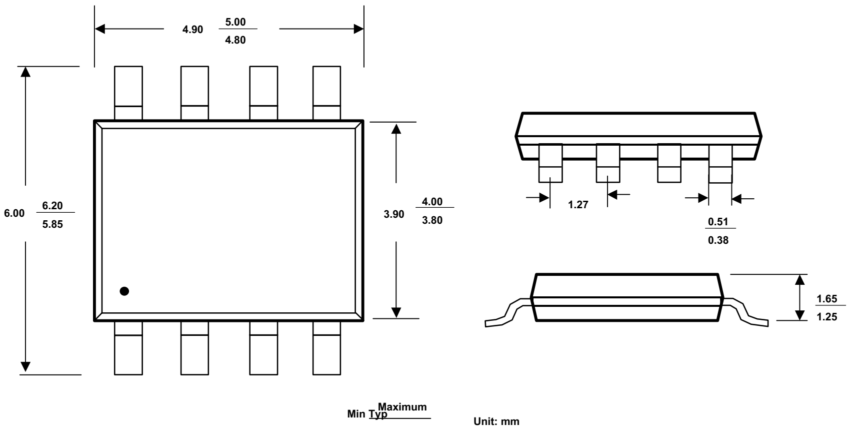
```
sbit     ADDO = P1 ^ 5; sbit
         ADSK = P0 ^ 0;
unsigned long ReadCount (void) {
  unsigned long Count; unsigned
  char i; ADDO = 1;
                        51 @ Non-class MCU, this line is omitted
  ADSK = 0; Count = 0; while
  (ADDO); for (i = 0; i <24; i ++) {


    ADSK = 1;
    Count = Count << 1; ADSK
    = 0;
    if (ADDO) Count ++;}

  ADSK = 1;
```

Count = Count ^ 0x800000; ADSK =

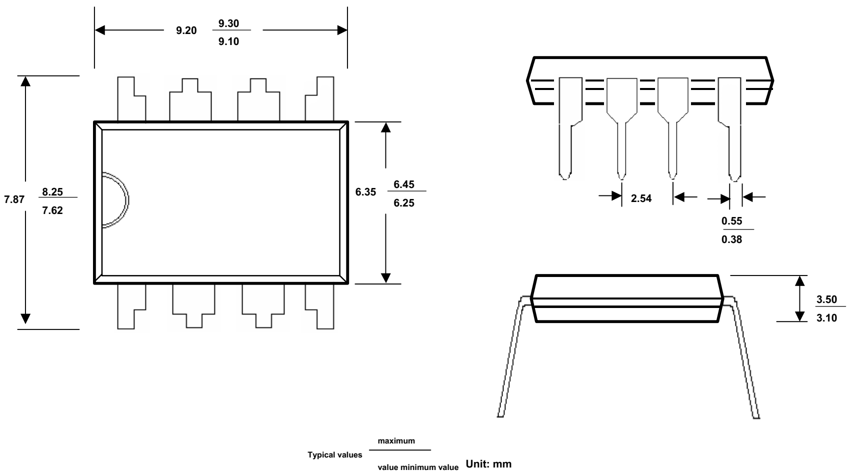
0;

return (Count);}

Package size



SOP-8L Package



DIP-8 Package