

Diagram illustrating a 16-bit shift register (S = 15) and its output (i = 16). The register contains the sequence: 0 1 2 3 4 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 4 0 1 2 3 A B C D... The first six bits (0 1 2 3 4 0) are grouped by a grey bracket. The next six bits (0 1 2 3 4 5) are grouped by a red bracket. The output i = 16 is connected to the input of the first bit (0).

Diagram illustrating a 16-bit shift register configuration. The register is represented as a sequence of 16 cells, indexed 0 to 15. The current state of the register is shown as a sequence of values: 0, 1, 2, 3, 4, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 4, 0, 1, 2, 3, A, B, C, D, ...

The register is divided into three sections:

- Section 1 (Cells 0-5):** Indicated by a grey bracket above and a blue bracket below. The values are 0, 1, 2, 3, 4, 0.
- Section 2 (Cells 6-11):** Indicated by a red bracket below. The values are 1, 2, 3, 4, 5, 6.
- Section 3 (Cells 12-15):** The values are 7, 8, 9, 0.

Input and Output:

- Input:** A black arrow labeled $S = 15$ points to the input of the first cell (index 0).
- Output:** A black arrow labeled $i = 16$ points to the output of the first cell (index 0).

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Diagram illustrating a 16-bit shift register configuration. The register is represented as a sequence of cells, with indices 0 to 15. The current state of the register is shown as a sequence of values: 0, 1, 2, 3, 4, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 4, 0, 1, 2, 3, A, B, C, D, ...

The register is divided into three sections:

- Section 1 (Indices 0-5):** Grouped by a grey bracket above and a blue bracket below. The values are 0, 1, 2, 3, 4, 0.
- Section 2 (Indices 6-11):** Grouped by a red bracket below. The values are 1, 2, 3, 4, 5, 6.
- Section 3 (Indices 12-15):** Individual cells. The values are 7, 8, 9, 0.

Input and Output:

- Input:** A black arrow labeled $S = 15$ points to the first cell (index 0).
- Output:** A black arrow labeled $i = 16$ points to the first cell (index 0).

Diagram illustrating a 16-bit shift register (S = 15) and its output (i = 16). The register contains the sequence: 0 1 2 3 4 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 4 0 1 2 3 A B C D... The first six bits (0 1 2 3 4 0) are grouped by a grey bracket. The next six bits (0 1 2 3 4 5) are grouped by a red bracket. The output i = 16 is connected to the input of the first bit (0).

Diagram illustrating a 16-bit shift register configuration for a linear feedback shift register (LFSR). The register is labeled $S = 15$ at the top left. The output is labeled $i = 16$ at the bottom center. The register contains the sequence: 0 1 2 3 4 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 4 0 1 2 3 A B C D... The first six bits (0 1 2 3 4 0) are grouped by a grey bracket. The next six bits (0 1 2 3 4 5) are grouped by a red bracket. The output bit is the 16th bit, which is 0. The feedback loop connects the output bit to the input of the first bit (0). The input of the first bit is labeled 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15. The input of the 16th bit is labeled 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15.

Diagram illustrating a 16-bit shift register (S = 15) and its output (i = 16). The register contains the sequence: 0 1 2 3 4 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 4 0 1 2 3 A B C D... The first six bits (0 1 2 3 4 0) are grouped by a grey bracket. The next six bits (0 1 2 3 4 5) are grouped by a red bracket. The output i = 16 is connected to the input of the first bit (0).