

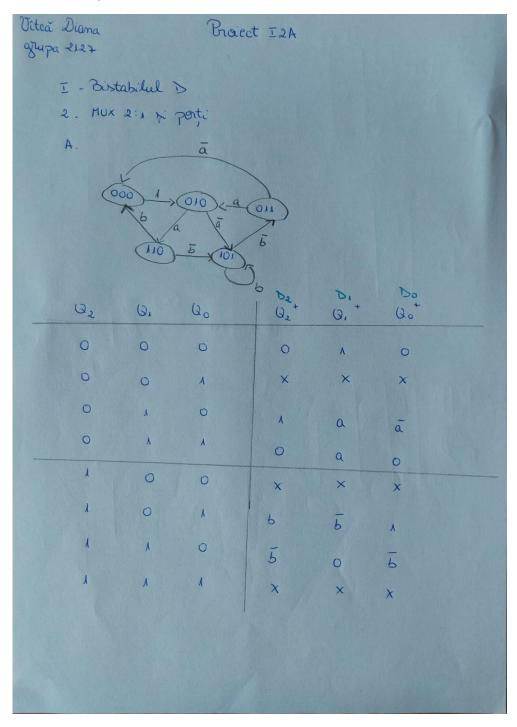
Proiect SCID 12A

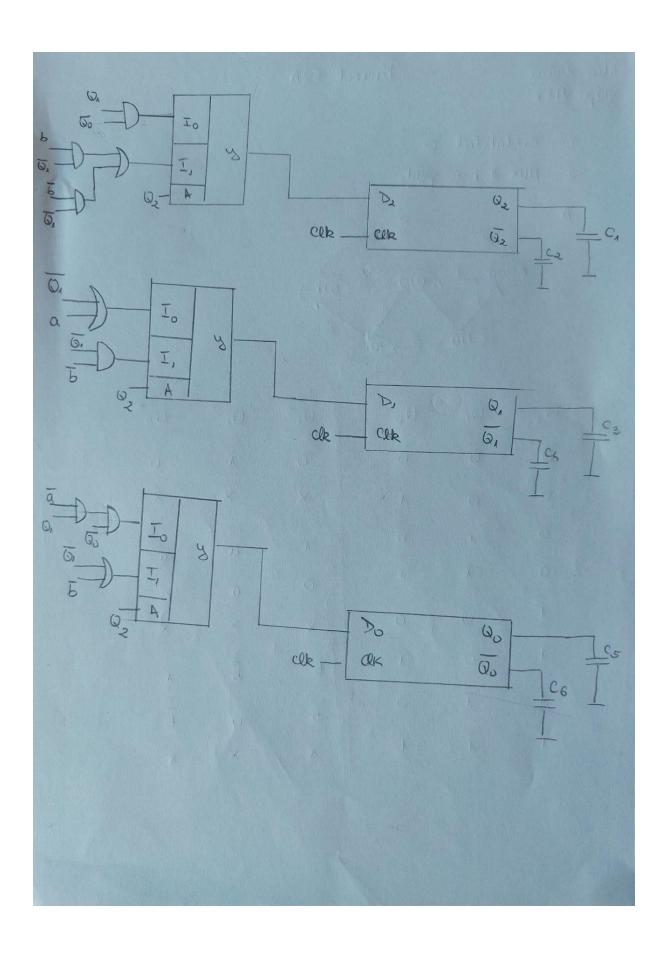
Vîtcă Diana-Nicoleta

Grupa 2127

Seria B

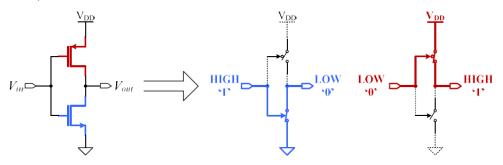
1. Rezolvarea pe hârtie





2. Implementarea inversorului CMOS

a) Schema electrică la nivel de tranzistor



io

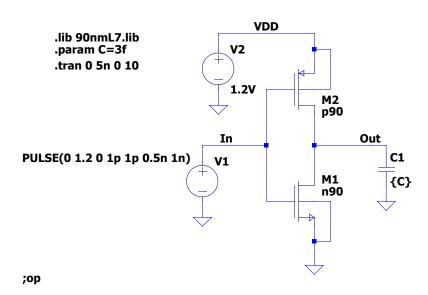
а	$f = \bar{a}$
0	1
1	0

Formalismul de reprezentare al nivelelor logice este

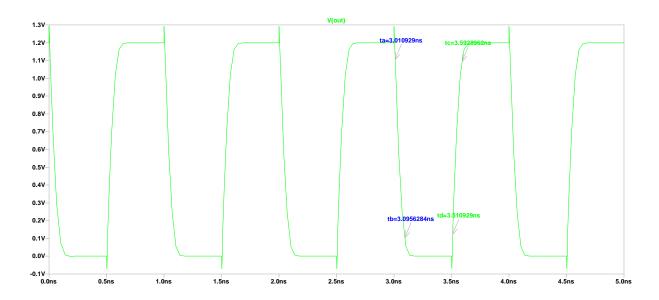
1 logic → nivel de tensiune HIGH, se obţine printr-un scurt-circuit la VDD

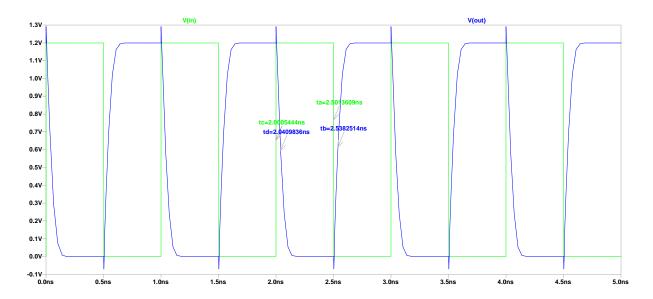
0 logic → nivel de tensiune LOW, se obţine printr-un scurt-circuit la GND

b) Circuitul de test cu verificarea funcționării



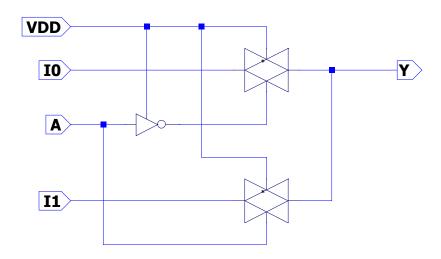
c) Măsurarea timpilor de tranziție și a timpului de propagare.



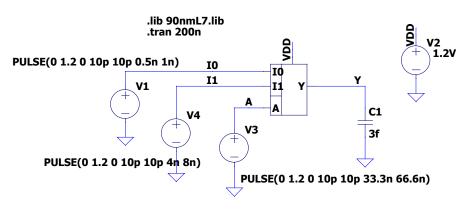


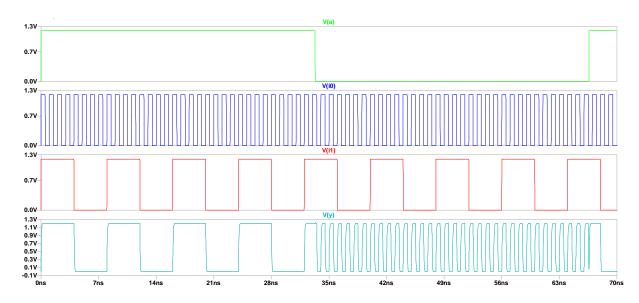
3. Circuit combinational

a) Schemă electrică mux21.asc



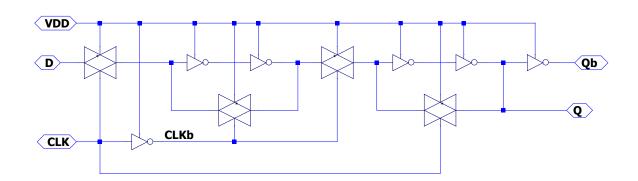
b) Circuitul de test cu verificarea funcționării test_mux21.asc



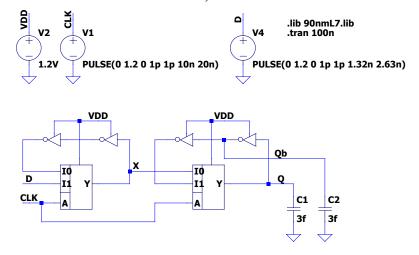


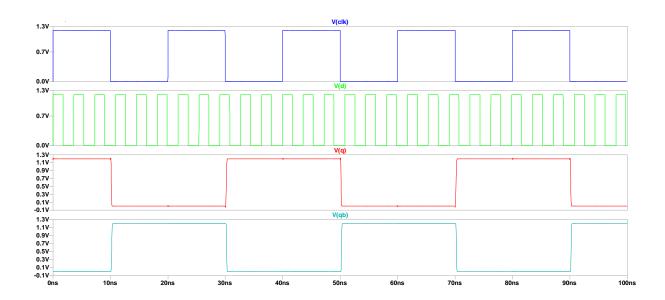
4.Circuitul secvential

a) Schemă electrică dff.asc



b) Circuitul de test cu verificarea funcționării test_dff.asc





5. Implementarea finală

a) Schema finală a automatului implementare_finala.asc

