ECN3053F

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3-Phase Motor Bridge Driver IC

The ECN3053F drives a 3-Phase Motor Bridge with 3 TOP and 3 BOTTOM Arms, Push-Pull Output Drivers controlled by 6 CMOS inputs. Built in a High Voltage Dielectric Isolation Process, this Latch-Up Free IC can directly drive 6 IGBT or MOSFET gates in 3-Phase Brushless DC and Induction Motor Bridges. The TOP Arms can Boot Strap bias at up to 620VDC (Breakdown). An on-chip OpAmp allows Custom, Low, Over Current (OC) trip voltages so as to minimize Sense Resistor power dissipation in High Wattage applications. The TOP and BOTTOM Arms are Under Voltage (UV) protected.

Description

- 3-Phase TOP Arm Boot Strap Bias (620VDC Breakdown)
- TOP and BOTTOM Arm gate drive outputs are Push-Pull
- TOP and BOTTOM Arms can switch at up to 20kHz
- Latch-Up Free IC built in a High Voltage Dielectric Isolation Process

Functions and Features

- TOP and BOTTOM 3-Phase Drive via CMOS Logic inputs
- Over Current (OC) Protection
- OpAmp allows Custom (Low) trip voltage on OC Sense Resistor
- TOP & BOTTOM Arm Under Voltage (UV) Protection
- Fault Output Signal reports OC and low Vcc conditions
- On-Chip 7.5VDC regulator (CB) with guaranteed Min load (15mA)

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Block Diagram

Figure 1 Block Diagram

Part Name and Packaging

FP-28DJ(JEDEC)

ECN3053F
(Package Type:FP-28DJ)
(JEDEC)

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1. General

This specification shall be applied to the following semiconductor integrated circuits.

1) Type: ECN3053F

2) Application: 3-Phase Brushless DC Motor; 3-Phase Induction Motor

3) Structure: Monolithic IC

4) Package: FP-28DJ(JEDEC)

2. Maximum Allowable Ratings

Ta = 25 °C

	ITEM	SYMBOL	UNIT	VALUES	CONDITIONS
1	Output breakdown voltage	Vbv	V	620	Between Vcu, cv, cw and GL1
2	A+(GL2) OpAmp input	Vgl2	V	-5 to Vcc	Vcc = 18V max at A+(GL2) = -5V
3	U,V,W pin voltage	Vu, v, w	V	-5 to 600	
4	Supply voltage	Vcc	V	20	
5	Input voltage	Vin	V	-0.5 to Vcc+0.5	
6	Junction Operating Temperature	Tjop	C	-20 to 125	
7	Storage Temperature	Tstg	C	-40 to 150	

Thermal Resistance Rja

PACKAGE	FP-28DJ(JEDEC)	UNIT
Isolated	121	°C/W
Mounted	84	°C/W
PCB size (wiring density)	12.0x21x1.6 (30%)	mm

General Note: Please refer to the "Precautions for Use" on our website.

3. Electrical Characteristics

Unless otherwise noted, Ta = 25°C, u,v,w to GL1 = 374V, Vcc = 15V (suffix T = Top, B = Bottom Arm)

	ITEM		SYMBOL	UNIT	MIN	TYP	MAX.	CONDITIONS
1	StandBy current		Is1	mA	-	6.5	10	Vin = H or L, Between Vcc - GL1
			Is2	µA	-	15	30	Between Vcu-U, Vcv-V, Vcw-W = 15V, Vin = H or L
2	Input Voltage (Output Switches OFF)		VIH	V	3.5	-	-	Vin = H or L
	Input Voltage (Output Switches ON)		VIL	V	-	-	1.5	
3	Output Source Current		Io+	A	0.2	0.25	-	Vcu-PGU, Vcv-PGV, Vcw-PGW = 15V, Vcc - NGU,V,W = 15V, PW < 10µs
4	Output Sink Current		Io-	A	0.4	0.5	-	PGU-U, PGV-V, PGW-W = 15V, NGU,V,W - GL2 = 15V, PW < 10µs
5	High level Output Voltage		VOH	mV	-	-	100	Vcu,cv,cw - PGU,V,W & Vcc - NGU,V,W Vin = 0, Io = 0
6	Low level Output Voltage		VOL	mV	-	-	100	PGU,V,W - U,V,W & NGU,V,W - GL2 Vin = 5V, Io = 0
7	Leakage Current at HV pin		IL	µA	-	-	50	Vcu,cv,cw = U,V,W = 600V
8	Input Current		IIL	µA	-200	-	-	Vin = 0V Internal Pull Up R = 200kΩ
9	Input Current		IIH	µA	-120	-	-	Vin = 5V Internal Pull Up R = 200kΩ
10	Vcc Under Voltage	Negative Going	Vuvb	V	9.5	10.5	11.6	
	BOTTOM Arm	Reset Hysteresis	Vrhb	V	0.1	-	0.9	
11	Vcu, cv, cw Under Voltage	Negative Going	Vuvt	V	8.9	10.5	12.1	
	TOP Arm	Reset Hysteresis	Vrht	V	0.1	-	0.9	
12	OC Input Positive Going Threshold		Voc	V	0.44	0.49	0.54	
13	Fault Output ON Resistance		Ronf	Ω	-	300	400	F - GL1 = 0.5V
14	Turn-On Delay Time		ton	µs	-	0.8	1.5	CL = 1000pF RL = 0
15	Turn-Off Delay Time		toff	µs	-	0.5	1.2	CL = 1000pF RL = 0
16	OC Output to Output Shutdown Delay		toc	µs	-	0.7	1.7	CL = 1000pF RL = 0
17	OC to Fault Delay		tflt	µs	-	0.6	1.6	CL = 1000pF RL = 0
18	Fault Reset Delay Time		Tflrs	µs	6.5	10	20	CL = 1000pF RL = 0
19	Fault Output terminal Voltage		Vflt	V	-0.5	-	Vcc + 0.5	
20	Fault Output Sink Current		Iflt	mA	4	-	-	Vcc = 15V, F-GL = 2V
21	VB Output Voltage		VB	V	6.8	7.5	8.2	
22	VB Output Current		IB	mA	15	20	-	Delta Vload = 0.1V
23	Op-Amp Input Offset Voltage		Vos	mV	-	-	30	A+(GL2) = A- = 0.2V
24	Op-Amp High Level Output Voltage		VOHa	V	5.0	7.5	-	A- = 0V A+(GL2) = 1V
25	Op-Amp Low Level Output Voltage		VOLa	mV	-	-	20	A- = 1V A+(GL2) = 0V
26	Op-Amp Output Source Current		Isrca	mA	1.0	-	-	A- = 0V A+(GL2) = 1V AO = 4V
27	Op-Amp Output Sink Current		Isnka	mA	1.0	-	-	A- = 1V A+(GL2) = 0V AO = 2V

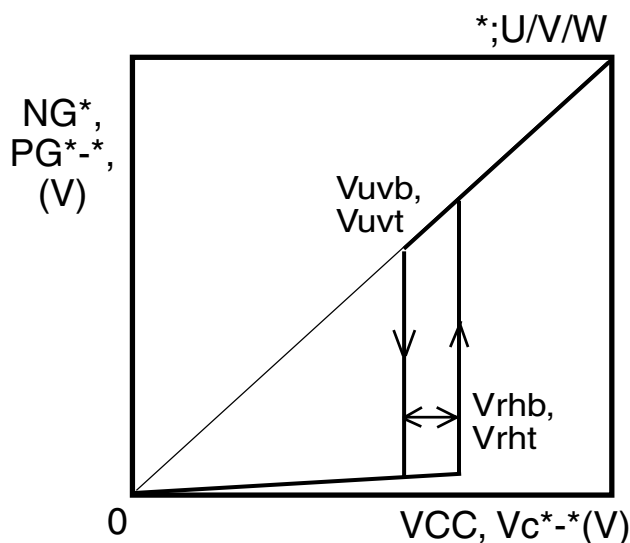Note: Vuvb, Vrhb, Vuvt and Vrht are defined and shown in Fig. 2.

Figure 2. Negative going and reset voltage and hysterisis
for the Top and Bottom Arm Under Voltage circuit.

4. Recommended Operating Conditions

	ITEM	SYMBOL	UNIT	VALUE / TOL	REMARKS
1	Power Supply Voltage	Vcc	V	13.5 to 16.5	
2	PWM Frequency	Fpwm	kHz	1 to 20	
3	VB Smoothing Capacitor	Co	μF	≥ 0.22	Stress voltage = VB
4	Boot Strap Capacitor	Cb	μF	≥ 3.3	Stress voltage = Vcc
5	Boot Strap Diode	Db		Hitachi DFG1C6 DFM1F6 or equivalent	600V / ≥ 1.0A trr ≤ 0.1μs
6	OC Sense Resistor	Rs	Ω	Note 1	
7	OC Filter Resistor	R1	Ω	Note 2	
8	OC Filter Capacitor	C1	μF	Note 2	
9	Load resistor for pin F	Rf	kΩ	≥ 5.6	

Note 1. Over Current detection level is determined by the following equation:
$I_{oc} = V_{oc}/RS$; Where the Tolerances of Voc and RS must be applied.

Note 2. The ECN3053F has an internal 0.4us filter to reduce noise. But, an appropriate filter [R1, C1] should be added if application noise necessitates further removal.

5. Truth Table

INPUT		OC Input	U Phase		V Phase		W Phase	
			TOP Arm	BOT Arm	TOP Arm	BOT Arm	TOP Arm	BOT Arm
SUT	L		ON	-	-	-	-	-
	H		OFF	-	-	-	-	-
SUB	L		-	ON	-	-	-	-
	H		-	OFF	-	-	-	-
SVT	L		-	-	ON	-	-	-
	H		-	-	OFF	-	-	-
SVB	L	L	-	-	-	ON	-	-
	H		-	-	-	OFF	-	-
SWT	L		-	-	-	-	ON	-
	H		-	-	-	-	OFF	-
SWB	L		-	-	-	-	-	ON
	H		-	-	-	-	-	OFF
-	-	H	OFF	OFF	OFF	OFF	OFF	OFF
SUT, SUB	L	-	OFF	OFF	-	-	-	-
SVT, SVB	L	-	-	-	OFF	OFF	-	-
SWT, SWB	L	-	-	-	-	-	OFF	OFF

Note 1: Fault output level is referenced Low when Over Current or Under Voltage for Vcc is detected.

Note 2: Over Current protection works when the voltage drop of the external sense resistor exceeds the threshold voltage Voc (typical 0.49V). In this case all six outputs are turned OFF and Fault output level goes Low. Reset after OC is done via a High signal to all six inputs (or re-supplying the Vcc voltage).

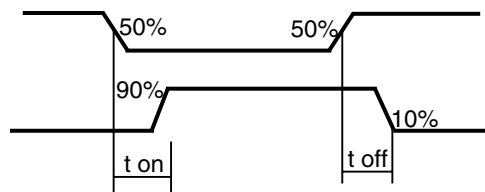Note 3: The Fault output signal is Reset by applying a High signal to all six inputs.

6. Definition of switching delay

Input
(SUB,T   SVB,T   SWB,T)
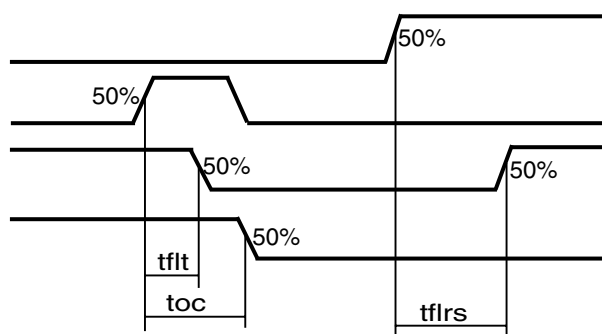Output
(PGU,V,W   NGU,V,W)
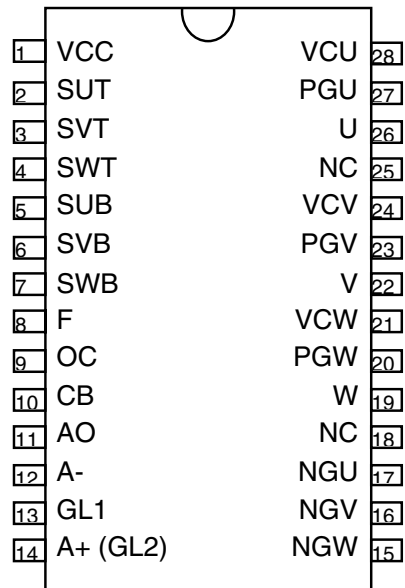

Input
(SUB,T   SVB,T   SWB,T)

OC

F

Output
(PGU,V,W   NGU,V,W)

6

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7. Pinout

1	VCC	VCU	28
2	SUT	PGU	27
3	SVT	U	26
4	SWT	NC	25
5	SUB	VCV	24
6	SVB	PGV	23
7	SWB	V	22
8	F	VCW	21
9	OC	PGW	20
10	CB	W	19
11	AO	NC	18
12	A-	NGU	17
13	GL1	NGV	16
14	A+ (GL2)	NGW	15

8. Pin Definitions

Pin #	Symbol	Pin Definition
1	Vcc	External Analog Power Supply (15VDC +/- 10%)
2	SUT	Phase U TOP Arm control signal (CMOS logic input)
3	SVT	Phase V TOP Arm control signal (CMOS logic input)
4	SWT	Phase W TOP Arm control signal (CMOS logic input)
5	SUB	Phase U BOTTOM Arm control signal (CMOS logic input)
6	SVB	Phase V BOTTOM Arm control signal (CMOS logic input)
7	SWB	Phase W BOTTOM Arm control signal (CMOS logic input)
8	F	Fault output signal reports OC and LOW Vcc conditions
9	OC	Over Current detection (analog input) from Ext. Sense Resistor or Int. Op-Amp
10	CB	Internally regulated (VB) 7.5V Output Pin (External 15mA guarantee)
11	AO	Op-Amp Output voltage
12	A-	Op-Amp Input voltage
13	GL1	Analog ground
14	A+(GL2)	Op-Amp Input voltage
15	NGW	BOTTOM Arm Gate Drive for Phase W
16	NGV	BOTTOM Arm Gate Drive for Phase V
17	NGU	BOTTOM Arm Gate Drive for Phase U
18	NC	No Connection
19	W	Phase W TOP Arm return ("ground") reference rail
20	PGW	Phase W TOP Arm gate drive Push-Pull output
21	VCW	Phase W TOP Arm Boot Strap summing point via external capacitor Cb
22	V	Phase V TOP Arm return ("ground") reference rail
23	PGV	Phase V TOP Arm gate drive Push-Pull output
24	VCV	Phase V TOP Arm Boot Strap summing point via external capacitor Cb
25	NC	No Connection
26	U	Phase U TOP Arm return ("ground") reference rail
27	PGU	Phase U TOP Arm gate drive Push-Pull output
28	VCU	Phase U TOP Arm Boot Strap summing point via external capacitor Cb

<u>9. Quality Assurance</u>

  9.1 Appearance and dimension
     ANSI Z1.4-1993 General inspection levels II AQL 1.0%
  9.2 Electrical characteristics
     ANSI Z1.4-1993 General inspection levels II AQL 0.65%

<u>10. Do's and Don'ts</u>

10.1 To protect this chip from Electrical Static Discharge (ESD), the ECN3053F should be handled in accordance with normal industry standard procedures for protection against damage due to ESD. For a more detailed discussion of this area, please refer to the web, "Precautions for Use" Section 5.

10.2 Depending on local industry/market regulations, conformal coating may be required for the following pin-to-pin spacings: 17-19, 21-22, 24-26.

10.3 Protective function against short circuit (ex. load short, line-to-ground short or TOP/BOTTOM Arm shorts) is not built into this IC. External protection may be needed to prevent IC breakdown under these potential application conditions.

10.4 Hitachi high voltage ICs are manufactured to meet standard industrial grade reliability specifications. In cases where extremely high reliability is required (such as nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment) system integrity must be achieved via fail-safe system design. Additionally, it is the responsibility of the designer to insure that any IC failure does not damage property or human life. Users should evaluate and consider employing the following design precautions:
  a) Sufficient derating of the specifications should be utilized to minimize the possibility of failures based on the maximum ratings, operating temperature and environmental conditions.
  b) Design redundancy should be applied so that application performance will be maintained even in a case of IC failure.
  c) The system design should implement fail-safe design techniques to protect property and human life even where incorrect system operation is experienced.

11. Precautions for Safe Use

If semiconductor devices are handled in an inappropriate manner, failure may result. For this reason, be sure to read "Precautions for Use" on our website before use.

⚠ **CAUTION**

(1). Regardless of changes in external conditions during use, "absolute maximum ratings" should never be exceeded in designing electronic circuits that employ semiconductors.
Furthermore, in the case of pulse use, "safe operating area (SOA)" precautions should be observed.

(2). Semiconductor devices may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features and practices, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of failure.

(3). In cases where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support related medical equipment, fuel control equipment and various kinds of safety equipment), safety should be ensured by using semiconductor devices that feature assured safety or by means of user's fail-safe precautions or other arrangement. Or consult Hitachi's sales department staff.

(If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

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12. Notices

1. This publication contains the specifications, characteristics (in figures and tables), dimensions and handling notes concerning power semiconductor products (hereinafter called "products" to aid in the selection of suitable products.

2. The specifications and dimensions, etc. stated in this publication are subject to change without prior notice to improve product's characteristics. Before ordering, purchasers are advised to contact Hitachi's sales department for the latest version of this publication and specifications.

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Appendix - Supplementary and Reference Data

1. An On-Chip differential Op-Amp to Customize Over Current (OC) protection

An On-Chip differential Op-Amp can be externally connected in a standard, non-inverting (positive) gain configuration, where the Voltage Gain is defined as:

Voltage Gain = **1** + (**R2** / **R1**)   **Equation A.1**

Thus, it is possible to produce the necessary OC trip voltage (typically 0.49VDC) in High Wattage applications where it may also be **desirable to use less than 0.49VDC** across that external OC Sense Resistor and, in so doing, minimize the power dissipated by that Sense Resistor passing **Im**. The power dissipated in the external Sense Resistor is:

Power Dissipated in RS = (**Im**) x (**V[RS]**)   **Equation A.2**

As an example, suppose we want 0.20VDC to represent the OC trip point. Then:

V[OC] = (Voltage Gain) x (**V[RS]**)   **Equation A.3**

Voltage Gain = **1** + (**R2** / **R1**) = (**V[OC]**) / (**V[RS]**) = 0.49 / 0.20

Voltage Gain = **1** + (**R2** / **R1**) = 2.45
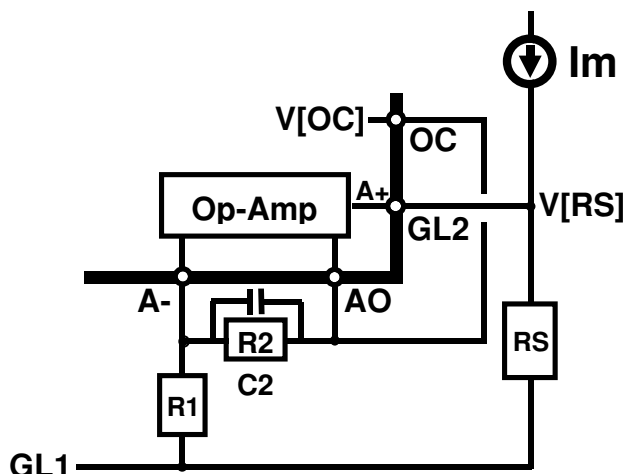
R2 / **R1** = 2.45 - **1** = 1.45

Figure 3. Using the Op-Amp to scale OC trip voltage

Given the Op-Amp current spec (3. Electrical Characteristics, lines 26 & 27), of 1.0mA (guaranteed) Min and, Op-Amp output voltage limited by the CB voltage (8.2VDC Max), the minimum value of R2 (8.2V / 1.0mA) is 8.2Kohms. Thus, a practical range for R2 is 10K to 20K Ohms. C2 can be used as a noise filter depending on application conditions but, recognize C2 can only reduce the (high frequency) voltage gain down to unity (1).

Going back to Equation A.2 and, using the 0.20VDC (**V[RS]**) OC trip voltage:

Power Dissipated in RS = (**Im**) x (**V[RS]**) = (**Im**) x (0.2) **Watts**

With a typical NA Appliance OC of 12 Amp, the sense resistor dissipates 2.4 Watts. Without an Op-Amp, i.e., with **V[RS]** = 0.49VDC, this would normally be 5.9 Watts. Likewise, using **V[RS]** = 0.10VDC, the sense resistor would dissipate only 1.2 Watts at 12 Amps (instead of 5.9 Watts at the normal 0.49VDC reference value).

2. Package Dimensions
      1) ECN3053F