



*General-Purpose
3-Phase AC Industrial
Motor Controller*

*Designer Reference
Manual*

*MC3PHAC
Motor Controller*

DRM006/D
4/2002

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General-Purpose 3-Phase AC Industrial Motor Controller Reference Design

Designer Reference Manual

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Section 1. Introduction and Setup

1.1 Contents

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1.2 Introduction

Motorola's MC3PHAC motor control reference PC board is designed for use with optoisolation and power modules that are an integral part of the embedded motion control series of development tools. It may be used with custom power stages as well, and it is intended as a vehicle to evaluate the MC3PHAC motor control device. The MC3PHAC is designed to provide all of the necessary pulse-width modulated outputs and monitor the system parameters necessary to control a 3-phase induction motor. The reference PC board interfaces easily with power stages and optoisolator boards. Details of the interface are given in **Section 3. Pin Descriptions**. A photograph of the board is shown in **Figure 1-1**.

Some applications for this system include:

- Low horsepower, variable-speed HVAC compressors, blowers, and air handler motors
- Garage door openers
- Variable-speed pumps
- Submersible pumps

- Soft-start drive systems
- Hot tub pump motors
- Commercial laundry and dishwashers
- Process control systems
- Variable speed refrigeration compressors

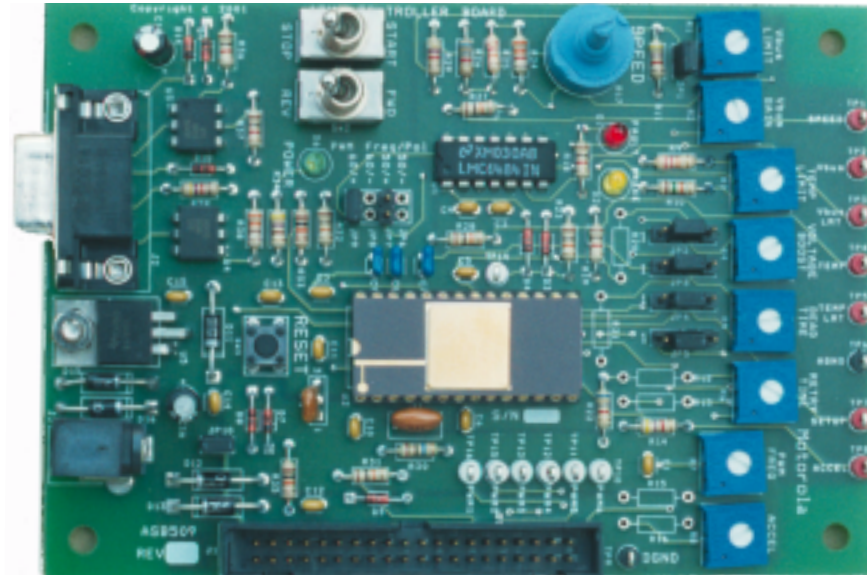


Figure 1-1. Board Photograph

1.3 Brief Overview to 3-Phase Induction Motors

Various market studies indicate up to 90 percent of all industrial motor applications are induction type motors. Induction motors are sometimes referred to as the “workhorse” of industrial motors. An induction motor is the lowest cost motor for applications that require one-third or more horsepower when some form of ac is available. This is true partly because of the simple design of an induction motor. Three-phase motors are becoming more popular for consumer applications as well. There are many reasons for using an induction motor. Some of the reasons are:

- Low cost
- Simple to construct
- High reliability

- High efficiency
- No brushes to wear out
- Operate well in extreme temperature conditions
- Minimum maintenance

In the case of the system described in this document, the ac power for the 3-phase induction motor is generated by an inverter, driven from a pulse-width modulator (PWM) within the MC3PHAC controller.

These advantages do not come without a price. An induction motor's speed is difficult to control due to its complex mathematical model and its non-linear behavior when its core is saturated. Semiconductor-based control systems have enabled the use of induction motors for many applications requiring speed control.

Induction motors are available in a wide range of sizes, from less than one watt to thousands of kilowatts. Common input voltage ranges are 230 and 460 volts for 60 Hz and input voltages of 380 volts when operating at 50 Hz.

The motors are available in a variety of mounting styles. Mounting styles include C-face, foot mount, large flange, vertical, and custom mounts. Depending on the environment where the motor will reside, open, explosion proof, totally enclosed, fan-cooled, water-cooled, blower-cooled, and other enclosures are available.

An ac induction motor consists of two windings. The windings are the rotor and stator assemblies. An induction motor can be thought of as a transformer with a fixed primary (stator) and a rotating secondary (rotor). The motor's name "induction" comes from the fact that alternating currents are induced from the stator into the rotor by the rotating magnetic flux produced in the stator. The motor's torque is developed from the interaction of the currents flowing in the rotor and the stator's rotating magnetic field. The stator, or primary, windings connect to the 3-phase voltage source to produce a rotating magnetic field. The stator structure is constructed with steel laminations shaped to form poles that are wound with copper wire coils. The rotor is an assembly of laminations over a steel shaft core. Radial slots around the laminations periphery house copper or aluminum conductors at one end and are

positioned in parallel to the shaft. The primary windings are connected to a 3-phase power source which produce a rotating magnetic field. In the case of a 3-phase induction motor, the primary or stator windings are spaced physically 120 degrees apart. If you view the rotor from one end, it appears to look like a squirrel cage. Sometimes an induction motor is referred to as a squirrel cage induction motor.

Figure 1-2 shows a schematic view of the construction of a 3-phase ac induction motor.

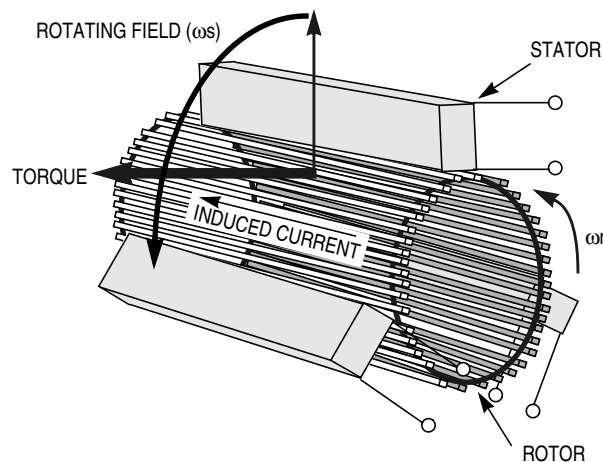


Figure 1-2. Schematic View of a 3-Phase AC induction Motor

The magnetic field in the stator rotates at a synchronous speed around the parameter of the stator with the applied power's frequency. The speed of an ac induction motor is controlled by the following factors:

- The number of poles (winding sets) built into the motor
- The frequency of the ac line voltage
- The amount of torque loading, which causes slippage

In actual practice, the rotor speed of the motor will always lag the rotating magnetic field of the stator. Typical slip values range from 2 percent to 5 percent of the theoretical rotational speed. Slip will always increase with the applied loading of the motor.

To put the rotation speed in equation form, the theoretical speed of the motor shaft is $V_s = 120$ (input frequency/number of poles). For a 60-Hz fixed frequency and a motor with four poles, the theoretical speed would be 1800 rpm. However, taking slip into consideration, using 4 percent slip, the actual speed of the motor would be 1728 rpm.

A number of techniques can be used to control an ac induction motor. Ac induction motor drives are based on the fact that variable frequency and variable voltage waveforms can be generated. The most common ac induction motor drive utilizes a converter-inverter structure as shown in **Figure 1-3**.

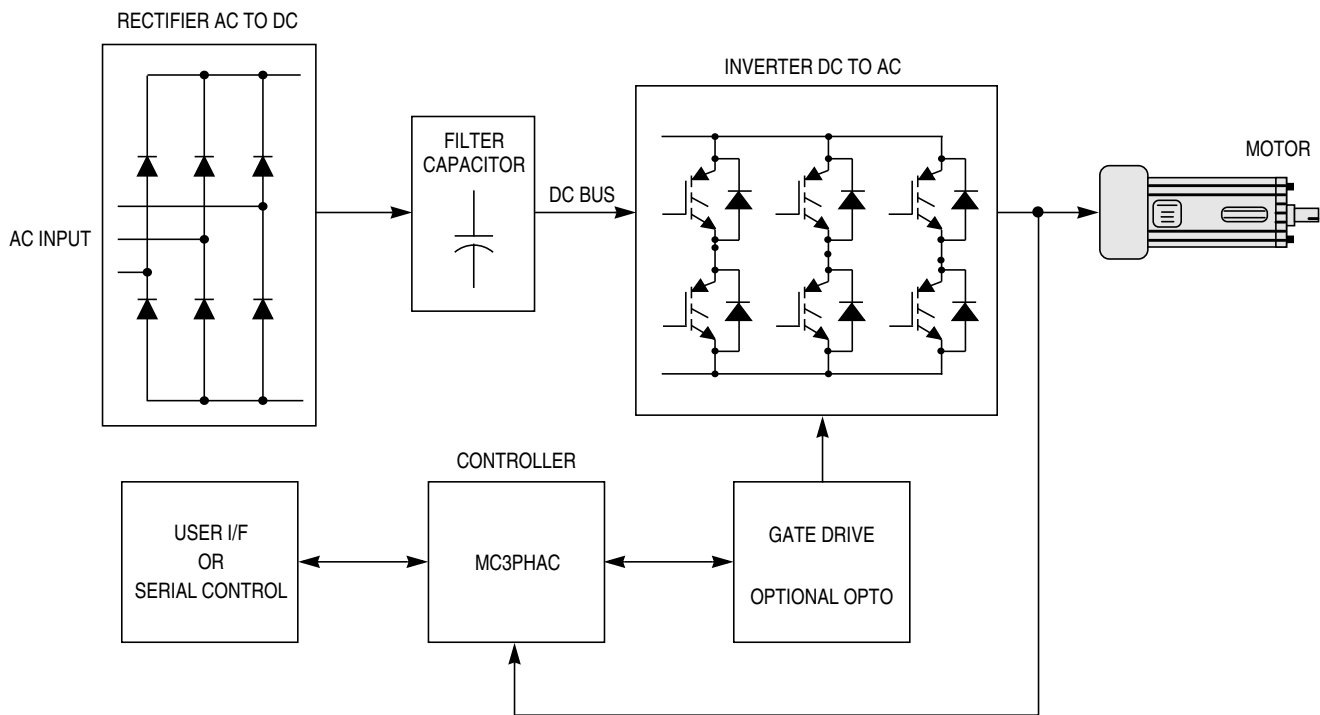


Figure 1-3. 3-Phase AC Motor Drive

As shown in **Figure 1-3**, the rectifier creates dc from the ac line while the inverter develops the variable-frequency, variable-voltage ac voltage from the dc bus. The controller is the intelligent heart of the system. It provides pulse-width modulated outputs used to drive the gate drive to the inverter. The controller also provides some form of user input/output (I/O) and reads the bus voltage and uses system fault information during its control tasks. Some systems optionally optoisolate the controller from the gate drives.

Many excellent text and reference books describe motors and their control techniques. A list containing several of them is presented here:

- *Motor Control Electronics Handbook*, by Richard Valentine, McGraw-Hill, 1998, ISBN 0-07-066810-8
- *DC Motors, Speed Controls, Servo Systems*, by Electro-Craft Corp., 1980, ISBN 0-9601914-0-2
- *Electric Machinery*, by A. E. Fitzgerald, Charles Kingsley Jr., and Stephen D. Umans, McGraw-Hill, 1990, ISBN 0-07-021134-5
- *Vector Control of AC Machines*, by Peter Vas, Oxford University Press, 1994, ISBN 0-19-859370-8
- *Power Electronics*, by Ned Mohan, Tore Undeland, and William Robbins, John Wiley & Sons, 1995, ISBN 0-471-58408-8
- *Power Electronics and Variable Frequency Drives*, edited by Bimal Bose, IEEE Press, 1997, ISBN 0-7803-1084-5
- *Electric Drives, an Integrative Approach*, by Ned Mohan, University of Minnesota Printing Services, 2000, ISBN 0-9663530-1-3

1.4 About this Manual

Key items can be found in the following locations in this manual:

- Setup instructions are found in [1.7 Setup Guide](#).
- Schematics are found in [Section 4. Schematics and Parts List](#).
- Pin assignments are shown in [Figure 3-1. 40-Pin Ribbon Connector J1](#), and a pin-by-pin description is contained in [3.3 Control Board Signal Descriptions](#).
- For those interested in the reference design aspects of the board's circuitry, a description is provided in [Section 5. Design Considerations](#).

1.5 Features

Some of the more noteworthy features of the reference PC board are:

- Six motor control PWM outputs
- Speed control potentiometer
- Optoisolated half-duplex RS232 interface
- Start/stop and forward/reverse switches
- Eight jumper headers for system setup
- MC3PHAC RESET switch
- Two system fault inputs
- Four analog inputs
- Two software controlled LEDs
- Regulated on-board power supply

The reference PC board fits into the system's configuration that is shown in **Figure 1-4**.

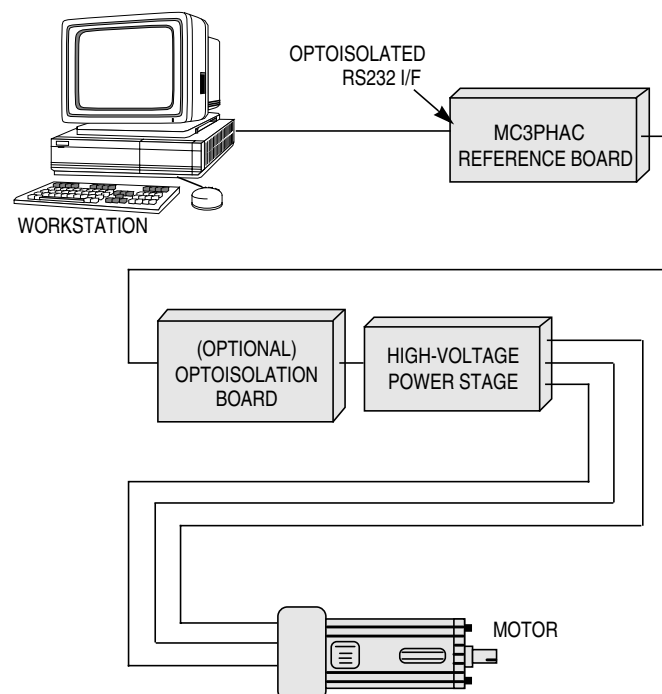


Figure 1-4. System's Configurations

1.6 Warnings

This MC3PHAC reference PC board operates in an environment that includes dangerous voltages and rotating machinery.

To facilitate safe operation, input power for the high-voltage power stages should come from a current limited dc laboratory power supply. If ac power is applied directly to the power stage, an isolation transformer should be used.

When operating high-voltage power stages directly from an ac line, power stage grounds and oscilloscope grounds are at different potentials, unless the oscilloscope is floating. Note that probe grounds and, therefore, the case of a floated oscilloscope, are subjected to dangerous voltages.

- Before moving scope probes, making connections, etc., you must power down the high-voltage supply.
- When high voltage is applied to the high-voltage power stage, using only one hand for operating the test setup minimizes the possibility of electrical shock.
- Operation in lab setups that have grounded tables and/or chairs should be avoided.
- Wearing safety glasses, avoiding ties and jewelry, using shields, and operation by personnel trained in high-voltage lab techniques are also advisable.

1.7 Setup Guide

Setup for and connections to the MC3PHAC reference PC board are straight forward. Output connections to an embedded motion control optoisolation board or high-voltage power stage are made via a 40-pin ribbon cable. The optoisolation board and power stage referred to in this manual ship as a set and can be ordered from Motorola or distribution partners as part number ECOPTHIVACBLDC.

The reference PC board is powered through the 40-pin ribbon cable, regardless of whether it is connected to the optoisolation board or connected directly to a high-voltage power stage. A 12-volt/4-amp power supply provides power for the reference PC board side of the optoisolation board. **Figure 1-5** depicts a completed system setup.

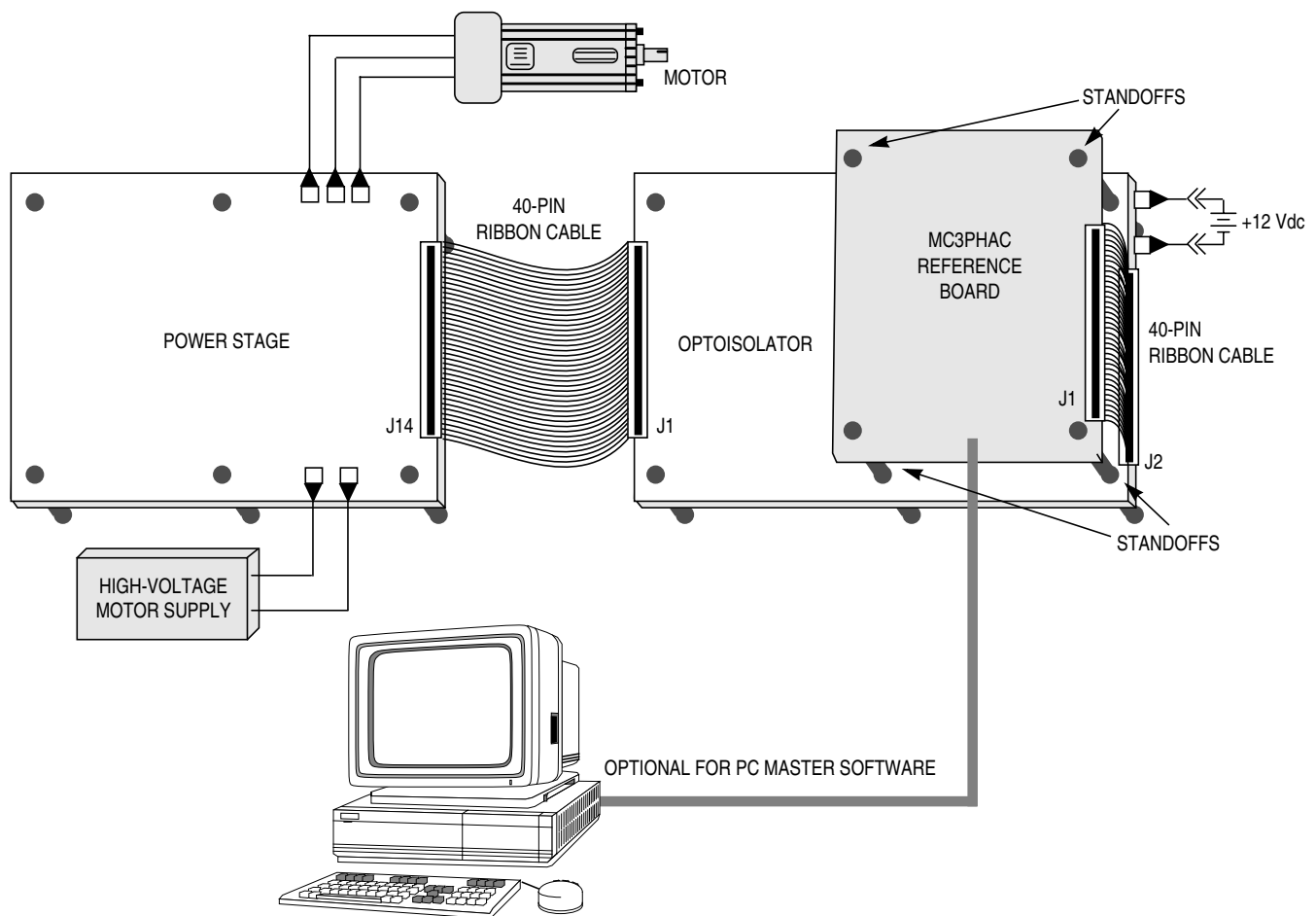


Figure 1-5. System Setup

A step-by-step procedure for setup of the reference PC board with an optoisolator board and high-voltage power stage is described here:

1. Mount four standoffs to the optoisolation board at the locations indicated in **Figure 1-5**. Standoffs, screws, and washers are included with the optoisolation board.
2. Plug one end of the 40-pin ribbon cable into the optoisolation board's input connector J2, labeled "Control Board."
3. Mount the reference PC board on top of the standoffs.
4. In this configuration, the reference PC board is powered from the optoisolation PC board. Jumper JP10, located to the right and slightly below the RESET push button, must be removed.
5. Plug the free end of the 40-pin ribbon cable into the reference PC board's output connector J1, located on the right hand side of the reference PC board.
6. Connect a 40-pin ribbon cable between the optoisolation board's connector J1 and the power stage's connector J14, as indicated in **Figure 1-5**.
7. Connect the three motor leads to the power stage as indicated in **Figure 1-5**.
8. Locate the START/STOP switch on the reference PC board and set it to STOP.
9. Locate the SPEED potentiometer on the reference PC board, R17, and set it to the slowest speed by rotating R17 to its most counter clockwise position.
10. Locate the forward/reverse (FWD/REV) switch on the reference PC board and set it to the desired direction of motor rotation.

NOTE: *When performing setup of the reference PC board, JP2 pins 1 to 2 must remain shorted throughout the process, as long as power is applied, unless otherwise stated.*

The following setup will be performed with both the 12-volt power supply connected to the optoisolation PC board and high-voltage power supply connected to the power module, with both power supplies turned on. The high-voltage power supply's output should be set between 140 and

230 Vdc, based on the motor requirements. Prior to connecting the high-voltage power supply to the power module, adjust its output voltage to that required by your specific motor.

11. The temperature limit, trim potentiometer (pot) (TEMP LIMIT, R3), sets the point at which an overtemperature fault will be input to the MC3PHAC, located on the reference PC board. The temperature signal is derived on the power stage from four diodes connected in series (located near the IGBT power transistors) and is pulled up with a resistor connected to 3.3 V, generated on the power stage. The temperature coefficient of the four series diodes is approximately $-8.8 \text{ mV}/^{\circ}\text{C}$. The diodes are not a calibrated temperature sensor, but provide an approximation of the temperature of the power transistors on the power module. The voltage output from the diodes at room temperature will range from 2.3 V to 2.4 V. Now set the overtemperature fault point:
 - a. Connect the high-voltage power supply to the line input terminal (J111) of the power stage.
 - b. Turn on the 12-volt supply connected to the optoisolation PC board.
 - c. Turn on the high-voltage power supply, leaving it set for the voltage of your specific motor.
 - d. Connect the ground lead of a digital volt-ohm meter (DVM) to the AGND (TP6) test point, located to the right center top of the reference PC board.
 - e. Connect the positive lead of the DVM to the test point marked TEMP (TP4), located at the center top of the reference PC board. The voltage at the test point (TP4) will be that of the temperature diode string residing on the power module at room temperature (V_{Room}). We will call the temperature of the room T_{Room} , which could be approximately 22°C .
 - f. Compute the voltage of the power module's heat sink temperature diodes at which a temperature fault should occur. An example would be to set the overtemperature fault (T_{Fault}) at 75°C (recommended). For this example, assume the T_{Room} (TP4) to be 2.35 volts. To compute the voltage

from the diode string at 75°C (T_{Fault}), the following equation applies: $V_{\text{TP4}} = V_{\text{Room}} + ((T_{\text{Fault}} - T_{\text{Room}}) * -0.0088)$.

That is, the voltage at TP5 will be:

$$1.88 \text{ V} = 2.35 + ((75-22) * -0.0088).$$

- g. Connect the DVM to the TEMP LMT (temperature limit) test point TP5. Adjust the TEMP LIMIT (R3) trim pot such that the voltage reads 1.88 volts on the DVM. The overtemperature fault is now set for ~75°C, based on the values calculated from the previous step.

12. The MC3PHAC requires the value of the high-voltage bus when operating. The bus voltage signal is derived on the power stage from a voltage divider connected to the high-voltage bus.

The voltage bus signal serves two purposes on the reference PC board. The divided, high-voltage bus is amplified and used for system control and also serves as an input to the overvoltage fault-generating circuitry. Now set the bus voltage amplifier, followed by the overvoltage fault point, by:

- a. Connect the ground lead of a DVM to the AGND (TP6) test point, located to the right center top of the reference PC board.
 - b. Connect the positive lead of the DVM to the test point marked V_{Bus} (TP2), located at the left top of the reference PC board.
 - c. Adjust the V_{Bus} GAIN (R2) trim pot such that the voltage reads 3.5 volts on the DVM.
 - d. To adjust the point at which the MC3PHAC will receive an overvoltage fault, connect the positive lead of the DVM to the test point marked V_{Bus} LIMIT (R1).
 - e. Adjust the V_{Bus} LIMIT (R1) trim pot such that the voltage reads 4.5 volts on the DVM.
13. If you are NOT using PC master software, skip to step 15.
 14. If PC master software is used for real-time control of motor operation, it is necessary to set up RS232 serial communication with a PC. To do this, connect a 9-conductor straight through cable from the reference board's DB-9 connector, J2, to the serial

port of the PC. If PC master software is used for real-time control of motor operation, it is necessary to set up the RS232 serial port of the PC. PC serial ports are wired as DTE (data terminal equipment) and the reference board's serial port is wired as DCE (data communications equipment). Therefore, a 9-conductor cable wired straight through cable must be used. Do NOT use a null modem cable.

Adjust the SPEED potentiometer to its most clockwise position. Install a shorting jumper on JP1. Install shorting jumpers on JP2–JP5, pins 1 to 2. Remove any additional jumpers from JP2–JP5. The reference board system setup when using PC master software is complete. Skip to step 26.

The following setup instructions pertain to use of the reference PC board and MC3PHAC in standalone mode:

15. The acceleration trim pot R8 sets the motor's acceleration and deceleration time. (Deceleration time is further controlled by other factors, such as the bus voltage. See the MC3PHAC data sheet, [Appendix A. MC3PHAC Data Sheet](#), for more detail.) The motor's acceleration can be specified in real time to range from 0.5 Hz/sec to 128 Hz/sec. Unlike trim pots R4–R6, the acceleration trim pot is constantly monitored by the MC3PHAC and may be changed while the motor is running. Acceleration time is specified to the MC3PHAC by supplying a voltage to pin 27. The value of the voltage at the wiper of trim pot R8 determines acceleration time. Acceleration time can be specified, with a scaling factor of 25.6 Hz/volt. To set the acceleration time:
 - a. Connect the ground lead of a DVM to the AGND (TP6) test point, located to the right center top of the reference PC board.
 - b. Connect the positive lead of the DVM to the test point marked ACCEL (TP8), located at the upper right top of the reference PC board. The voltage will be in the range from 0 to ~5 volts.
 - c. Adjust the ACCEL (R6) trim pot between 0 and ~5 volts to correspond to an acceleration range from 0.5 Hz/sec to 128 Hz/sec.

The remainder of the setup procedure for standalone mode will be completed with power removed from both the optoisolation board and the power stage.

16. Turn off the high voltage and the 12-volt power supplies.
17. Jumper header block JP1 is used to set the maximum frequency applied to the motor. The synchronous motor frequency can be specified in real time to be between 1 Hz to 128 Hz by the voltage output from the SPEED potentiometers. The scaling factor is 25.6 Hz/volt. Jumper JP1, located just above the SPEED potentiometers, sets the maximum frequency. To set the frequency limit:
 - a. Place a jumper on JP1 to obtain 0-Hz to 128-Hz motor frequency.
 - b. Remove the jumper from JP1 to obtain 0- to ~66-Hz motor frequency.
18. The MC3PHAC produces 50-Hz or 60-Hz base frequency and outputs positive or negative PWM (pulse-width modulated) polarities. Two jumper header blocks are resident on the reference PC board. These two jumper blocks, JP7 and JP9 (located to the lower left center of the reference PC board), provide the choice of positive PWM polarity at 50-Hz or 60-Hz base frequencies, respectively. Two unpopulated jumper block positions (JP6 and JP8) are located on the reference's PC board to accommodate two additional header blocks. These two unpopulated jumper blocks provide the choice of negative PWM polarity at 50-Hz or 60-Hz base frequencies, respectively. Because the reference PC board is intended to operate with the embedded motion control series of development tools, only the positive PWM polarity jumper headers are installed.

CAUTION: *Applying the improper polarity to a power stage could destroy it. Regardless of the system configuration, only one jumper can be applied to headers JP6–JP9.*

To set the PWM polarity and base frequencies:

- a. Place a jumper on JP7 for 50-Hz positive polarity PWM operation.
- b. Place a jumper on JP9 for 60-Hz positive polarity PWM operation.

Eight square trim pots are located at the top of the reference PC board. These must be set prior to using the system in standalone mode. Trim pots R1–R3 and R6 have been adjusted already. The trim pots control V_{BUS} limit (R1), V_{BUS} gain (R2), temp limit (R3), and retry time (R6).

19. Set the DVM to its resistance setting. The resistance values in the following procedures will be in the range of 0 to 50 k Ω . Connect one lead of the DVM to the test point labeled SETUP (TP7). That lead will remain in place on TP7 for the remainder of the setup procedure.
20. Remove all jumpers from JP2–JP5.
21. DEAD TIME trim pot R5 sets the dead time between the “on” states of the complementary PWM pairs to be specified. The range in standalone mode is 0.5 μ s to 6.0 μ s. In standalone mode, dead time is specified during the initialization phase of the MC3PHAC by supplying a voltage to pin 25 of the MC3PHAC pin while pin 19 of the MC3PHAC is driven low. In this way, dead time can be specified from 0.5 μ s to 6.0 μ s, with a scaling factor of 2.075 μ s/volt. The value of the voltage at the wiper of trim pot R5 determines dead time.

To set the dead time:

- a. Connect the loose lead of the DVM to JP3 pin 3.
- b. Adjust the DEAD TIME trim pot, R5, to the required resistance for the desired dead time (see [Figure 1-6](#)). When using the power stage described in this manual, set the dead time for 2.5 μ s, which will be approximately 2200 Ω .
- c. Remove the lead of the DVM from JP3 pin 3.



Figure 1-6. Dead Time vs. Resistance

22. RETRY TIME trim pot R6 sets the time between a system fault being cleared and the time when the system will re-enable the PWM outputs. The retry time range in standalone mode is 1 second to ~53 seconds. In standalone mode, retry time is specified during the initialization phase of the MC3PHAC by supplying a voltage to pin 25 of the MC3PHAC pin while pin 17 of the MC3PHAC is driven low. In this way, retry time can be specified with a scaling factor of 12 sec/volt. The value of the voltage at the wiper of trim pot R6 determines the retry time.

To set the retry time:

- Connect the loose lead of the DVM to JP4 pin 3.
- Adjust the RETRY TIME trim pot, R6, to the required resistance for the desired retry time (see [Figure 1-7](#)). For example, set the retry time to 15 seconds, which will be approximately 2200 Ω.
- Remove the lead of the DVM from JP4 pin 3.

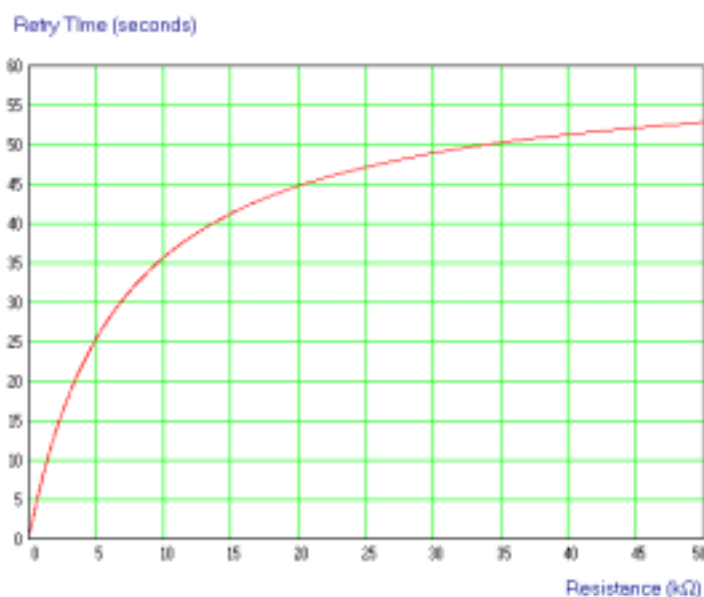


Figure 1-7. Retry Time vs. Resistance

23. PWM FREQ trim pot R7 sets the system's PWM base frequency. The system accommodates four discrete PWM base frequencies. Unlike trim pots R4–R6, the PWM frequency trim pot is constantly monitored by the MC3PHAC and may be changed while the motor is running. In standalone mode, PWM frequency is input to the MC3PHAC by supplying a voltage to pin 25 of the MC3PHAC while pin 16 of the MC3PHAC is driven low. The value of the voltage at the wiper of trim pot R7 determines PWM frequency. **Table 1-1** shows the required resistance levels on the PWM FREQ trim pot for the system to produce the various PWM base frequencies. The PWM frequencies are based on a 4.00-MHz frequency provided to the oscillator input pin of the MC3PHAC.

To set the PWM base frequency:

- a. Connect the loose lead of the DVM to JP5 pin 3.
- b. Adjust the PWM FREQ trim pot R7 to the required resistance for PWM frequency (see **Table 1-1**). For example, set the PWM frequency to 15.873 kHz which will be 12,000 Ω. The resistance tolerance of this setting can be ± 15 percent and still be within range.
- c. Remove the lead of the DVM from JP5 pin 3.

Table 1-1. Resistance and Corresponding PWM Frequencies

| PWM Frequency Resistance | PWM Frequency |
|-----------------------------|---------------|
| 1000 Ω | 5.291 kHz |
| 3900 Ω | 10.582 kHz |
| 12,000 Ω | 15.873 kHz |
| 43,000 Ω | 21.164 kHz |

24. VOLTAGE BOOST trim pot R4 sets the voltage boost to be specified as a percentage of full voltage at 0 Hz. In standalone mode, voltage boost is specified during the initialization phase of the MC3PHAC by supplying a voltage to pin 25 of the MC3PHAC pin while pin 20 of the MC3PHAC is driven low. In this way, voltage boost can be specified from 0 percent to 35 percent, with a scaling factor of 8 percent per volt. The value of the voltage at the wiper of trim pot R4 determines voltage boost.

To set the voltage boost:

- Connect the loose lead of the DVM to JP2 pin 3.
- Adjust the VOLTAGE BOOST trim pot, R4, to the required resistance for the desired percent voltage boost (see [Figure 1-8](#)). For example, set the voltage boost to 20 percent, which will be approximately 6800 Ω .
- Remove the lead of the DVM from JP2 pin 3.

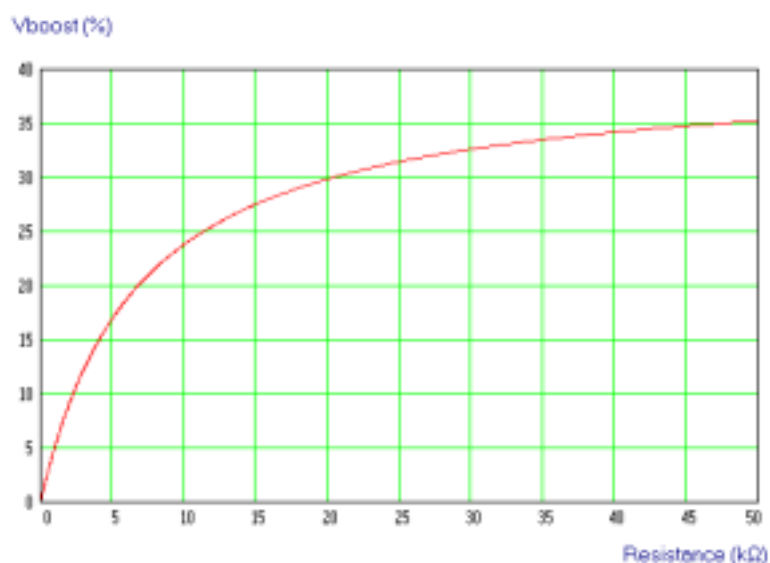


Figure 1-8. Voltage Boost vs. Resistance

25. Place jumpers on pins 2 to 3 of JP2–JP5. No other pins on JP2–JP5 can be shorted in standalone mode.
26. This completes control board setup.

CAUTION: *Hazardous voltages are present. **Re-read all of 1.6 Warnings carefully.***

Section 2. Operational Description

2.1 Contents

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2.2 Introduction

The reference PC board, utilizing the MC3PHAC integrated circuit, is designed to provide control signals for 3-phase ac induction motors. In combination with the embedded motion control series power stages and an optoisolation board, it provides a platform for evaluating the MC3PHAC.

User control inputs are accepted from START/STOP switches, FWD/REV switches, and a SPEED potentiometer located on the reference design PC board. Alternatively, motor commands can be entered via a PC and transmitted over a serial cable to DB-9 connector J2. Output connections and power stage feedback signals are grouped together on 40-pin ribbon cable connector J1. Power for operation of the reference PC board is supplied through the 40-pin ribbon cable from the optoisolation board.

Figure 2-1 shows a block diagram of the reference board's circuitry.

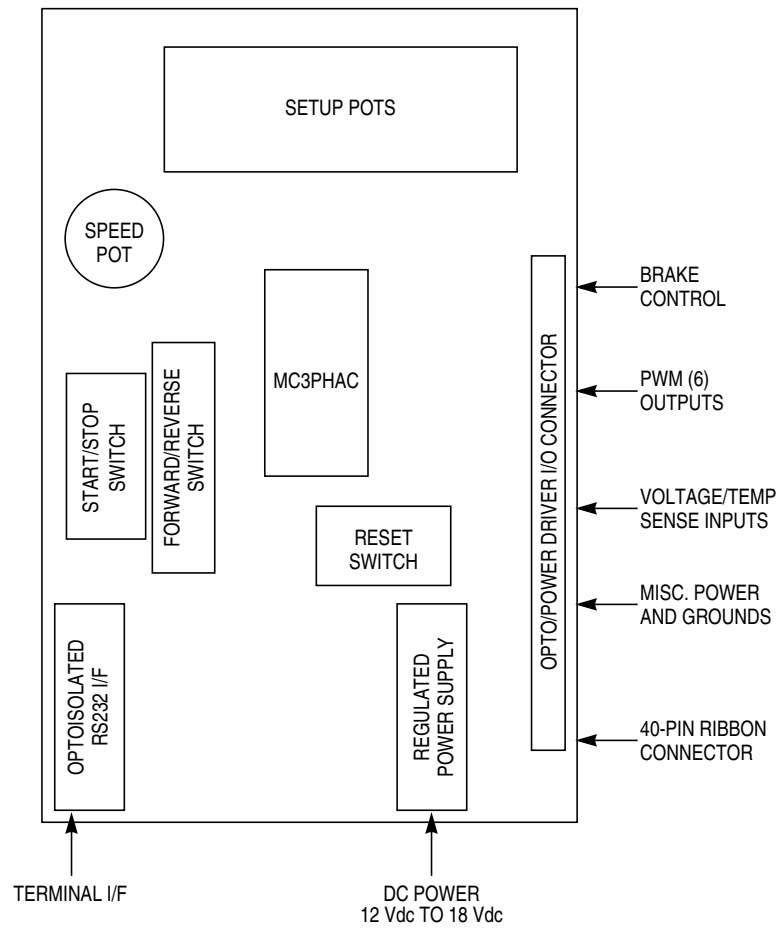


Figure 2-1. Reference PC Board Block Diagram

A summary of the information needed to use the reference PC board is presented in these sections. A discussion of the design appears in [Section 5. Design Considerations](#).

2.3 Electrical Characteristics

The electrical characteristics in [Table 2-1](#) apply to operation of the MC3PHAC reference PC board at 25°C.

Table 2-1. Electrical Characteristics

| Characteristic | Symbol | Min | Typ | Max | Units |
|---------------------------|-----------------|---------------------|-------------------|---------------------|-------|
| dc power supply voltage | V _{dc} | 10.8 ⁽¹⁾ | 12 ⁽¹⁾ | 16.5 ⁽¹⁾ | V |
| Quiescent current | I _{CC} | — | 80 | — | mA |
| Min logic 1 input voltage | V _{IH} | 2.0 | — | — | V |
| Max logic 0 input voltage | V _{IL} | — | — | 0.8 | V |
| Analog input range | V _{IN} | 0 | — | 5.0 | V |
| RS232 connection speed | — | 9504 | 9600 | 9696 | Baud |

1. When operated and powered separately from other embedded motion control toolset products

2.4 User Interfaces

The MC3PHAC reference PC board has several user interfaces. They include an optoisolated RS232 serial interface, potentiometers, switches, jumpers, indicator LEDs, and test points. Descriptions for each of these interfaces follow.

2.4.1 Potentiometers

Nine potentiometers are provided on the reference PC board for system operation and setup. When the PC board is used in PC master software mode, three of the potentiometers are used by the reference PC board's hardware. These are the V_{BUS} LIMIT, V_{BUS} GAIN, and TEMP LIMIT potentiometers. The potentiometers are listed here.

- **R17: SPEED** — R17, labeled SPEED, is the speed control potentiometer. When the system is operated in standalone mode, speed control defaults to R17. Clockwise rotation increases motor speed. Jumper JP1 is used in concert with the SPEED potentiometers. When JP1 is shorted, the speed range is 0 to

128 Hz. When JP1 is removed, the speed range is 0 to ~66 Hz. When operating in PC master software mode, speed control commands are sent over the RS232 interface. In PC master software mode, R17 may be monitored but its position has no control over the motor. In future implementations of PC master software, R17 could be used to control the motor's speed.

- **R8: ACCEL** — Acceleration control is set by trim potentiometer R8 (ACCEL). Clockwise rotation increases the motor's acceleration rate.
- **R1: V_{Bus} LIMIT** — The overvoltage fault threshold is set by trim potentiometer R1 (V_{Bus} LIMIT). Clockwise rotation increases the threshold. R1 is used in concert with trim potentiometer R2, V_{Bus} GAIN.
- **R2: V_{Bus} GAIN** — The voltage bus gain trim potentiometer, R2 (V_{Bus} GAIN), divides the high-voltage bus feedback that is input from the optoisolator board or power board. Its output then drives a gain-of-three amplifier which provides a bus voltage representation to the MC3PHAC and also drives the overvoltage fault input. Clockwise rotation increases gain.
- **R3: TEMP LIMIT** — The high-temperature fault threshold is set by trim potentiometer R3 (TEMP LIMIT). Clockwise rotation increases the high-temperature threshold fault point.
- **R4: VOLTAGE BOOST** — The voltage boost trim potentiometer, R4 (VOLTAGE BOOST), is used as an input to the MC3PHAC. It sets the low-frequency voltage boost characteristic. Clockwise rotation increases voltage boost.
- **R5: DEAD TIME** — The dead time trim potentiometer, R5 (DEAD TIME), is used to set the complementary top-to-bottom transition delay time. The range of dead time in standalone operation is 0.5 μs to 6.0 μs . Clockwise rotation increases dead time.
- **R6: RETRY TIME** — The retry time trim potentiometer, R6 (RETRY TIME), sets the time between a system fault being cleared and the time when the system will re-enable the PWM outputs. Retry range in standalone mode is 1 second to ~53 seconds. Clockwise rotation increases fault retry time.

- **R7: PWM FREQ** — The PWM frequency trim potentiometer sets the PWM frequency. Depending on the position of the trim potentiometer, the PWM frequency choices are 5.291 kHz, 10.582 kHz, 15.873 kHz, and 21.164 kHz. Clockwise rotation increases PWM frequency.

2.4.2 Switches

Three switches provide for user inputs. They are listed here.

- **SW1: START/STOP** — SW1, START/STOP, is a toggle switch located on the left-hand side of the board. It starts and stops the motor when the system is operated in standalone mode. Switching it up (toward the top of the board) turns the motor on, and switching it down stops it. In PC master software mode, the START/STOP switch may be monitored, but its position has no control over the motor. In future implementations of PC master software, SW1 could be used to start or stop the motor.
- **SW2: FWD/REV** — SW2, FWD/REV, is a toggle switch located to the right of the START/STOP. It controls direction of the motor when the system is operated in standalone mode. Positioning it up (toward the top of the board) runs the motor forward; switching it down runs it in reverse. In PC master software mode, the FWD/REV switch may be monitored, but its position has no control over the motor. In future implementations of PC master software, SW2 could be used to change direction of the motor.
- **SW3: RESET** — SW3, the RESET switch, is a push button located near the lower center of the board. It resets the MC3PHAC in standalone and PC master software modes.

2.4.3 Jumpers

There are 10 jumpers: JP1–JP10. Jumper JP1 is located on the upper-left corner of the PC board, just above the SPEED potentiometers. JP2 through JP5 are grouped near the upper center of the PC board. JP6 through JP9 are located above and to the right of the FWD/REV switch. JP10 is located near the bottom right-hand side of the PC board and to the left of the 40-pin ribbon cable connector. They are described here.

- **JP1** — Jumper JP1 is used to set the frequency range of the six PWM outputs. When JP1 is shorted, the speed range is 0 to 128 Hz. When JP1 is removed, the speed range is 0 to ~66 Hz.
- **JP2** — Jumper JP2 is a 4-position jumper header. When shorted between positions 1 and 2, the MC3PHAC is set to run in PC master software mode. When shorted between positions 2 and 3, the MC3PHAC is set to run in standalone mode. In standalone mode, the voltage boost trim potentiometer is connected to the MC3PHAC's pin 20. Positions 3 and 4 are unused.
- **JP3** — Jumper JP3 is a 4-position jumper header. When shorted between positions 1 and 2, the MC3PHAC is set to run in PC master software mode and the fault LED is connected to the MC3PHAC's fault output. When shorted between positions 2 and 3, the MC3PHAC is set to run in standalone mode. In standalone mode, the dead time trim potentiometer is connected to the MC3PHAC's pin 19. Positions 3 and 4 are unused.
- **JP4** — Jumper JP4 is a 4-position jumper header. When shorted between positions 1 and 2, the MC3PHAC is set to run in PC master software mode and the serial output of the MC3PHAC is connected to the optoisolated RS232 transmit optoisolator. When shorted between positions 2 and 3, the MC3PHAC is set to run in standalone mode. In standalone mode, the retry time trim potentiometer is connected to the MC3PHAC's pin 17. Positions 3 and 4 are unused.
- **JP5** — Jumper JP5 is a 4-position jumper header. When shorted between positions 1 and 2, the MC3PHAC is set to run in PC master software mode and the serial input of the MC3PHAC is connected to the optoisolated RS232 receive optoisolator. When

JP5 is shorted between positions 2 and 3, the MC3PHAC is set to run in standalone mode. In standalone mode, the PWM frequency trim potentiometer is connected to the MC3PHAC's pin 18. Positions 3 and 4 are unused.

- **JP6 through JP9** — Jumpers JP6 through JP9 are 2-position jumper headers. Only one of these jumpers may be installed at any given time. The jumpers set the PWM frequency at 50 Hz or 60 Hz, positive or negative PWM polarity. Only jumper blocks JP7 and JP9 are populated on the PC board.
- **JP10** — Jumper JP10 is used to prevent ground loops when the analog ground reference originates on an external PC board, as in the case with the optoisolation PC board. In normal operation, this jumper is removed. JP10 is installed if the reference PC board is self-powered and running without a power module or optoisolation board connected to J1.

2.4.4 Indicator Lights

Three LEDs located on the control board provide status information to the user. The power-on LED, D6, is located to the right of the FWD/REV switch. The fault LED, D1, is located just above and to the right of the SPEED potentiometers. The brake LED, D2, is located to the right of the fault LED. Descriptions are listed here.

- **D1: Fault (Red)** — D1 illuminates when a fault has occurred.
- **D2: Brake (Yellow)** — D2 illuminates when the MC3PHAC energizes the resistive brake.
- **D6: Power On** — D6, labeled POWER, illuminates when power is applied to the board.

2.4.5 Test Points

A variety of test points are provided to facilitate measurements with a DVM or an oscilloscope. They are listed in [Table 2-2](#).

Table 2-2. Test Points

| Label | Location | Signal Name | Connected To |
|------------------------|--------------------------|----------------------|----------------|
| SPEED | Upper-left edge (TP1) | SPEED | MC3PHAC PIN 26 |
| V _{Bus} | Upper-left edge (TP2) | V _{Bus} | MC3PHAC PIN 28 |
| V _{Bus} LIMIT | Upper-left edge (TP3) | V _{Bus} LMT | U1B Pin 6 |
| TEMP | Upper-edge center (TP4) | TEMP | U1A Pin 2 |
| TEMP LIMIT | Upper-edge center (TP5) | TEMP LMT | U1A Pin 3 |
| AGND | Upper-edge center (TP6) | AGND | AGND |
| SETUP | Upper-right edge (TP7) | Setup | MC3PHAC Pin 25 |
| ACCEL | Upper-right edge (TP8) | Accel. input | MC3PHAC Pin 27 |
| DGND | Upper-right edge (TP9) | DGND | DGND |
| PWM6 | Right-center edge (TP10) | PWM6 | MC3PHAC Pin 14 |
| PWM5 | Right-center edge (TP11) | PWM5 | MC3PHAC Pin 13 |
| PWM4 | Right-center edge (TP12) | PWM4 | MC3PHAC Pin 12 |
| PWM3 | Right-center edge (TP13) | PWM3 | MC3PHAC Pin 11 |
| TP14 | Center (TP14) | Fault | MC3PHAC Pin 15 |
| PWM2 | Right-center edge (TP15) | PWM2 | MC3PHAC Pin 10 |
| PWM1 | Right-center edge (TP16) | PWM1 | MC3PHAC Pin 9 |

2.4.6 Optoisolated RS232 Interface

An optoisolated RS232 interface is available via DB-9 connector J2. It connects to the serial port of a Windows[®]-based PC, or any microcontroller emulating the PC master software interface, and enables motor commands to be entered via PC master software. Control is transferred to the serial interface on reset with JP2 pins 1 and 2 shorted.

[®] Windows is a registered trademark of Microsoft Corporation in the United States and/or other countries.

Section 3. Pin Descriptions

3.1 Contents

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| 3.3.3 | Power Connector J3 | 45 |

3.2 Introduction

Three connectors are resident on the control board, labeled J1 through J3. They are:

- J1 — 40-pin ribbon cable connector
- J2 — RS232 DB-9 connector
- J3 — Power jack

3.3 Control Board Signal Descriptions

The following subsections describe signals on control board connectors J1 through J3.

3.3.1 40-Pin Connector J1

Signals to and from an optoisolation board or power stage are grouped together on 40-pin ribbon cable connector J1. Pin assignments are shown in **Figure 3-1**. In this figure, a schematic representation appears on the left, and a physical layout of the connector appears on the right. Pin descriptions are listed in **Table 3-1**.

Pin Descriptions

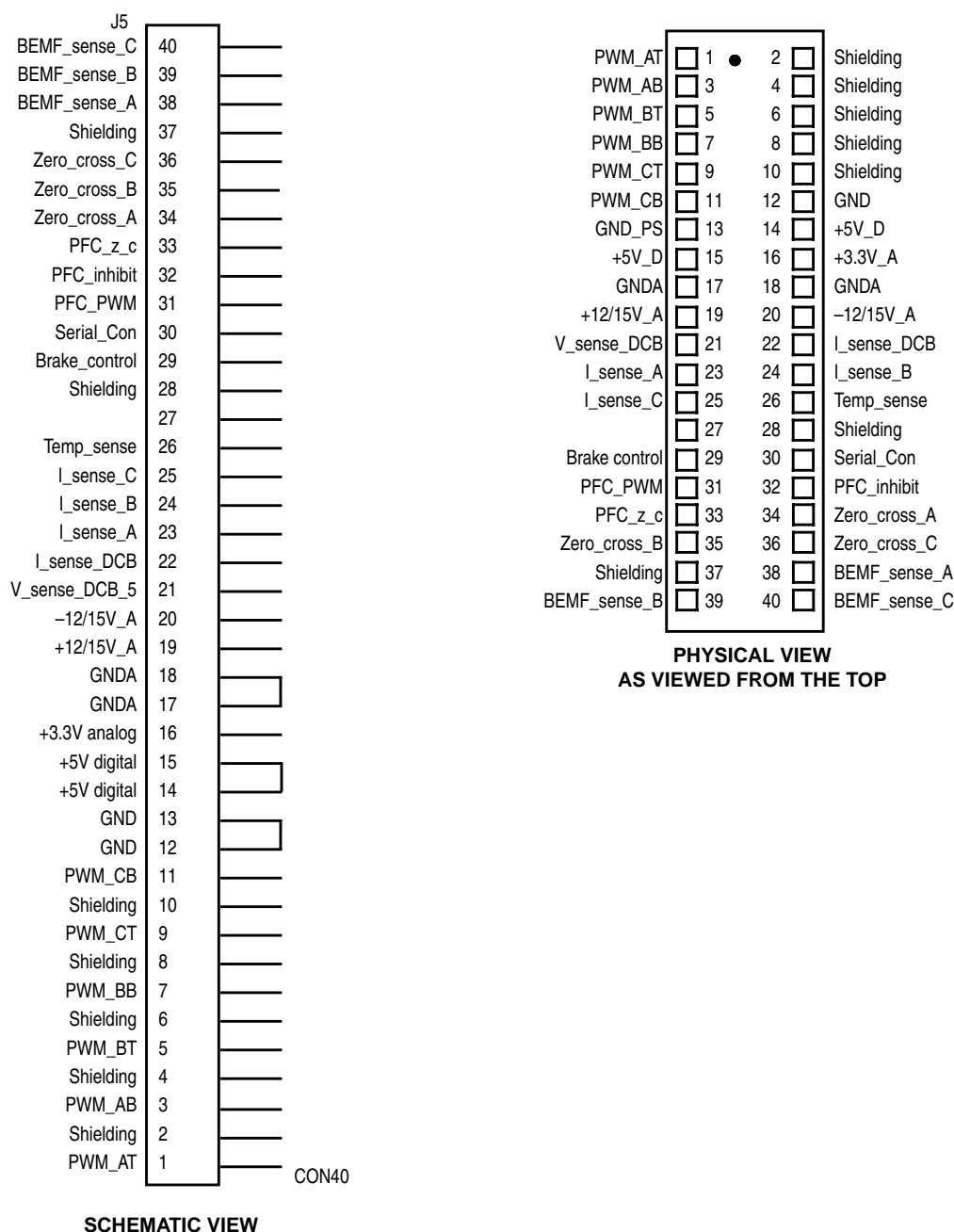


Figure 3-1. 40-Pin Ribbon Connector J1

Table 3-1. 40-Pin Ribbon Connector J1

| Pin No. | Signal Name | Description |
|---------|--------------|--|
| 1 | PWM_AT | PWM_AT is the gate drive signal for the top half-bridge of phase A. A logic high turns phase A's top switch on. PWM_AT is connected to PWM_U_TOP on the MC3PHAC. |
| 2 | Shielding | Pin 2 is not connected. The ribbon cable pin 2 is grounded on the optoisolation PC board. That ground helps prevent cross talk between adjacent signals. |
| 3 | PWM_AB | PWM_AB is the gate drive signal for the bottom half-bridge of phase A. A logic high turns phase A's bottom switch on. PWM_AB is connected to PWM_U_BOP on the MC3PHAC. |
| 4 | Shielding | Pin 4 is not connected. The ribbon cable pin 4 is grounded on the optoisolation PC board. That ground helps prevent cross talk between adjacent signals. |
| 5 | PWM_BT | PWM_BT is the gate drive signal for the top half-bridge of phase B. A logic high turns phase B's top switch on. PWM_BT is connected to PWM_V_TOP on the MC3PHAC. |
| 6 | Shielding | Pin 6 is not connected. The ribbon cable pin 6 is grounded on the optoisolation PC board. That ground helps prevent cross talk between adjacent signals. |
| 7 | PWM_BB | PWM_BB is the gate drive signal for the bottom half-bridge of phase B. A logic high turns phase B's bottom switch on. PWM_BB is connected to PWM_V_BOT on the MC3PHAC. |
| 8 | Shielding | Pin 8 is not connected. The ribbon cable pin 8 is grounded on the optoisolation PC board. That ground helps prevent cross talk between adjacent signals. |
| 9 | PWM_CT | PWM_CT is the gate drive signal for the top half-bridge of phase C. A logic high turns phase C's top switch on. PWM_CT is connected to PWM_W_TOP on the MC3PHAC. |
| 10 | Shielding | Pin 10 is not connected. The ribbon cable pin 10 is grounded on the optoisolation PC board. That ground helps prevent cross talk between adjacent signals. |
| 11 | PWM_CB | PWM_CB is the gate drive signal for the bottom half-bridge of phase C. A logic high turns phase C's bottom switch on. PWM_CB is connected to PWM_W_BOT on the MC3PHAC. |
| 12 | GND | Digital power supply ground |
| 13 | GND | Digital power supply ground, redundant connection |
| 14 | +5V_D | Digital +5-volt power supply |
| 15 | +5V digital | Digital +5-volt power supply, redundant connection |
| 16 | +3.3V analog | Unused |
| 17 | GNDA | Analog power supply ground |

Table 3-1. 40-Pin Ribbon Connector J1

| Pin No. | Signal Name | Description |
|---------|---------------|--|
| 18 | GNDA | Analog power supply ground, redundant connection |
| 19 | +12/15V_A | Unused analog +12-volt to +15-volt power supply |
| 20 | +12/15V_A | Unused analog +12-volt to +15-volt power supply |
| 21 | V_sense_DCB_5 | V_sense_DCB is an analog sense signal that measures the power board's dc bus voltage. V_sense_DCB_5 is connected to the DC_BUS input pin on the MC3PHAC. |
| 22 | I_sense_DCB | Unused analog sense signal |
| 23 | I_sense_A | Unused analog sense signal |
| 24 | I_sense_B | Unused analog sense signal |
| 25 | I_sense_C | Unused analog sense signal |
| 26 | Temp_sense | Temp_sense is an analog sense signal that measures the power stage's substrate temperature. |
| 27 | Shielding | Pin 27 is not connected. The ribbon cable pin 27 is grounded on the optoisolation PC board. That ground helps prevent cross talk between adjacent signals. |
| 28 | Shielding | Pin 28 is not connected. The ribbon cable pin 28 is grounded on the optoisolation PC board. That ground helps prevent cross talk between adjacent signals. |
| 29 | Brake_control | Brake_control is the gate drive signal for the power board's brake transistor. Brake_control is connected to the RBRAKE output pin on the MC3PHAC. |
| 30 | Serial_Con | Pin 30: Unused Serial_Con, normally used to identify the type of board connected to the control board |
| 31 | PFC_PWM | Unused |
| 32 | PFC_inhibit | Unused |
| 33 | PFC_z_c | Unused |
| 34 | Zero_cross_A | Unused |
| 35 | Zero_cross_B | Unused |
| 36 | Zero_cross_C | Unused |
| 37 | Shielding | Pin 37 is not connected. The ribbon cable pin 37 is grounded on the optoisolation PC board. That ground helps prevent cross talk between adjacent signals. |
| 38 | BEMF_sense_A | Unused |
| 39 | BEMF_sense_B | Unused |
| 40 | BEMF_sense_C | Unused |

3.3.2 Optoisolated RS232 DB-9 Connector J2

The RS232 DB-9 connector, J2, is a 9-pin female connector for serial communications with a PC. It has standard RS232 pinouts. The schematic [Figure 4-3](#) shows J2 at the top-center of the page. Pinouts are listed in [Table 3-2](#).

Table 3-2. Optoisolated RS232 DB-9 Connector J2

| Pin No. | Signal Name | Description |
|---------|-------------|---|
| 1 | Unused | N/A |
| 2 | RXD | Data received by the PC from the control board |
| 3 | TXD | Data transmitted from the PC to the control board |
| 4 | DTR | PC indicates that it is ready to receive data. |
| 5 | GND | Common ground reference |
| 6 | Unused | N/A |
| 7 | RTS | PC requests to send data to the control board. |
| 8 | Unused | N/A |
| 9 | Unused | N/A |

3.3.3 Power Connector J3

A power connector, J3, is a 2.1-mm power jack that provides connection to a 12-volt dc power supply. This power input connector is used only when the control board is operating independently from other boards in the embedded motion control toolset.

Section 4. Schematics and Parts List

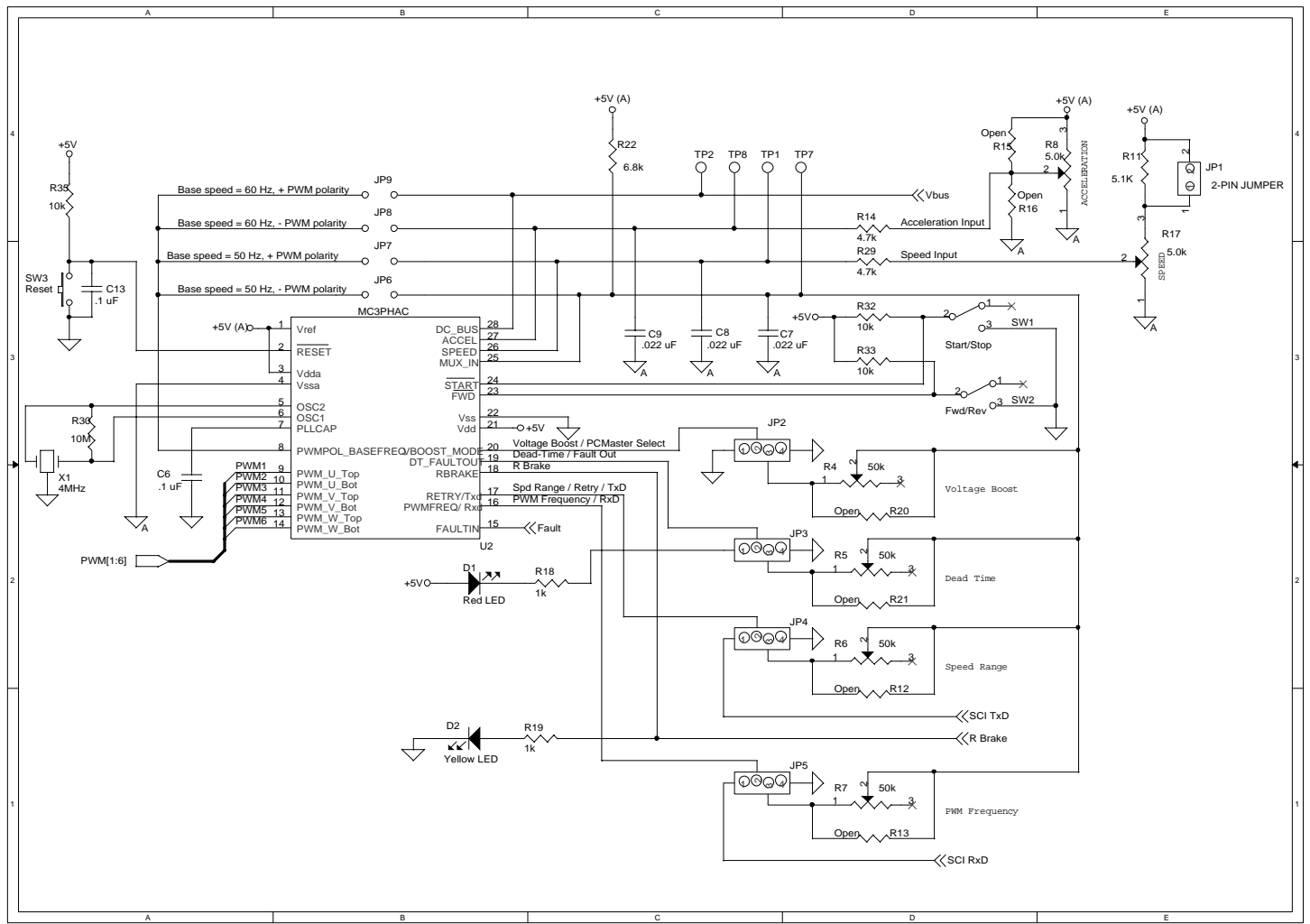
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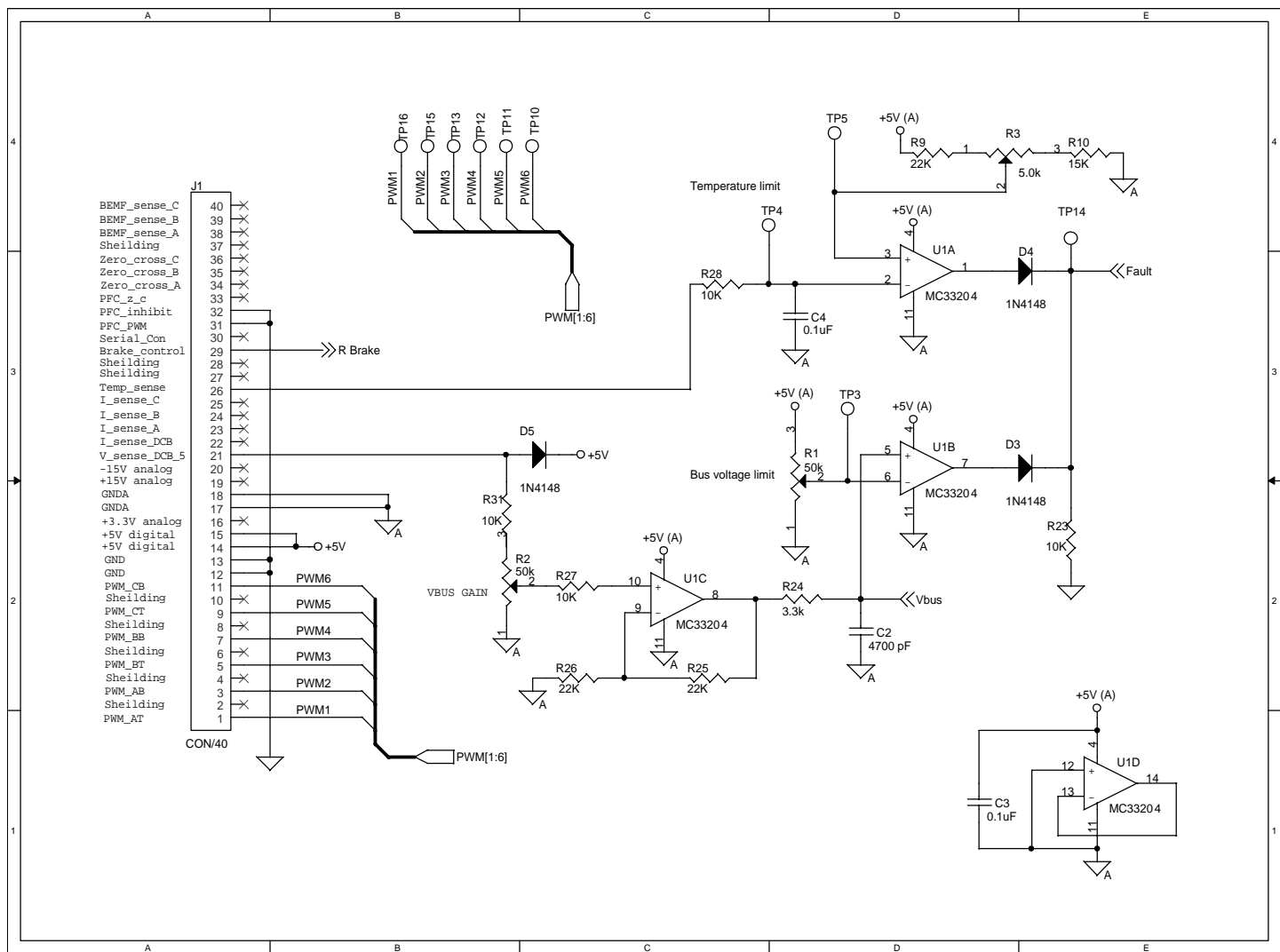
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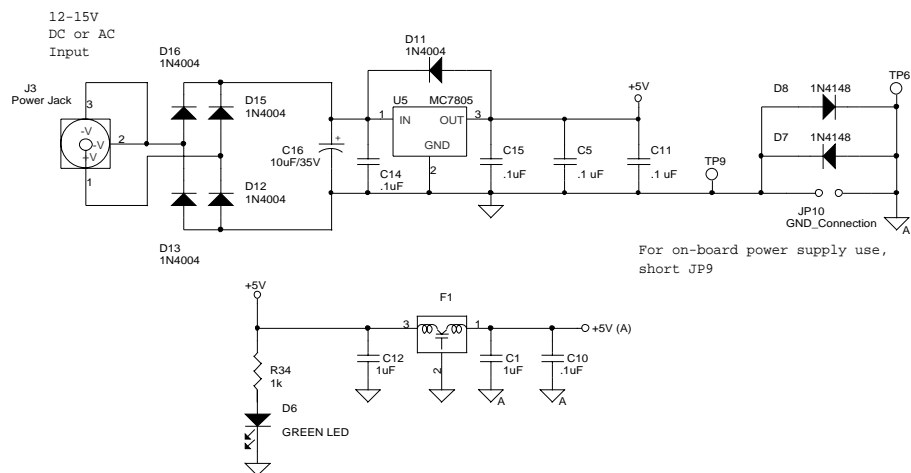
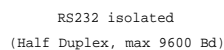
4.3 Parts Lists51

4.2 Schematics

A set of schematics for the reference PC board appears in **Figure 4-1** through **Figure 4-3**. Unless otherwise specified, resistors are 1/4 watt, have a ± 5 percent tolerance, and have values shown in ohms. Interrupted lines coded with the same letters are electrically connected.







4.3 Parts Lists

The MC3PHAC PC reference board parts content is described in [Table 4-1](#).

Table 4-1. Reference PC Board Parts List (Sheet 1 of 3)

| Designators | Qty | Description ⁽¹⁾ | Manufacturer | Part Number |
|--|-----|---------------------------------|--------------|---------------|
| C2 | 1 | 4700 pF | Digi-Key | P4902-ND |
| C1, C3, C4, C5, C6, C10, C11, C12, C13, C14, C15 | 11 | 0.1- μ F capacitor | Digi-Key | P4910-ND |
| C7, C8, C9 | 3 | 0.022 μ F | Digi-Key | P4906-ND |
| C16 | 1 | 10- μ F capacitor @ 50 Vdc | Digi-Key | P5567-ND |
| C17 | 1 | 2.2- μ F capacitor @ 50 Vdc | Digi-Key | P5564-ND |
| D1 | 1 | Red LED | Digi-Key | 160-1081-ND |
| D2 | 1 | Yellow LED | Digi-Key | 160-1082-ND |
| D6 | 1 | Green LED | Digi-Key | 160-1083-ND |
| D3, D4, D5, D7, D8, D9, D10, D14 | 8 | 1N4148 small signal diode | Digi-Key | 1N4148DICT-ND |
| D11, D12, D13, D15, D16 | 5 | Diode | Digi-Key | 1N4004MSCT-ND |
| F1 | 1 | 3-pin filter | Digi-Key | P9809CT-ND |
| J1 | 1 | 40-pin shrouded connector | Digi-Key | A26279-ND |
| J2 | 1 | DB-9 | Digi-Key | A23301-ND |
| J3 | 1 | Power connector | Digi-Key | SC1152-ND |
| JP2, JP3, JP4, JP5 | 4 | 1x4 pin header ⁽²⁾ | Digi-Key | S1011-36-ND |
| JP1, JP7, JP9, JP10 | 4 | 1x2 pin header ⁽²⁾ | Digi-Key | S1011-36-ND |
| JP6, JP8 | 0 | 1x2 pin header — not installed | N/A | N/A |

Table 4-1. Reference PC Board Parts List (Sheet 2 of 3)

| Designators | Qty | Description ⁽¹⁾ | Manufacturer | Part Number |
|---|-----|----------------------------------|--------------|--------------|
| R18, R19, R36, R37 | 4 | 1-k Ω resistor | Digi-Key | 1.0KQBK-ND |
| R11, R14, R29, R39 | 4 | 4.7-k Ω resistor | Digi-Key | 4.7KQBK-ND |
| R22, R26 | 2 | 6.8-k Ω resistor | Digi-Key | 6.8KQBK-ND |
| R34 | 1 | 470- Ω resistor | Digi-Key | 470QBK-ND |
| R12, R13, R15, R16, R20, R21 | 0 | Resistors — not installed | N/A | N/A |
| R1, R2, R4, R6, R7 | 5 | 50-k Ω trim potentiometer | Digi-Key | 3386F-503-ND |
| R5 | 1 | 10-k Ω trim potentiometer | Digi-Key | 3386F-103 |
| R3, R8 | 2 | 5-k Ω trim potentiometer | Digi-Key | 3386F-502-ND |
| R17 | 1 | 5-k Ω potentiometer | Digi-Key | 392JB-502-ND |
| R9, R25 | 2 | 22-k Ω resistor | Digi-Key | 22KQBK-ND |
| R38 | 1 | 330- Ω resistor | Digi-Key | 330QBK-ND |
| R23, R27, R28, R31, R32, R33, R35 | 8 | 10-k Ω resistor | Digi-Key | 10KQBK-ND |
| R30 | 1 | 10-M Ω resistor | Digi-Key | 10MQBK-ND |
| R10 | 1 | 15-k Ω resistor | Digi-Key | 15KQBK-ND |
| R24 | 1 | 3.3-k Ω resistor | Digi-Key | 3.3KQBK-ND |
| SW1, SW2 | 2 | SPDT toggle switch | NKK | M2012SS1G03 |
| SW3 | 1 | Momentary push button switch | Digi-Key | CKN9009-ND |
| TP6, TP9 | 2 | Test point black | Digi-Key | 5006K-ND |
| TP1, TP2, TP3, TP4, TP5, TP7, TP8 | 7 | Test point red | Digi-Key | 5005K-ND |
| TP10, TP11, TP12, TP13, TP14, TP15, TP16 | 7 | Test point white | Digi-Key | 5007K-ND |

Table 4-1. Reference PC Board Parts List (Sheet 3 of 3)

| Designators | Qty | Description⁽¹⁾ | Manufacturer | Part Number |
|--------------------|------------|----------------------------------|---------------------|--------------------|
| U2 | 1 | MC3PHAC | Motorola | MC3PHACVP |
| U3, U4 | 2 | 4N35 optocoupler | Digi-Key | 4N35QT-ND |
| U5 | 1 | Fixed 5-V regulator | Digi-Key | UA7805CKC |
| U1 | 1 | Quad operational amplifier | National | LMC6484N |
| X1 | 1 | 4.00-MHz resonator | Digi-Key | X902-ND |
| XU2 | 1 | 28-pin socket for U2 | Digi-Key | A409-ND |
| No designator | 1 | 0.25-inch 4-40 screw for U5 | Any | N/A |
| No designator | 1 | 4-40 nut for U5 | Any | N/A |
| No designator | 5 | Stick-on rubber feet | Digi-Key | SJ5003-0-ND |
| Bare PCB | 1 | ASB509 bare PCB | DS Electronics | N/A |
| No designator | 7 | Shunts for JP1–JP5, PJ9, JP10 | Digi-Key | S9000-ND |

1. All resistors are 1/4 W with a tolerance of 5% unless otherwise noted.

2. Shipped in strips of 36 x 1 cut to length

Section 5. Design Considerations

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| 5.8 | Optoisolated RS232 Interface | 60 |

5.2 Overview

Motor drive systems have a number of important design considerations related to noise management and protection of the power transistors. Some of the considerations are dead time, power-up/power-down, and grounding. These design considerations are discussed in [5.3 Dead Time](#) through [5.5 Grounding](#). A description of some of the reference board's circuits is included in [5.6 Fault Circuits](#) and [5.7 On-Board Power Supply](#).

5.3 Dead Time

In induction motor drives, providing dead time between turn-off of one output transistor and turn-on of the other output transistor in the same phase is an important design consideration. Dead time is also a feature that is built into the MC3PHAC's PWM module. It is programmable, to accommodate a variety of gate drives and output transistors. When using the power module referenced in this document, 2.5- μ s dead time should be selected.

5.4 Power-Up/Power-Down

When power is applied or removed, it is important that top and bottom output transistors in the same phase are not turned on simultaneously. Since logic states are not always defined during power-up, it is important to ensure that all power transistors remain off when the controller's supply voltage is below its normal operating level. The MC3PHAC module's outputs switch to a high-impedance configuration whenever the 5-volt supply is below its specified minimum.

The power module has pulldown resistors at all of the gate drive inputs. This feature, coupled with the MC3PHAC's PWM module's outputs, ensures that all power transistors remain off during power-up and power-down.

5.5 Grounding

PC board layout is an important design consideration. In particular, ground planes and how grounds are tied together influence noise immunity. To maximize noise immunity, it is important to get a good ground plane under the MC3PHAC integrated circuit. It is also important to separate analog and digital grounds. That is why there are two ground designations, digital GND and AGND. Digital GND is the digital ground plane and power supply return. AGND is the analog circuit ground. They are both the same reference voltage, but are routed separately, and tie together at only one point.

5.6 Fault Circuits

In the design of the reference PC board, two fault signals are combined to produce one fault input to the MC3PHAC's FAULTIN pin. The combined faults are overvoltage and overtemperature. These analog signals are fed into comparators having adjustable reference voltages, used for setting the individual fault levels.

The comparator outputs provide digital signals to the MC3PHAC's FAULTIN pin. These faults, should one or both occur, will force the PWM module into a known inactive state, protecting the power module.

Figure 5-1 is a schematic of the overvoltage fault generating circuit. The input for this circuit originates from the power module and is connected to a voltage divider that is connected to the power module's high-voltage bus. U1C is used to amplify the bus voltage signal before it is input to the overvoltage comparator, U1B. The threshold for the bus overvoltage fault is set by trim pot R1. As long as the voltage fed into the inverting input of comparator U1B is greater than the voltage from the bus voltage divider from the power module, the output from comparator U1B is held at a logic 0. If the voltage from the voltage divider on the power module exceeds the voltage set by trim pot R1, the output of the comparator will be driven to a logic 1, driving a fault into the MC3PHAC's fault input.

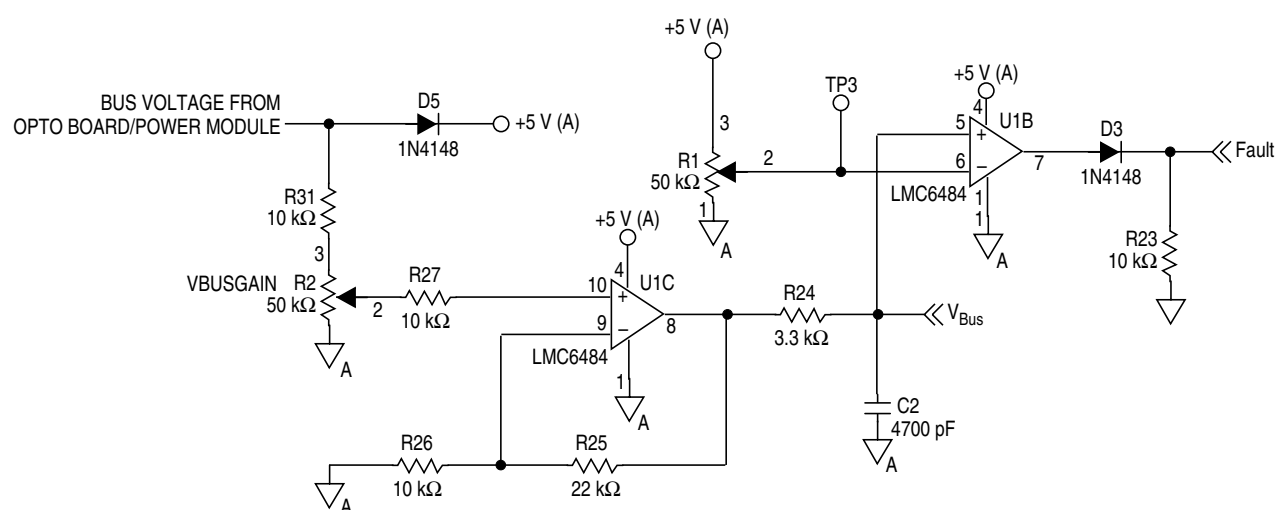


Figure 5-1. Overvoltage Fault Circuit

Figure 5-2 is a schematic of the overtemperature fault generating circuit. The input for this circuit originates on the power module from a string of four diodes connected in series, pulled up to 3.3 volts through a resistor. These four diodes have a temperature coefficient of approximately $-8.8 \text{ mV}/^{\circ}\text{C}$. The output from the diode string is connected to the inverting input of U1A. As long as the voltage applied to the inverting input of U1A, set by R9, R10, and trim pot R3 is greater than the voltage connected to the non-inverting input of U1A, the output of the comparator (U1A) will be at a logic 0. When the voltage output from the diode string falls below the input at the non-inverting input of the comparator, indicating a rise in temperature above the fault setpoint, the output of the comparator will switch to a logic 1, driving a fault into the MC3PHAC's fault input.

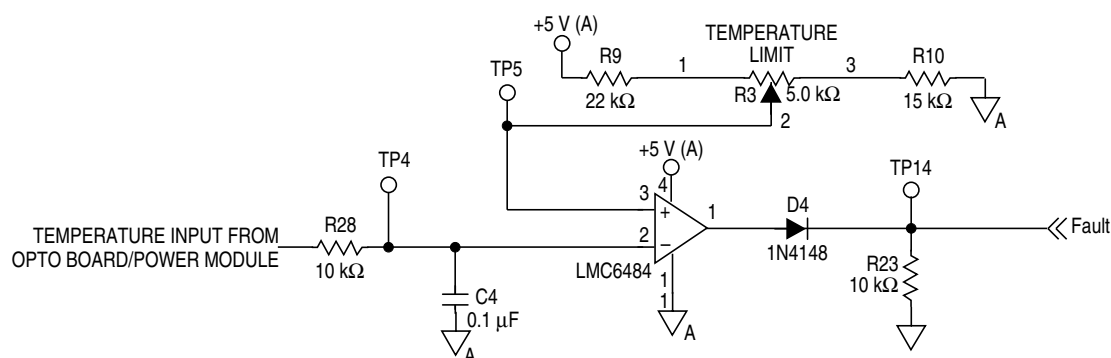


Figure 5-2. Overtemperature Fault Circuit

5.7 On-Board Power Supply

Figure 5-3 is the schematic of the on-board power supply. The power supply resident on the reference PC board is simply a 5-volt linear regulator. This power supply is only used if the PC board is run with no power module or optoisolation board connected to the 40-pin connector J1. This on-board power supply has a full wave bridge, allowing ac or dc to be applied to its power jack J3.

The 5 volts supplied to the analog-to-digital converter is filtered by filter F1 to provide a quiet source of power.

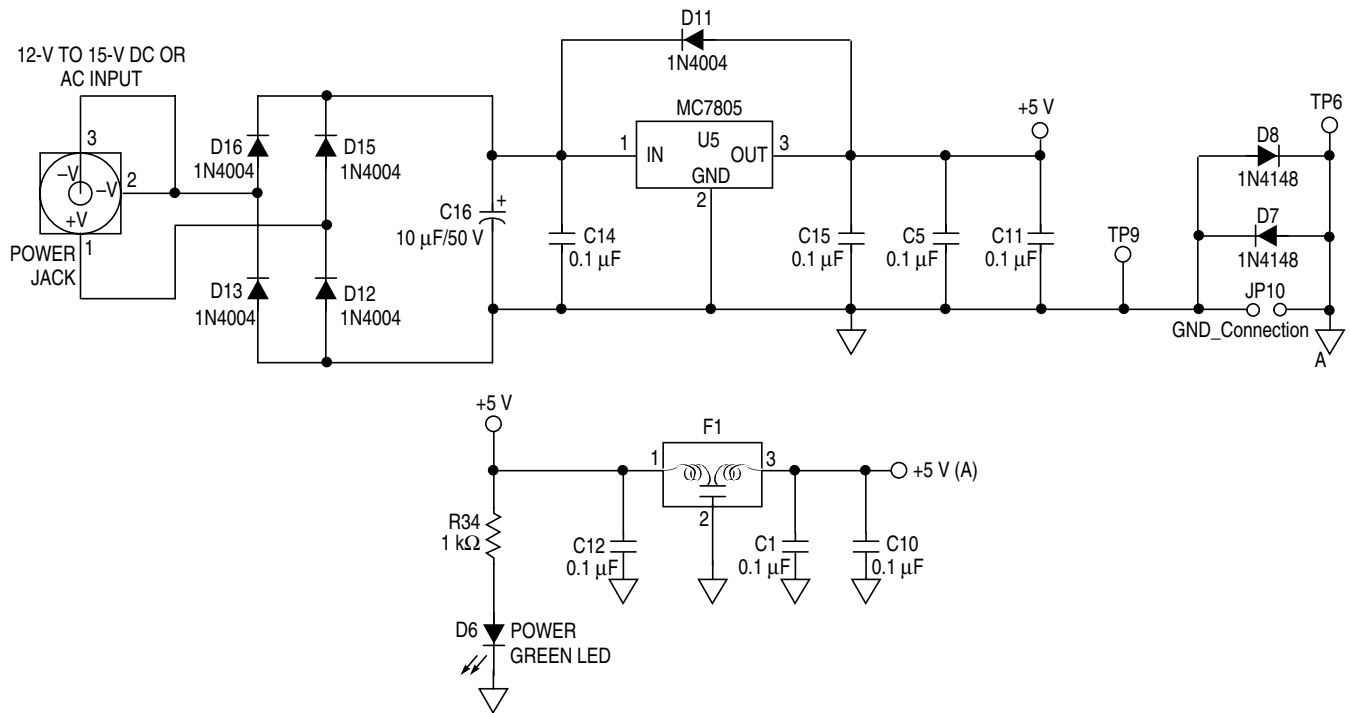


Figure 5-3. On-Board Power Supply

5.8 Optoisolated RS232 Interface

RS232 serial communication is provided by the circuit in [Figure 5-4](#). It is optically isolated for safety and is suitable for communication rates up to 9600 baud.

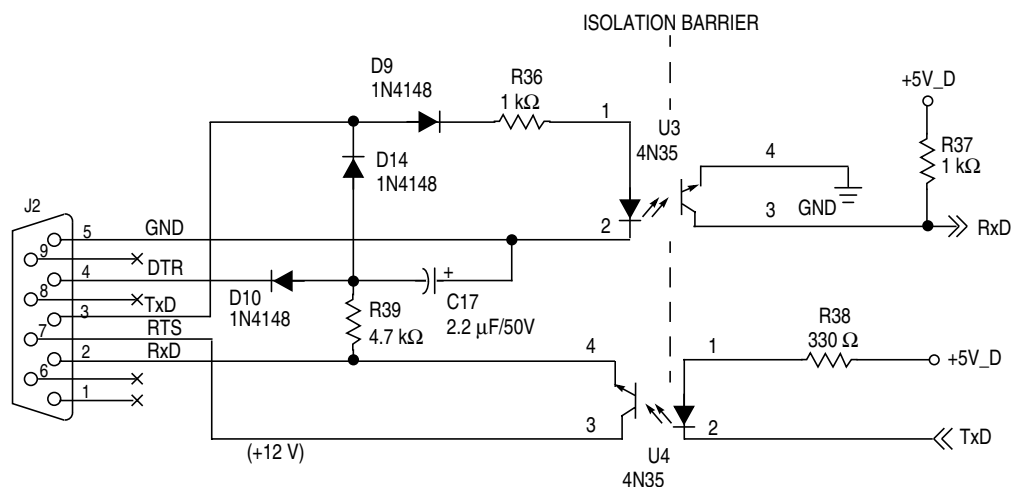


Figure 5-4. RS232 Interface

The EIA RS232 specification states that signal levels can range from ± 3 volts to ± 25 volts. A mark is defined as a signal that ranges from -3 volts to -25 volts. A space is defined as a signal that ranges from $+3$ volts to $+25$ volts. Therefore, to meet the RS232 specification, signals to and from a terminal must transition through 0 volts as they change from a mark to a space. Breaking the isolated RS232 circuit into input and output sections makes explanation of the circuit simpler.

Input interface is through opto coupler U3. To send data from a PC through U3, it is necessary to satisfy the PWMFREQ_RxD input to the MC3PHAC. In the idle condition, the PWMFREQ_RxD input must be at a logic 1. To accomplish that, the transistor in U3 must be off. The idle state of the transmit data line (TXD) on the PC serial port is a mark (-3 V to -25 V). Therefore, the diode in U3 is off and the transistor in U3 is off, yielding a logic 1 to the SCI input. When the start bit is sent to the PWMFREQ_RxD input from the PC's serial port, the PC's TXD transitions from a mark to a space ($+3$ V to $+25$ V), forward biasing the diode in U3. Forward biasing the diode in D9 turns on the transistor in U3, providing a logic 0 to the input of the SCI. Simply stated, the input half of the circuit provides input isolation, signal inversion, and level

shifting from the PC to the MC3PHAC's PWMFREQ_RxD pin. An RS232 line receiver, such as an MC1489, serves the same purpose without the optoisolation function.

To send data from the M3PHAC's RETRY_TxD pin to a PC serial port input, it is necessary to satisfy the PC's receive data (RXD) input requirements. In an idle condition, the RXD input to the PC must be at mark (-3 V to -25 V). The data terminal ready output (DTR) on the PC outputs a mark when the port is initialized. The request to send RTS output is set to a space ($+3\text{ V}$ to $+25\text{ V}$) when the PC's serial port is initialized. Because the interface is half-duplex, the PC's TXD output is also at a mark, as it is idle. The idle state of the transmit data line (RETRY_TxD) on the MC3PHAC's serial port is a logic 1. The logic 1 out of the serial port output port forces the diode in U4 to be turned off. With the diode in U4 turned off, the transistor in U4 is also turned off. The junction of D10 and D14 are at a mark (-3 V to -25 V). With the transistor in U4 turned off, the input is pulled to a mark through current limiting resistor R39, satisfying the PC's serial input in an idle condition. When a start bit is sent from the MC3PHAC's serial port, the output of the MC3PHAC's serial port transitions to a logic 0. That logic 0 turns on the diode in U5, thus turning on the transistor in U5. The conducting transistor in U5 passes the voltage output from the PC's RTS output, that is now at a space ($+3\text{ V}$ to $+25\text{ V}$) to the PC's receive data (RXD) input. Capacitor C17 is a bypass capacitor used to "stiffen" the mark signal. The output half of the circuit provides output isolation, signal inversion, and level shifting from the MC3PHAC's serial output port to the PC's serial port. An RS232 line driver, such as an MC1488, serves the same purpose without the optoisolation function.

Appendix A. MC3PHAC Data Sheet



Overview

The MC3PHAC is a high-performance monolithic intelligent motor controller designed specifically to meet the requirements for low-cost, variable-speed, 3-phase ac motor control systems. The device is adaptable and configurable, based on its environment. It contains all of the active functions required to implement the control portion of an open loop, 3-phase ac motor drive.

One of the unique aspects of this device is that although it is adaptable and configurable based on its environment, it does not require any software development. This makes the MC3PHAC a perfect fit for customer applications requiring ac motor control but with limited or no software resources available.

The device features are:

- Volts-per-Hertz speed control
- Digital signal processing (DSP) filtering to enhance speed stability
- 32-bit calculations for high-precision operation
- Internet enabled
- No user software development required for operation
- 6-output pulse-width modulator (PWM)
- 3-phase waveform generation
- 4-channel analog-to-digital converter (ADC)
- User configurable for standalone or hosted operation
- Dynamic bus ripple cancellation
- Selectable PWM polarity and frequency
- Selectable 50/60 Hz base frequency
- Phase-lock loop (PLL) based system oscillator
- Serial communications interface (SCI)
- Low-power supply voltage detection circuit

Included in the MC3PHAC are protective features consisting of dc bus voltage monitoring and a system fault input that will immediately disable the PWM module upon detection of a system fault.

Some target applications for the MC3PHAC include:

- Low horsepower HVAC motors
- Home appliances
- Commercial laundry and dishwashers
- Process control
- Pumps and fans

As shown in [Table 1](#), the MC3PHAC is offered in these packages:

- Plastic 28-pin dual in-line package (DIP)
- Plastic 28-pin small outline integrated circuit (SOIC)
- Plastic 32-pin quad flat pack (QFP)

See [Figure 1](#) and [Figure 2](#) for the pin connections.

Table 1. Ordering Information

| Device | Operating Temperature Range | Package |
|------------|-----------------------------|---------------------|
| MC3PHACVP | –40°C to +105°C | Plastic 28-pin DIP |
| MC3PHACVDW | –40°C to +105°C | Plastic 28-pin SOIC |
| MC3PHACVFA | –40°C to +105°C | Plastic 32-pin QFP |

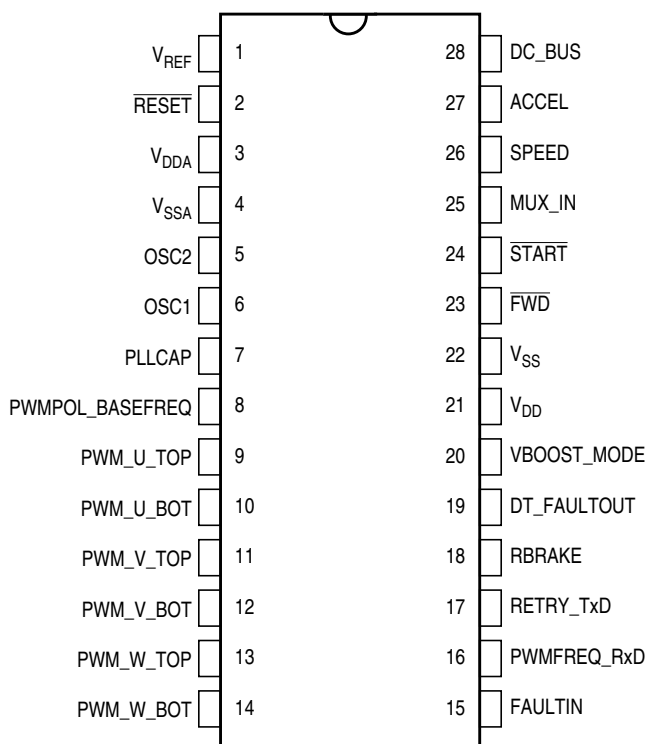


Figure 1. Pin Connections for PDIP and SOIC

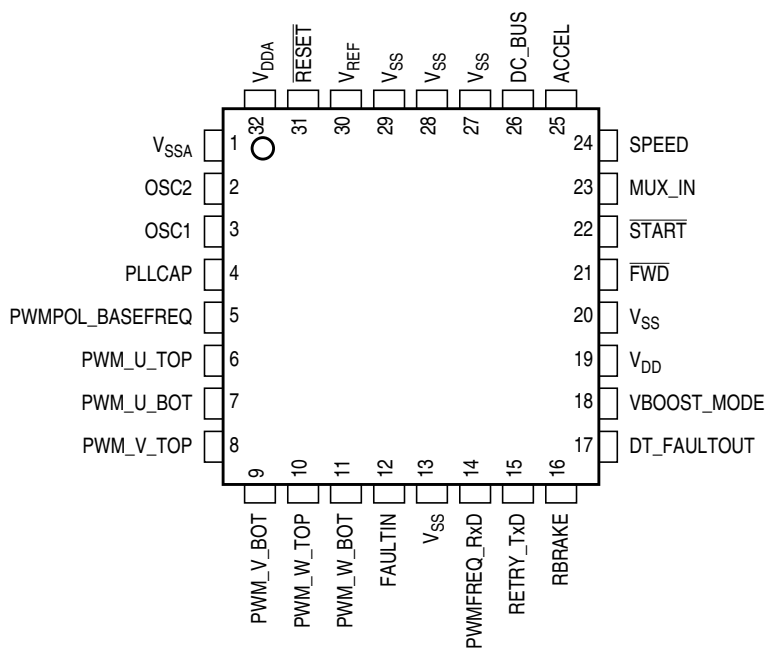


Figure 2. Pin Connections for QFP

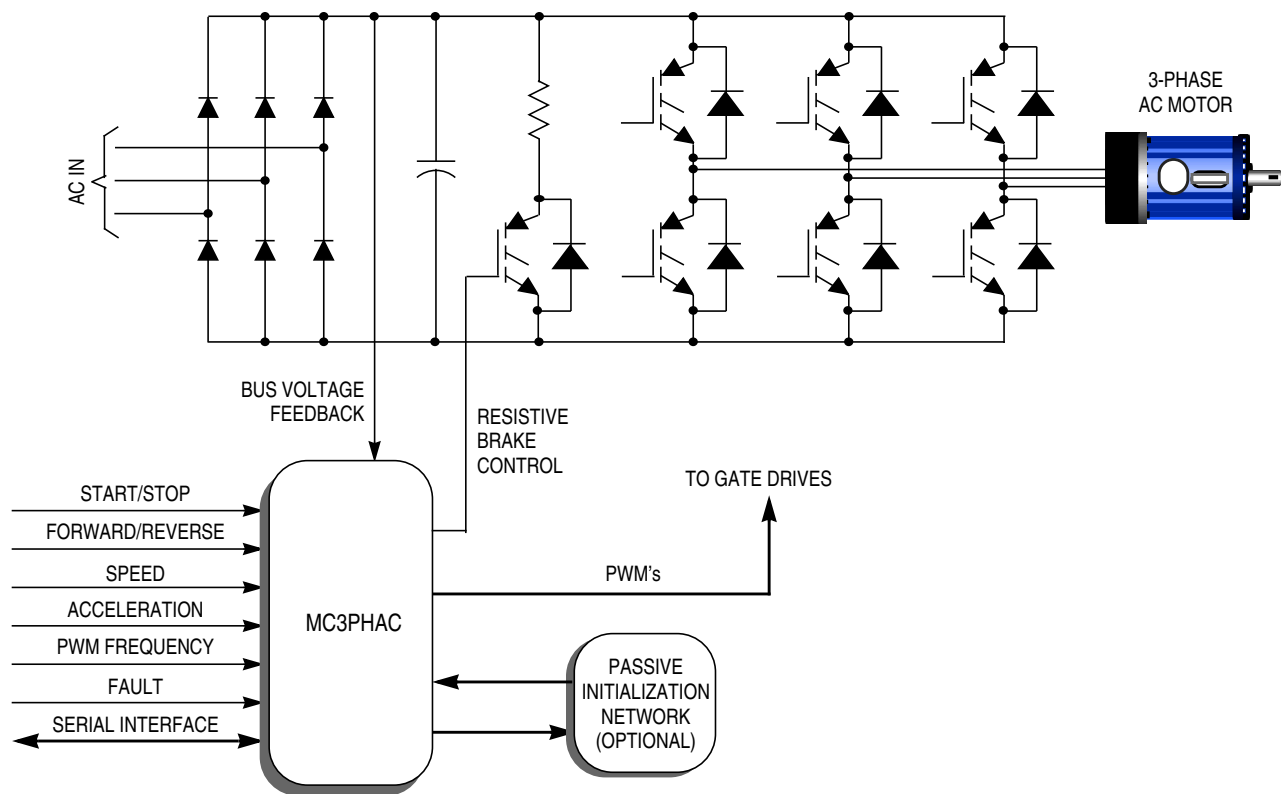


Figure 3. MC3PHAC-Based Motor Control System

Electrical Characteristics

Maximum Ratings

| Characteristic ⁽¹⁾ | Symbol | Value | Unit |
|---|------------|------------------------|------|
| Supply voltage | V_{DD} | −0.3 to +6.0 | V |
| Input voltage | V_{In} | −0.3 to $V_{DD} + 0.3$ | V |
| Input high voltage | V_{Hi} | $V_{DD} + 0.3$ | V |
| Maximum current per pin excluding V_{DD} and V_{SS} | I | 25 | mA |
| Storage temperature | T_{stg} | −55 to +150 | °C |
| Maximum current out of V_{SS} | IMV_{SS} | 100 | mA |
| Maximum current into V_{DD} | IMV_{DD} | 100 | mA |

1. Voltages referenced to V_{SS}

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{In} and V_{Out} be constrained to the range $V_{SS} \leq (V_{In} \text{ or } V_{Out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}).

Functional Operating Range

| Characteristic | Symbol | Value | Unit |
|---|----------|-----------------|------|
| Operating temperature range (see Table 1) | T_A | −40°C to +105°C | °C |
| Operating voltage range | V_{DD} | $5.0 \pm 10\%$ | V |

Control Timing

| Characteristic | Symbol | Value | Unit |
|-------------------------------------|-----------|----------------|------|
| Oscillator frequency ⁽¹⁾ | F_{osc} | $4.00 \pm 1\%$ | MHz |

1. Follow the crystal/resonator manufacturer's recommendations, as the crystal/resonator parameters determine the external component values required for maximum stability and reliable starting. The load capacitance values used in the oscillator circuit design should include all stray capacitances.

DC Electrical Characteristics

| Characteristic ⁽¹⁾ | Symbol | Min | Max | Unit |
|---|-----------------------|---------------------|---------------------|----------|
| Output high voltage ($I_{Load} = -2.0$ mA) All I/O pins except RBRAKE | V_{OH} | $V_{DD} - 0.8$ | — | V |
| Output high voltage RBRAKE ($I_{RBRAKE} = -15.0$ mA) | V_{OHRB} | $V_{DD} - 1.0$ | — | V |
| Output low voltage ($I_{Load} = 1.6$ mA) All I/O pins except FAULTOUT and RETRY/TxD | V_{OL} | — | 0.4 | V |
| Output low voltage ($I_{Load} = 15$ mA) FAULTOUT and RETRY/TxD | V_{OL1} | — | 1.0 | V |
| Input high voltage All ports | V_{Hi} | $0.7 \times V_{DD}$ | V_{DD} | V |
| Input low voltage All ports | V_{IL} | V_{SS} | $0.3 \times V_{DD}$ | V |
| V_{DD} supply current | I_{DD} | — | 60 | mA |
| I/O ports high-impedance leakage current | I_{IL} | — | ± 5 | μ A |
| Input current | I_{In} | — | ± 1 | μ A |
| Capacitance Ports (as input or output) | C_{Out} C_{In} | — — | 12 8 | pF |
| V_{DD} low-voltage inhibit reset | V_{LVR1} | 3.80 | 4.3 | V |
| V_{DD} low-voltage reset/recovery hysteresis | V_{LVH1} | 50 | 150 | mV |
| V_{DD} power-on reset re-arm voltage | V_{POR} | 3.85 | 4.45 | V |
| V_{DD} power-on reset rise time ramp rate | R_{POR} | 0.035 | — | V/ms |
| Serial communications interface baud rate | SCI_{BD} | 9504 | 9696 | Bits/sec |
| Voltage Boost ⁽²⁾ | V_{Boost} | 0 | 100 | % |
| Dead time range ⁽³⁾ | DT_{Range} | 0 | 31.875 | μ s |
| Retry time ⁽⁴⁾ | RT_{Time} | 0 | 4.55 | Hours |
| Acceleration rate | AC_{Rate} | 0.5 | 128 | Hz/sec |
| Speed control | $SPEED$ | 1 | 128 | Hz |
| PWM Frequency | PWM_{FREQ} | 5.291 | 21.164 | kHz |
| High side power transistor drive pump-up time | T_{Pump} | 99 | 101 | ms |

1. $V_{DD} = 5.0$ Vdc $\pm 10\%$

2. Limited in standalone mode to 0 to 35%

3. Limited in standalone mode to 0.5 to 6.0 μ s

4. Limited in standalone mode to 0 to ~53 seconds

Pin Descriptions

Table 2 is a pin-by-pin functional description of the MC3PHAC. The pin numbers in the table refer to the 28-pin packages (see **Figure 1**).

Table 2. MC3PHAC Pin Descriptions (Sheet 1 of 3)

| Pin Number | Pin Name | Pin Function |
|------------|--------------------|--|
| 1 | V_{REF} | Reference voltage input for the on-chip ADC. For best signal-to-noise performance, this pin should be tied to V_{DDA} (analog). |
| 2 | \overline{RESET} | A logic 0 on this pin forces the MC3PHAC to its initial startup state. All PWM outputs are placed in a high-impedance mode. Reset is a bidirectional pin, allowing a reset of the entire system. It is driven low when an internal reset source is asserted (for example, loss of clock or low V_{DD}). |
| 3 | V_{DDA} | Provides power for the analog portions of the MC3PHAC, which include the internal clock generation circuit (PLL) and the ADC |
| 4 | V_{SSA} | Returns power for the analog portions of the MC3PHAC, which include the internal clock generation circuit (PLL) and the ADC |
| 5 | OSC2 | Oscillator output used as part of a crystal or ceramic resonator clock circuit. ⁽¹⁾ |
| 6 | OSC1 | Oscillator input used as part of a crystal or ceramic resonator clock circuit. Can also accept a signal from an external canned oscillator. ⁽¹⁾ |
| 7 | PLLCAP | A capacitor from this pin to ground affects the stability and reaction time of the PLL clock circuit. Smaller values result in faster tracking of the reference frequency. Larger values result in better stability. A value of 0.1 μF is typical. |
| 8 | PWMPOL_BASEFREQ | Input which is sampled at specific moments during initialization to determine the PWM polarity and the base frequency (50 or 60 Hz) |
| 9 | PWM_U_TOP | PWM output signal for the top transistor driving motor phase U |
| 10 | PWM_U_BOT | PWM output signal for the bottom transistor driving motor phase U |
| 11 | PWM_V_TOP | PWM output signal for the top transistor driving motor phase V |
| 12 | PWM_V_BOT | PWM output signal for the bottom transistor driving motor phase V |
| 13 | PWM_W_TOP | PWM output signal for the top transistor driving motor phase W |
| 14 | PWM_W_BOT | PWM output signal for the bottom transistor driving motor phase W |

Table 2. MC3PHAC Pin Descriptions (Sheet 2 of 3)

| Pin Number | Pin Name | Pin Function |
|------------|---------------------------|--|
| 15 | FAULTIN | A logic high on this input will immediately disable the PWM outputs. A retry timeout interval will be initiated once this pin returns to a logic low state. |
| 16 | PWMFREQ_RxD | In standalone mode, this pin is an output that drives low to indicate the parameter mux input pin is reading an analog voltage to specify the desired PWM frequency. In PC master software mode, this pin is an input which receives UART serial data. |
| 17 | RETRY_TxD | In standalone mode, this pin is an output that drives low to indicate the parameter mux input pin is reading an analog voltage to specify the time to wait after a fault before re-enabling the PWM outputs. In PC master software mode, this pin is an output that transmits UART serial data. |
| 18 | RBRAKE | Output which is driven to a logic high whenever the voltage on the dc bus input pin exceeds a preset level, indicating a high bus voltage. This signal is intended to connect a resistor across the dc bus capacitor to prevent excess capacitor voltage. |
| 19 | DT_FAULTOUT | In standalone mode, this pin is an output which drives low to indicate the parameter mux input pin is reading an analog voltage to specify the dead-time between the on states of the top and bottom PWM signals for a given motor phase. In PC master software mode, this pin is an output which goes low whenever a fault condition occurs. |
| 20 | VBOOST_MODE | At startup, this input is sampled to determine whether to enter standalone mode (logic high) or PC master software mode (logic low). In standalone mode, this pin is also used as an output that drives low to indicate the parameter mux input pin is reading an analog voltage to specify the amount of voltage boost to apply to the motor. |
| 21 | V _{DD} | +5-volt digital power supply to the MC3PHAC |
| 22 | V _{SS} | Digital power supply ground return for the MC3PHAC |
| 23 | $\overline{\text{FWD}}$ | Input which is sampled to determine whether the motor should rotate in the forward or reverse direction |
| 24 | $\overline{\text{START}}$ | Input which is sampled to determine whether the motor should be running. |
| 25 | MUX_IN | In standalone mode, during initialization this pin is an output that is used to determine PWM polarity and base frequency. Otherwise, it is an analog input used to read several voltage levels that specify MC3PHAC operating parameters. |

Table 2. MC3PHAC Pin Descriptions (Sheet 3 of 3)

| Pin Number | Pin Name | Pin Function |
|------------|----------|--|
| 26 | SPEED | In standalone mode, during initialization this pin is an output that is used to determine PWM polarity and base frequency. Otherwise, it is an analog input used to read a voltage level corresponding to the desired steady-state speed of the motor. |
| 27 | ACCEL | In standalone mode, during initialization this pin is an output that is used to determine PWM polarity and base frequency. Otherwise, it is an analog input used to read a voltage level corresponding to the desired acceleration of the motor. |
| 28 | DC_BUS | In standalone mode, during initialization this pin is an output that is used to determine PWM polarity and base frequency. Otherwise, it is an analog input used to read a voltage level proportional to the dc bus voltage. |

1. Correct timing of the MC3PHAC is based on a 4.00 MHz crystal or ceramic resonator. Follow the crystal/resonator manufacturer's recommendations, as the crystal/resonator parameters determine the external component values required for maximum stability and reliable starting. The load capacitance values used in the oscillator circuit design should include all stray capacitances.

Introduction

The MC3PHAC is a high-performance intelligent controller designed specifically to meet the requirements for low-cost, variable-speed, 3-phase ac motor control systems. The device is adaptable and configurable, based on its environment. Constructed with high-speed CMOS (complementary metal-oxide semiconductor) technology, the MC3PHAC offers a high degree of performance and ruggedness in the hostile environments often found in motor control systems.

The device consists of:

- 6-output pulse-width modulator (PWM)
- 4-channel analog-to-digital converter (ADC)
- Phase-lock loop (PLL) based system oscillator
- Low-power supply voltage detection circuit
- Serial communications interface (SCI)

The serial communications interface is used in a mode, called PC master software mode, whereby control of the MC3PHAC is from a host or master personal computer executing PC master software or a microcontroller emulating PC master software commands. In either case, control via the internet is feasible.

Included in the MC3PHAC are protective features consisting of dc bus monitoring and a system fault input that will immediately disable the PWM module upon detection of a system fault.

Included motor control features include:

- Open loop volts/Hertz speed control
- Forward or reverse rotation
- Start/stop motion
- System fault input
- Low-speed voltage boost
- Internal power-on reset (POR)

Features

3-Phase Waveform Generation — The MC3PHAC generates six PWM signals which have been modulated with variable voltage and variable frequency information in order to control a 3-phase ac motor. A third harmonic signal has been superimposed on top of the fundamental motor frequency to achieve full bus voltage utilization. This results in a 15 percent increase in maximum output amplitude compared to pure sine wave modulation.

The waveform is updated at a 5.3 kHz rate (except when the PWM frequency is 15.9 kHz), resulting in near continuous waveform quality. At 15.9 kHz, the waveform is updated at 4.0 kHz.

DSP Filtering — A 24-bit IIR digital filter is used on the SPEED input signal in standalone mode, resulting in enhanced speed stability in noisy environments. The sampling period of the filter is 3 ms (except when the PWM frequency is 15.9 kHz) and it mimics the response of a single pole analog filter having a pole at 0.4 Hz. At a PWM frequency of 15.9 kHz, the sampling period is 4 ms and the pole is located at 0.3 Hz.

High Precision Calculations — Up to 32-bit variable resolution is employed for precision control and smooth performance. For example, the motor speed can be controlled with a resolution of 4 mHz.

Smooth Voltage Transitions — When the commanded speed of the motor passes through ± 1 Hz, the voltage is gently applied or removed depending on the direction of the speed change. This eliminates any pops or surges that may occur, especially under conditions of high-voltage boost at low frequencies.

High-Side Bootstrapping — Many motor drive topologies (especially high-voltage drives) use optocouplers to supply the PWM signal to the high-side transistors. Often, the high-side transistor drive circuitry contains a charge pump circuit to create a floating power supply for each high-side transistor that is dependent on low-side PWMs to develop power. When the motor has been off for a period of time, the charge on the high-side power supply capacitor is depleted and must be replenished before proper PWM operation can resume.

To accommodate such topologies, the MC3PHAC will always provide 100 ms of 50 percent PWM drive to only the low-side transistors each time the motor is turned on. Since the top transistors remain off during this time, it has the effect of applying zero volts to the motor, and no motion occurs. After this period, motor waveform modulation begins, with PWM drive also being applied to the high-side transistors.

Fast Velocity Updating — During periods when the motor speed is changing, the rate at which the velocity is updated is critical to smooth operation. If these updates occur too infrequently, a ratcheting effect will be exhibited on the motor, which inhibits smooth torque performance. However, velocity profiling is

a very calculation intensive operation to perform, which runs contrary to the previous requirement.

In the MC3PHAC, a velocity pipelining technique is employed which allows linear interpolation of the velocity values, resulting in a new velocity value every 189 μs (252 μs for 15.9 kHz PWMs). The net result is ultra smooth velocity transitions, where each velocity step is not perceivable by the motor.

Dynamic Bus Ripple Cancellation — The dc bus voltage is sensed by the MC3PHAC, and any deviations from a predetermined norm (3.5 V on the dc bus input pin) result in corrections to the PWM values to counteract the effect of the bus voltage changes on the motor current. The frequency of this calculation is sufficiently high to permit compensation for line frequency ripple, as well as slower bus voltage changes resulting from regeneration or brown out conditions. See [Figure 4](#).

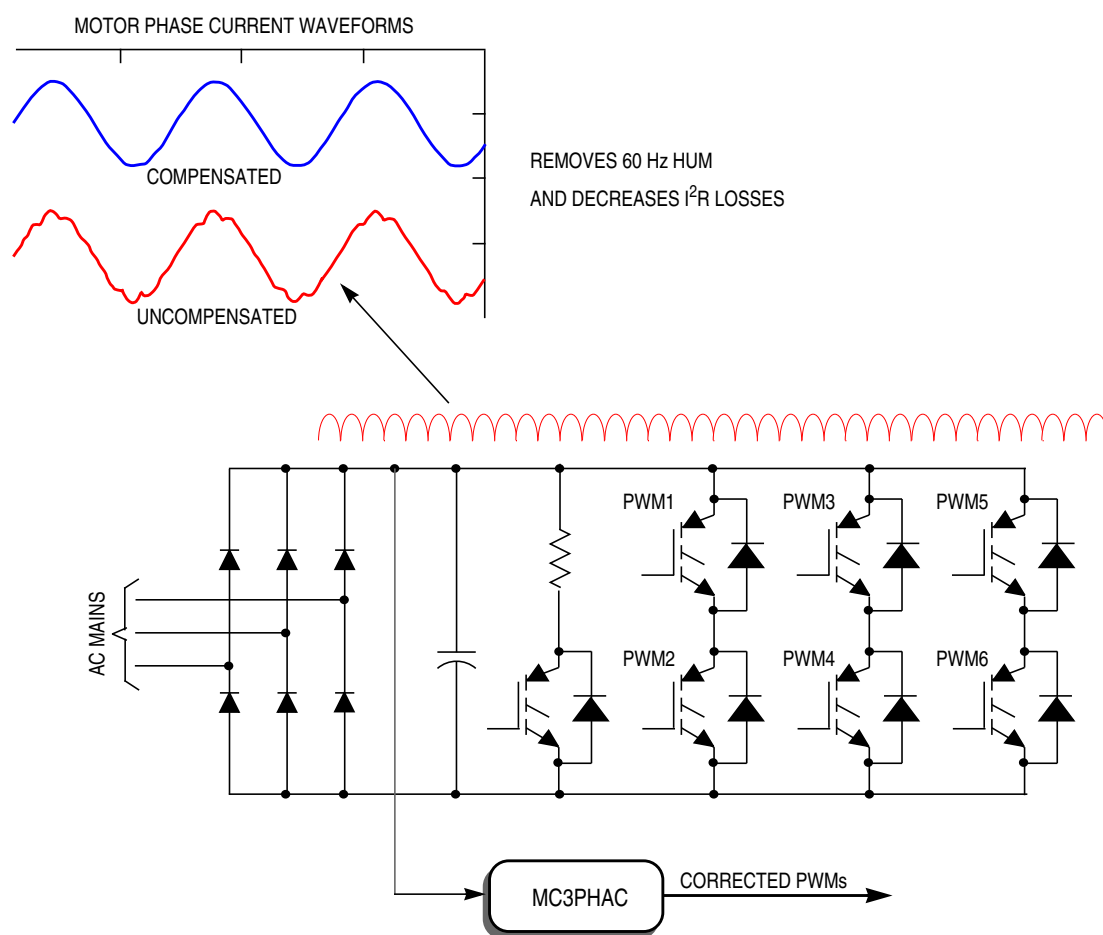


Figure 4. Dynamic Bus Ripple Cancellation

Selectable Base Frequency — Alternating current (ac) motors are designed to accept rated voltage at either 50 or 60 Hz, depending on what region of the world they were designed to be used. The MC3PHAC can accommodate both types of motors by allowing the voltage profile to reach maximum value at either 50 or 60 Hz. This parameter can be specified at initialization in standalone mode, or it can be changed at any time in PC master software mode.

Selectable PWM Polarity — The polarity of the PWM outputs may be specified such that a logic high on a PWM output can either be the asserted or negated state of the signal. In standalone mode, this parameter is specified at initialization and applies to all six PWM outputs. In PC master software mode, the polarity of the top PWM signals can be specified separately from the polarity of the bottom PWM signals.

This specification can be done at any time, but once it is done, the polarities are locked and cannot be changed until a reset occurs. Also, any commands from PC master software that would have the effect of enabling PWMs are prevented by the MC3PHAC until the polarity has been specified.

In standalone mode, the base frequency and PWM polarity are specified at the same time during initialization by connecting either pin 25, 26, 27, or 28 exclusively to the PWMPOL_BASEFREQ input. During initialization, pins 25, 26, 27, and 28 are cycled one at a time to determine which one has been connected to the PWMPOL_BASEFREQ input.

Table 3 shows the selected PWM polarity and base frequency as a function of which pin connection is made. Refer to the standalone mode schematic, **Figure 8**. Only one of these jumpers (JP1–JP4) can be connected at any one time.

NOTE: *It is not necessary to break this connection once the initialization phase has been completed. The MC3PHAC will function properly while this connection is in place.*

**Table 3. PWM Polarity and Base Frequency
Specification in Standalone Mode**

| Pin Connected to PWMPOL_BASEFREQ Pin | PWM Polarity | Base Frequency |
|---|-----------------|-------------------|
| MUX_IN (JP1) | Logic low = on | 50 Hz |
| SPEED (JP2) | Logic high = on | 50 Hz |
| ACCEL (JP3) | Logic low = on | 60 Hz |
| DC_BUS (JP4) | Logic high = on | 60 Hz |

Selectable PWM Frequency — The MC3PHAC accommodates four discrete PWM frequencies and can be changed dynamically while the motor is running. This resistor can be a potentiometer or a fixed resistor in the range shown in [Table 4](#). In standalone mode, the PWM frequency is specified by applying a voltage to the MUX_IN pin while the PWMFREQ_RxD pin is being driven low. [Table 4](#) shows the required voltage levels on the MUX_IN pin and the associated PWM frequency for each voltage range.

NOTE: *The PWM frequencies are based on a 4.00 MHz frequency applied to the oscillator input.*

**Table 4. MUX_IN Resistance Ranges
and Corresponding PWM Frequencies**

| Voltage Input | PWM Frequency |
|---------------|---------------|
| 0 to 1 V | 5.291 kHz |
| 1.5 to 2.25 V | 10.582 kHz |
| 2.75 to 3.5 V | 15.873 kHz |
| 4 to 5 V | 21.164 kHz |

Selectable PWM Dead Time — Besides being able to specify the PWM frequency, the blanking time interval between the on states of the complementary PWM pairs can also be specified. Refer to the graph in [Figure 9](#) for the resistance value versus dead time. [Figure 9](#) assumes a $6.8\text{ k}\Omega \pm 5\%$ pullup resistor. In standalone mode, this is done by

supplying a voltage to the MUX_IN pin while the DT_FAULTOUT pin is being driven low. In this way, dead time can be specified with a scaling factor of $2.075\text{ }\mu\text{s}$ per volt, with a minimum value of $0.5\text{ }\mu\text{s}$. In PC master software mode, this value can be selected to be anywhere between 0 and $32\text{ }\mu\text{s}$.

In both standalone and PC master software modes, the dead time value can be written only once. Further updates of this parameter are locked out until a reset condition occurs.

Speed Control — The synchronous motor frequency can be specified in real time to be any value from 1 Hz to 128 Hz by the voltage applied to the SPEED pin. The scaling factor is 25.6 Hz per volt. This parameter can also be controlled directly from PC master software in real time.

The SPEED pin is processed by a 24-bit digital filter to enhance the speed stability in noisy environments. This filter is only activated in standalone mode.

Acceleration Control — Motor acceleration can be specified in real time to be in the range from 0.5 Hz/second, ranging to 128 Hz/second, by the voltage applied to the ACCEL pin. The scaling factor is 25.6 Hz/second per volt. This parameter can also be controlled directly from PC master software in real time.

Voltage Profile Generation — The MC3PHAC controls the motor voltage in proportion to the specified frequency, as indicated in [Figure 5](#).

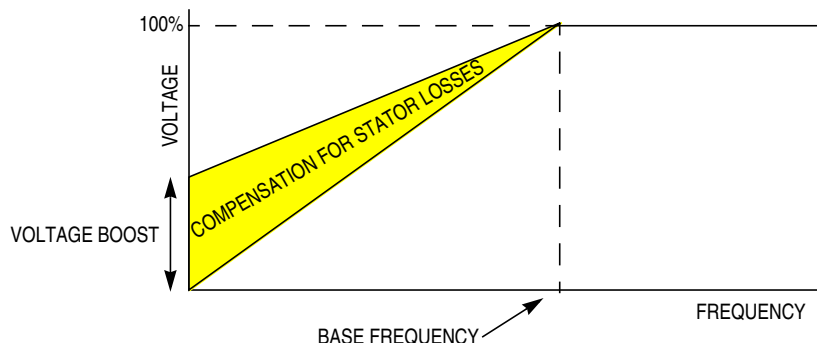


Figure 5. Voltage Profiling, Including Voltage Boost

An ac motor is designed to draw a specified amount of magnetizing current when supplied with rated voltage at the base frequency. As the frequency decreases, assuming no stator losses, the voltage must decrease in exact proportion to maintain the required magnetizing current. In reality, as the frequency decreases, the voltage drop in the series stator resistance increases in proportion to the voltage across the magnetizing inductance. This has the effect of further reducing the voltage across the magnetizing inductor, and consequently, the magnetizing current. A schematic representation of this effect is illustrated in [Figure 6](#). To compensate for this voltage loss, the voltage profile is boosted over the normal voltage curve in [Figure 5](#), so that the magnetizing current remains constant over the speed range.

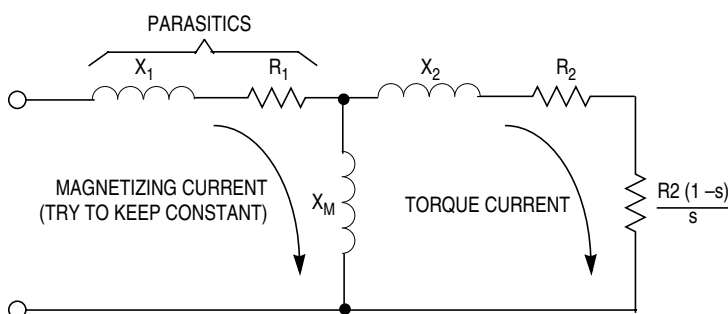


Figure 6. AC Motor Single Phase Model Showing Parasitic Stator Impedances

The MC3PHAC allows the voltage boost to be specified as a percentage of full voltage at 0 Hz, as shown in [Figure 5](#). In standalone mode, voltage boost is specified during the initialization phase by supplying a voltage to the MUX_IN pin while the VBOOST_MODE pin is being driven low. Refer to the graph in [Figure 11](#) for the resistance value versus voltage boost. [Figure 11](#) assumes a 6.8 k Ω pullup resistor. In this way, voltage boost can be specified from 0 to 40 percent, with a scaling factor of 8 percent per volt. In PC master software mode, the voltage boost can be specified from 0 to 100 percent and can be changed at anytime.

By using the voltage boost value, and the specified base frequency, the MC3PHAC has all the information required to generate a voltage profile automatically based on the generated waveform frequency. An additional feature exists in PC master software mode whereby this voltage value can be overridden and controlled in real time. Specifying a voltage lower than the normal volts-per-hertz profile permits a softer torque response in certain ergonomic situations. It also allows for load power factor control and higher operating efficiencies with high inertia loads or other loads where instantaneous changes in torque demand are not permitted. Details of this feature are discussed in the [PC Master Software Operation with the MC3PHAC](#).

PLL Clock Generation — The OSC1 pin signal is used as a reference clock for an internal PLL clocking circuit, which is used to drive the internal clocks of the MC3PHAC. This provides excellent protection against noise spikes that may occur on the OSC1 pin. In a clocking circuit that does not incorporate a PLL, a noise spike on the clock input can create a clock edge, which violates the setup times of the clocking logic, and can cause the device to malfunction. The same noise spike applied to the input of a PLL clock circuit is perceived by the PLL as a change in its reference frequency, and the PLL output frequency begins to change in an attempt to lock on to the new frequency. However, before any appreciable change can occur, the spike is gone, and the PLL settles back into the true reference frequency.

Fault Protection — The MC3PHAC supports an elaborate range of fault protection and prevention features. If a fault does occur, the MC3PHAC immediately disables the PWMs and waits until the fault condition is cleared before starting a timer to re-enable the PWMs. Refer to the graph in [Figure 10](#) for the resistance value versus retry time. [Figure 10](#) assumes a 6.8 k Ω pullup resistor. In standalone mode, this timeout interval is specified during the initialization phase by supplying a voltage to the MUX_IN pin while the RETRY_TxD pin is being driven low. In this way, the retry time can be specified from 1 to 60 seconds, with a scaling factor of 12 seconds per volt. In PC master software mode, the retry time can be specified from 0.25 second to over 4.5 hours and can be changed at any time.

The fault protection and prevention features are:

- **External Fault Monitoring** — The FAULTIN pin accepts a digital signal that indicates a fault has been detected via external monitoring circuitry. A high level on this input results in the PWMs being immediately disabled. Typical fault conditions might be a dc bus over voltage, bus over current, or over temperature. Once this input returns to a logic low level, the fault retry timer begins running, and PWMs are re-enabled after the programmed timeout value is reached.
- **Lost Clock Protection** — If the signal on the OSC1 pin is lost altogether, the MC3PHAC will immediately disable the PWM outputs to protect the motor and power electronics. This is a special fault condition in that it will also cause the MC3PHAC to be reset. Lost clock detection is an important safety consideration, as many safety regulatory agencies are now requiring a dead crystal test be performed as part of the certification process.
- **Low V_{DD} Protection** — Whenever V_{DD} falls below V_{LVR1} , an on-board power supply monitor will reset the MC3PHAC. This allows the MC3PHAC to operate properly with 5 volt power supplies of either 5 or 10 percent tolerance.
- **Bus Voltage Integrity Monitoring** — The DC_BUS pin is monitored at a 5.3 kHz frequency (4.0 kHz when the PWM frequency is set to 15.9 kHz), and any voltage reading outside of an acceptable window constitutes a fault condition. In standalone mode, the window thresholds are fixed at 4.47 volts (128 percent of nominal), and 1.75 volts (50 percent of nominal), where nominal is defined to be 3.5 volts. In PC master software mode, both top and bottom window thresholds can be set independently to any value between 0 volts (0 percent of nominal), and greater than 5 volts (143 percent of nominal), and can be changed at any time. Once the DC_BUS signal level returns to a value within the acceptable window, the fault retry timer begins running, and PWMs are re-enabled after the programmed timeout value is reached.

During power-up, it is possible that V_{DD} could reach operating voltage before the dc bus capacitor charges up to its nominal value. When the dc bus integrity is checked, an under voltage would be detected and treated as a fault, with its associated timeout period. To prevent this, the MC3PHAC monitors the dc bus voltage during power-up in standalone mode, and waits until it is higher than the under voltage threshold before continuing. During this time, all MC3PHAC functions are suspended. Once this threshold is reached, the MC3PHAC will continue normally, with any further under voltage conditions treated as a fault.

If dc bus voltage monitoring is not desired, a voltage of 3.5 volts \pm 5 percent should be supplied to the DC_BUS pin through an impedance of between 4.7 k Ω and 15 k Ω .

- **Regeneration Control** — Regeneration is a process by which stored mechanical energy in the motor and load is transferred back into the drive electronics, usually as a result of an aggressive deceleration operation. In special cases where this process occurs frequently (for example, elevator motor control systems), it is economical to incorporate special features in the motor drive to allow this energy to be supplied back to the ac mains. However, for most low cost ac drives, this energy is stored in the dc bus capacitor by increasing its voltage. If this process is left unchecked, the dc bus voltage can rise to dangerous levels, which can destroy the bus capacitor or the transistors in the power inverter.

The MC3PHAC incorporates two techniques to deal with regeneration before it becomes a problem:

- **Resistive Braking** — The DC_BUS pin is monitored at a 5.3 kHz frequency (4.0 kHz when the PWM frequency is set to 15.9 kHz), and when the voltage reaches a certain threshold, the RBRAKE pin is driven high. This signal can be used to control a resistive brake placed across the dc bus capacitor, such that mechanical energy from the motor will be dissipated as heat in the resistor versus being stored as voltage on the capacitor. In standalone mode, the DC_BUS threshold required to assert the RBRAKE signal is fixed at 3.85 volts (110 percent of nominal) where nominal is defined to be 3.5 volts. In PC master software mode, this threshold can be set to any value between 0 volts (0 percent of nominal) and greater than 5 volts (143 percent of nominal) and can be changed at any time.
- **Automatic Deceleration Control** — When decelerating the motor, the MC3PHAC attempts to use the specified acceleration value for deceleration as well. If the voltage on the DC_BUS pin reaches a certain threshold, the MC3PHAC begins to moderate the deceleration as a function of this voltage, as shown in [Figure 7](#). The voltage range on the DC_BUS pin from when the deceleration begins to decrease, to when it reaches 0, is 0.62 volts. In standalone mode, the DC_BUS voltage where deceleration begins to decrease is fixed at 3.85 volts (110 percent of nominal) where nominal is defined to be 3.5 volts. In PC master software mode, this threshold can be set to any value between 0 volts (0 percent of nominal) and greater than 5 volts (143 percent of nominal) and can be changed at any time.

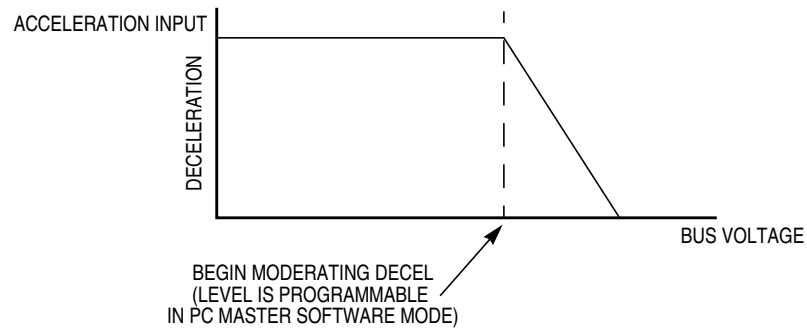


Figure 7. Deceleration as a Function of Bus Voltage

Digital Power Supply Bypassing

V_{DD} and V_{SS} are the digital power supply and ground pins for the MC3PHAC.

Fast signal transitions connected internally on these pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the V_{DD} and V_{SS} pins. Place the bypass capacitors as close as possible to the MC3PHAC. Use a high-frequency-response ceramic capacitor, such as a 0.1 μF , paralleled with a bulk capacitor in the range of 1 μF to 10 μF for bypassing the digital power supply.

Analog Power Supply Bypassing

V_{DDA} and V_{SSA} are the power supply pins for the analog portion of the clock generator and analog-to-digital converter (ADC). On the schematics in this document, analog ground is labeled with an A and other grounds are digital grounds. Analog power is labeled as +5 A. It is good practice to isolate the analog and digital +5 volt power supplies by using a small inductor or a low value resistor less than 5 ohms in series with the digital power supply, to create the +5 A supply. ADC V_{REF} is the power supply pin used for setting the ADC's voltage reference.

Decoupling of these pins should be per the digital power supply bypassing, described previously. ADC V_{REF} (pin 1) and V_{DDA} (pin 3) shall be connected together and connected to the same potential as V_{DD} .

Grounding Considerations

Printed circuit board layout is an important design consideration. In particular, ground planes and how grounds are tied together influence noise immunity. To maximize noise immunity, it is important to get a good ground plane under the MC3PHAC. It is also important to separate analog and digital grounds. That is why, shown on the schematics, there are two ground designations, analog ground is marked with an A and other grounds are digital grounds. GND is the digital ground plane and power supply return. GNDA is the analog circuit ground. They are both the same reference voltage, but are routed separately, and tie together at only one point.

Power-Up/Power-Down

When power is applied or removed, it is important that the inverter's top and bottom output transistors in the same phase are not turned on simultaneously. Since logic states are not always defined during power-up, it is important to ensure that all power transistors remain off when the controller's supply voltage is below its normal operating level. The MC3PHAC's PWM module outputs make this easy by switching to a high impedance configuration whenever the 5-volt supply is below its specified minimum.

The user should use pullup or pulldown resistors on the output of the MC3PHAC's PWM outputs to ensure during power-up and power-down, that the inverter's drive inputs are at a known, turned off, state.

Operation

The MC3PHAC motor controller will operate in two modes. The first is standalone operation, whereby the MC3PHAC can be used without any intervention from an external personal computer. In standalone mode, the MC3PHAC is initialized by passive devices connected to the MC3PHAC and input to the system at power-up/reset time. In standalone mode, some parameters continue to be input to the system as it operates. Speed, PWM frequency, bus voltage, and acceleration parameters are input to the system on a real-time basis.

The second mode of operation is called PC master software mode. That operational mode requires the use of a personal computer and PC master software executing on the personal computer, communicating with the MC3PHAC, or a microcontroller emulating PC master software commands. All command and setup information is input to the MC3PHAC via the PC host.

Standalone Operation

If the VBOOST_MODE pin is high when the MC3PHAC is powered up, or after a reset, the MC3PHAC enters standalone mode. In this mode of operation, the functionality of many of the MC3PHAC pins change so that the device can control a motor without requiring setup information from an external master. When operated in standalone mode, the MC3PHAC will drive certain pins corresponding to parameters which must be specified, while simultaneously monitoring the response on other pins.

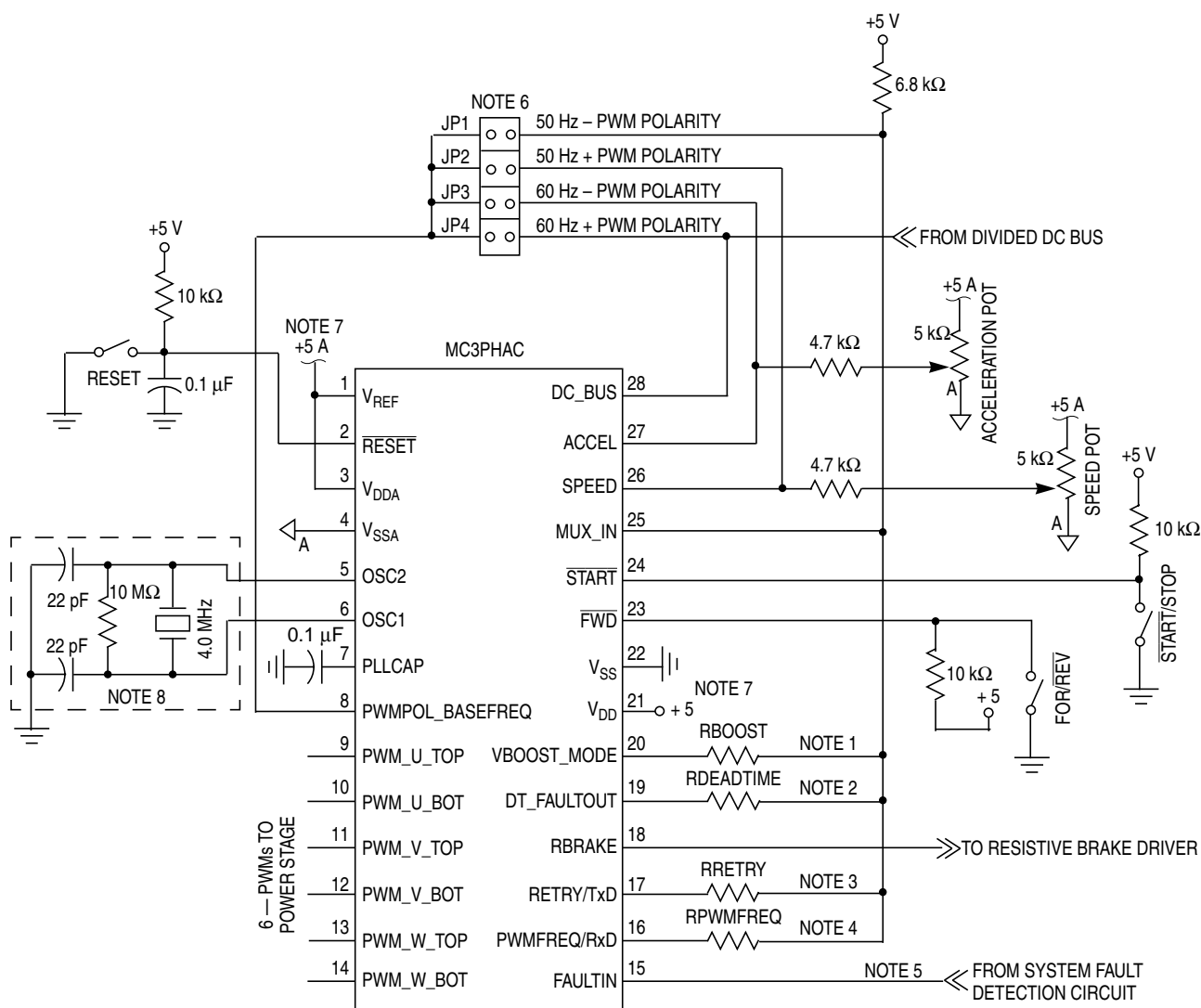
In many cases, the parameter to be specified is represented as an analog voltage presented to the MUX_IN pin, while certain other pins are driven low. In so doing, the MC3PHAC can accommodate an external analog mux which will switch various signals on the MUX_IN pin when the signal select line goes low. All signals must be in a range between 0 V and V_{REF} . As an economical alternative, an external passive network can be connected to each of the parameter select output pins and the MUX_IN pin, as shown in [Figure 8](#).

The Thevenin equivalent impedance of this passive network as seen by the MUX_IN pin is very important and should be in the range of 5 k Ω to 10 k Ω . If the resistance is too high, leakage current from the input/output (I/O) pins will cause an offset voltage that will affect the accuracy of the reading. If the resistance is too low, the parameter select pins will not be able to sink the required current for an accurate reading. Using a pullup resistor value of 6.8 k Ω (as indicated in [Figure 8](#)), the resulting value for each parameter as a function of the corresponding pulldown resistor value is shown in [Figure 9](#), [Figure 10](#), [Figure 11](#), and [Table 4](#).

The START input pin is debounced internally and a switch can be directly accommodated on this pin. The input is level sensitive, but a logic 1 level must exist on the pin before a logic 0 level will be processed as a start signal. This will prevent an accidental motor startup in the event of the MC3PHAC being powered up, where the switch was left in the start position.

The \overline{FWD} input pin is debounced internally and can directly accommodate a switch connection. The input is also level sensitive.

[Figure 8](#) shows the jumper arrangement connected to the PWMPOL_BASEFREQ input pin. For proper operation, one and only one jumper connection can be made at any given time. [Table 3](#) shows the polarity and base frequency selections as a function of the jumper connection.



Notes:

1. See [Figure 11](#).
2. See [Figure 9](#).
3. See [Figure 10](#).
4. See [Table 4](#).
5. If no external fault circuit is provided, connect to V_{SS} .
6. Connect only one jumper.
7. Use bypass capacitors placed close to the MC3PHAC.
8. Consult crystal/resonator manufacturer for component values.

Figure 8. Standalone MC3PHAC Configuration

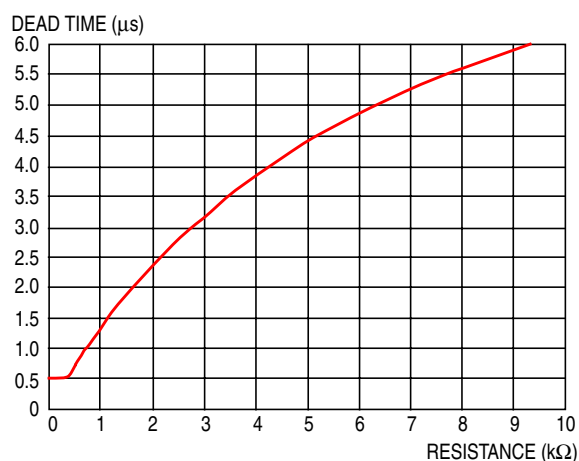


Figure 9. Dead Time as a Function of the RDEADTIME Resistor

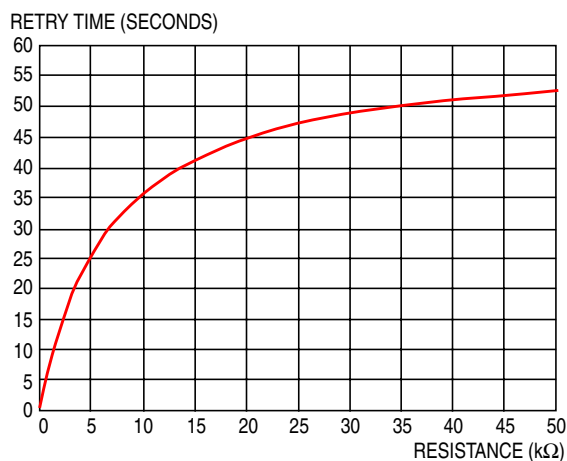


Figure 10. Fault Retry Time as a Function of the RRETRY Resistor



Figure 11. Voltage Boost as a Function of the RBOOST Resistor

Standalone Application Example

Figure 12 shows an application example of the MC3PHAC, configured in standalone mode. Resistor values and jumpers have been selected to provide the following performance:

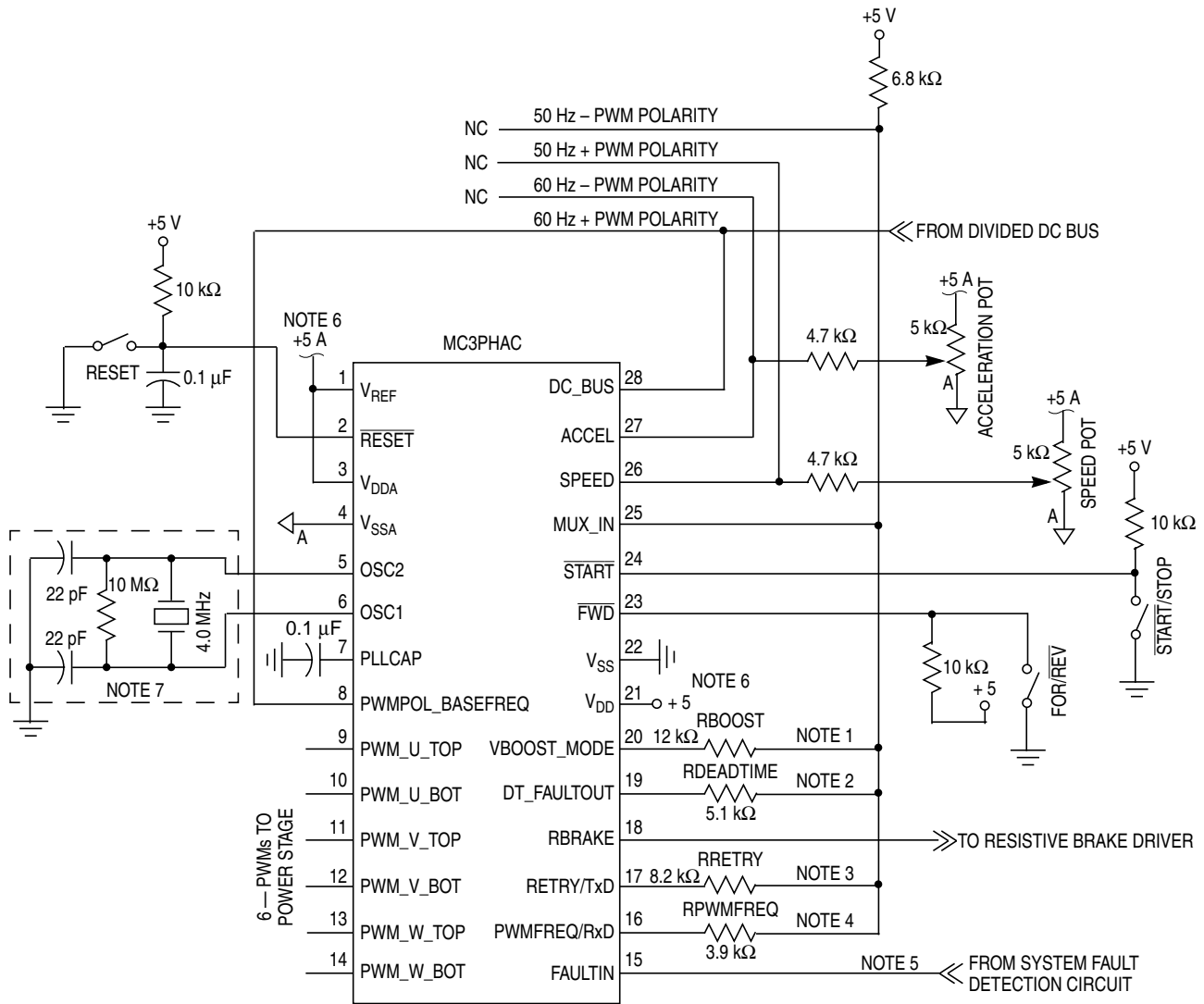
1. Base frequency of 60 Hz and positive PWM polarity (from **Table 3**)
2. PWM frequency resistor 3.9 k Ω , which implies 10.582 kHz from **Table 4**. $(5\text{V}/(3.9\text{k} + 6.8\text{k})) \cdot 3.9\text{k} = 1.82\text{ volts}$
3. Dead-time resistor = 5.1 k Ω , which implies 4.5 μs (from **Figure 9**)
4. Fault retry time resistor = 8.2 k Ω , which implies 32.8 seconds (from **Figure 10**).
5. Voltage boost resistor = 12 k Ω , which implies 25.5 percent (from **Figure 11**).
6. The wiper of the acceleration potentiometer is set at 2.5 V = 64 Hz/second acceleration rate (from the **Acceleration Control** description on **page 78**.) The potentiometer, in this case, could have been a resistor divider. If a resistor divider is used in place of the acceleration potentiometer, keep the total resistance of the two resistors less than 10 k Ω . Always use 4.7k Ω in series with the center of the acceleration voltage divider resistors, connected to the ACCEL (pin 27) as shown in the application example, **Figure 12**.
7. Crystal/resonator capacitor values are typical values from the manufacturer. Refer to the manufacturers data for actual values.

PC Master Software Operation

Introduction to PC Master Host Software

The MC3PHAC is compatible with Motorola's PC master host software serial interface protocol. Communication occurs over an on-chip UART, on the MC3PHAC at 9600 baud to an external master device, which may be a microcontroller that also has an integrated UART or a personal computer via a COM port. With PC master software, an external controller can monitor and control all aspects of the MC3PHAC operation.

When the MC3PHAC is placed in PC master software mode, all control of the system is provided through the integrated UART, resident on the MC3PHAC. Inputs such as START, $\overline{\text{FWD}}$, SPEED, ACCEL, MUX_IN, and PWMPOL_BASEFREQ have no controlling influence over operation of the system. Even though the SPEED, START, and $\overline{\text{FWD}}$ inputs are disabled while the system is in PC master software mode, through PC master software, it is possible to monitor the state of those inputs.

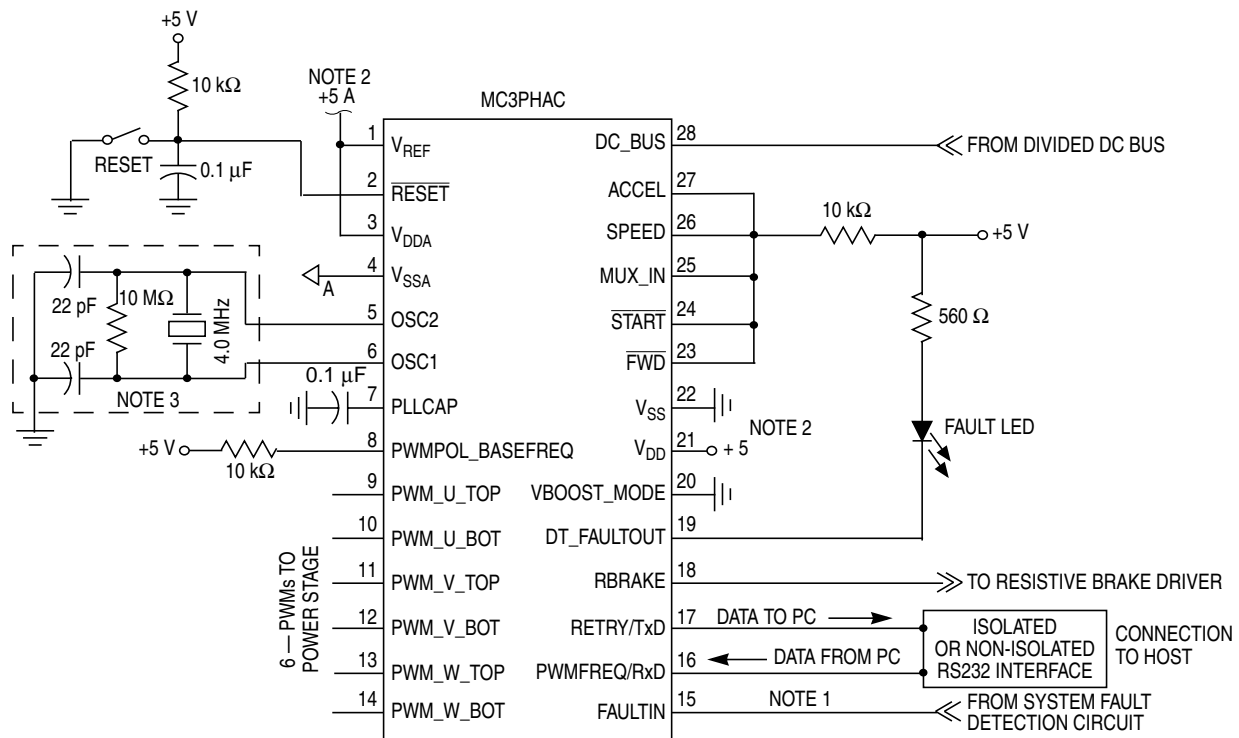


Notes:

1. See [Figure 11](#).
2. See [Figure 9](#).
3. See [Figure 10](#).
4. See [Table 4](#).
5. If no external fault circuit is provided, connect to VSS.
6. Use bypass capacitors placed close to the MC3PHAC.
7. Consult crystal/resonator manufacturer for component values.

Figure 12. MC3PHAC Application Example in Standalone Mode

The most popular master implementation is a PC, where a graphical user interface (GUI) has been layered on top of the PC master software command protocol, complete with a graphical data display, and an ActiveX interface. **Figure 13** shows the MC3PHAC configured in PC master software mode. It is beyond the scope of this document to describe the PC master software protocol or its implementation on a personal computer. For further information on these topics, refer to other Motorola documents relating to the PC master software protocol and availability of PC master host software.



Notes:

1. If no external fault circuit is provided, connect to V_{SS} .
2. Use bypass capacitors placed close to the MC3PHAC.
3. Consult crystal/resonator manufacturer for component values.

Figure 13. MC3PHAC Configuration for Using a PC as a Master

PC Master Software Operation with the MC3PHAC

When power is first applied to the MC3PHAC, or if a logic low level is applied to the $\overline{\text{RESET}}$ pin, the MC3PHAC enters PC master software mode if the VBOOST_MODE pin is low during the initialization phase. The MC3PHAC recognizes a subset of the PC master software command set, which is listed in [Table 5](#).

Table 5. Recognized PC Host Software Commands

| Command | Description |
|--------------|--|
| GETINFOBRIEF | MC3PHAC responds with brief summary of hardware setup and link configuration information |
| READVAR8 | MC3PHAC reads an 8-bit variable at a specified address and responds with its value |
| READVAR16 | MC3PHAC reads a 16-bit variable at a specified address and responds with its value |
| READVAR32 | MC3PHAC reads a 32-bit variable at a specified address and responds with its value |
| WRITEVAR8 | MC3PHAC writes an 8-bit variable at a specified address |
| WRITEVAR16 | MC3PHAC writes a 16-bit variable at a specified address |

With the READVARx commands, the addresses are checked for validity, and the command is executed only if the address is within proper limits. In general, a read command with an address value below \$0060 or above \$EE03 will not execute properly, but instead will return an invalid operation response. An exception to this rule is that PC master software allows reading locations \$0001, \$0036 and \$FE01, which are PORTB data register, Dead Time register and SIM Reset Status registers respectively. The addresses for the WRITEVARx commands are checked for validity, and the data field is also limited to a valid range for each variable. See [Table 6](#) for a list of valid data values and valid write addresses.

User interface variables and their associated PC master software addresses within the MC3PHAC are listed in [Table 6](#).

Table 6. User Interface Variables for Use with PC Master Software

| Name | Address | Read/Write | Size (Bytes) | Description | Valid Data |
|---|---------|------------|--------------|---|---|
| Commanded direction | \$1000 | W | 1 | Determines whether the motor should go forward, reverse, or stop | Forward — \$10 Reverse — \$11 Stop — \$20 |
| Command reset | \$1000 | W | 1 | Forces the MC3PHAC to perform an immediate reset | \$30 |
| Commanded PWM frequency ⁽¹⁾ | \$1000 | W | 1 | Specifies the frequency of the MC3PHAC PWM frequency | 5.3 kHz — \$41 10.6 kHz — \$42 15.9 kHz — \$44 21.1 kHz — \$48 |
| Measured PWM period | \$00A8 | R | 2 | The modulus value supplied to the PWM generator used by the MC3PHAC — value is multiplied by 250 ns to obtain PWM period | \$00BD–\$05E8 |
| Commanded PWM polarity ^{(2), (3), (4)} | \$1000 | W | 1 | Specifies the polarity of the MC3PHAC PWM outputs. This is a write once parameter after reset. Example: \$50 = Bottom and top PWM outputs are positive polarity. | B + T + \$50 B + T – \$54 B – T + \$58 B – T – \$5C |
| Dead time ^{(2), (3), (4)} | \$0036 | R/W | 1 | Specifies the dead time used by the PWM generator. Dead time = Value * 125 ns. This is a write-once parameter. | \$00–\$FF |
| Base frequency ⁽³⁾ | \$1000 | W | 1 | Specifies the motor frequency at which full voltage is applied | 60 Hz — \$60 50 Hz — \$61 |
| Acceleration ⁽³⁾ | \$0060 | R/W | 2 | Acceleration in Hz/sec (7.9 format) ⁽⁸⁾ | \$0000–\$7FFF |
| Commanded motor frequency ⁽³⁾ | \$0062 | R/W | 2 | Commanded frequency in Hz. (8.8 format) ⁽⁹⁾ | \$0000–\$7FFF |
| Actual frequency | \$0085 | R | 2 | Actual frequency in Hz. (8.8 format) ⁽⁹⁾ | \$0000–\$7FFF |
| Status ⁽⁷⁾ | \$00C8 | R | 1 | Status byte | \$00–\$FF |
| Voltage boost | \$006C | R/W | 1 | 0 Hz voltage. %Voltage boost = Value/\$FF | \$00–\$FF |
| Modulation index | \$0091 | R | 1 | Voltage level (motor waveform amplitude percent assuming no bus ripple compensation) Modulation index = value/\$FF | \$00–\$FF |
| Maximum voltage | \$0075 | R/W | 1 | Maximum allowable modulation index value %Maximum voltage = value/\$FF | \$00–\$FF |
| V _{Bus} voltage ^{(5), (10)} | \$0079 | R | 2 | DC bus voltage reading | \$000–\$3FF |

Table 6. User Interface Variables for Use with PC Master Software (Continued)

| Name | Address | Read/ Write | Size (Bytes) | Description | Valid Data |
|---|---------|----------------|-----------------|---|---------------|
| Fault timeout | \$006A | R/W | 2 | Specifies the delay time after a fault condition before re-enabling the motor. Fault timeout = value * 0.262 sec | \$0000–\$FFFF |
| Fault timer | \$006D | R | 2 | Real-time display of the fault timer Elapsed fault time = value * 0.262 sec | \$0000–\$FFFF |
| V _{BUS} decel value ⁽¹⁰⁾ | \$00C9 | R/W | 2 | V _{BUS} readings above this value result in reduced deceleration. | \$0000–\$03FF |
| V _{BUS} RBRAKE value ⁽¹⁰⁾ | \$0064 | R/W | 2 | V _{BUS} readings above this value result in the RBRAKE pin being asserted. | \$0000–\$03FF |
| V _{BUS} brownout value ⁽¹⁰⁾ | \$0066 | R/W | 2 | V _{BUS} readings below this value result in an under voltage fault. | \$0000–\$03FF |
| V _{BUS} over voltage value ⁽¹⁰⁾ | \$0068 | R/W | 2 | V _{BUS} readings above this value result in an over voltage fault. | \$0000–\$03FF |
| Speed in ADC value ⁽⁵⁾ | \$0095 | R | 2 | Left justified 10-bit ADC reading of the SPEED input pin. | \$0000–\$FFC0 |
| Setup ⁽⁷⁾ | \$00AE | R | 1 | Bit field indicating which setup parameters have been initialized before motion is permitted | \$E0–\$FF |
| Switch in ⁽⁷⁾ | \$0001 | R | 1 | Bit field indicating the current state of the start/stop and forward/reverse switches | \$00–\$FF |
| Reset status ^{(6), (7)} | \$FE01 | R | 1 | Indicates cause of the last reset | \$00–\$FF |
| Version | \$EE00 | R | 4 | MC3PHAC version | ASCII field |

1. The commanded PWM frequency cannot be written until the PWM outputs exit the high-impedance state. The default PWM frequency is 15.873 kHz.
2. The PWM output pins remain in a high-impedance state until this parameter is specified.
3. This parameter must be specified before motor motion can be initiated by the MC3PHAC.
4. This is a write-once parameter. The first write to this address will execute normally. Further attempts at writing this parameter will result in an illegal operation response from the MC3PHAC.
5. The value of this parameter is not valid until the PWM outputs exit the high-impedance state.
6. The data in this field is only valid for one read. Further reads will return a value of \$00.
7. See register bit descriptions following this table.
8. Acceleration is an unsigned value with the upper seven bits range of \$00 to \$7F = acceleration value of 0 to 127 Hertz/second. The lower nine bits constitute the fractional portion of the acceleration parameter. Its range is \$000 to \$1FF which equals 0 to ~1. Therefore, the range of acceleration is 0 to 127.99 Hertz/second.
9. Commanded motor frequency and actual frequency are signed values with the upper byte range of \$00 to \$7F = frequency of 0 to 127 Hz. The lower byte is the fractional portion of the frequency. Its range is \$00 to \$FF which equals 0 to ~1.
10. V_{BUS} is the voltage value applied to the DC_BUS analog input pin. The analog-to-digital converter is a 10-bit converter with a 5 volt full scale input. The value is equal to the voltage applied to the DC_BUS input pin/V_{REF} * \$03FF.

Each bit variable listed in [Table 6](#) is defined in [Figure 14](#), [Figure 15](#), [Figure 16](#), and [Figure 17](#).

Address: \$00C8

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------|-------|----------------|----------------|-----------------|-----------------|---------------------|-------------------|--------------------|
| Read: | | SPEED CHANGING | FORWARD MOTION | MOTOR ENERGIZED | RESISTIVE BRAKE | EXTERNAL FAULT TRIP | OVER-VOLTAGE TRIP | UNDER VOLTAGE TRIP |
| Write: | | | | | | | | |
| Reset: | U | 0 | 1 | 0 | 0 | U | 0 | 0 |


 = Unimplemented
 U = Unaffected

Figure 14. Status Register

SPEED CHANGING Bit

This read-only bit indicates if the motor is at a steady speed or if it is accelerating or decelerating.

- 1 = Motor is accelerating or decelerating.
- 0 = Motor is at a steady speed.

FORWARD MOTION Bit

This read-only bit indicates the direction of the motor. It also indicates if the motor is stopped.

- 1 = Motor is rotating in the forward direction. If this bit is a logic 1 and the actual frequency (location \$0085 and \$0086) is 0, the motor is stopped.
- 0 = Motor is rotating in the reverse direction.

MOTOR ENERGIZED Bit

This read-only bit indicates PWM output activity

- 1 = All PWM outputs are active.
- 0 = The PWM outputs are inactive or the bottom PWM outputs are in the pre-charge cycle.

RESISTIVE BREAK Bit

This read-only bit indicates the state of the RBRAKE output pin

- 1 = The RBRAKE output pin is active. Braking is in progress.
- 0 = The RBRAKE output pin is inactive and no braking is in progress.

EXTERNAL FAULT TRIP Bit

This read-only bit indicates a FAULT has occurred resulting from a logic 1 applied to the FAULTIN pin.

1 = A logic 1 was applied to the FAULTIN pin and a FAULT timeout is still in progress.

0 = A logic 0 is applied to the FAULTIN pin and no FAULT timeout is in progress.

OVER-VOLTAGE TRIP Bit

This read-only bit indicates if the voltage at the DC_BUS pin exceeds the preset value of V_{BUS} over voltage located at address \$0068 and \$0069.

1 = The voltage applied to the DC_BUS pin has exceeded the preset value of V_{BUS} over voltage and a FAULT timeout is still in progress.

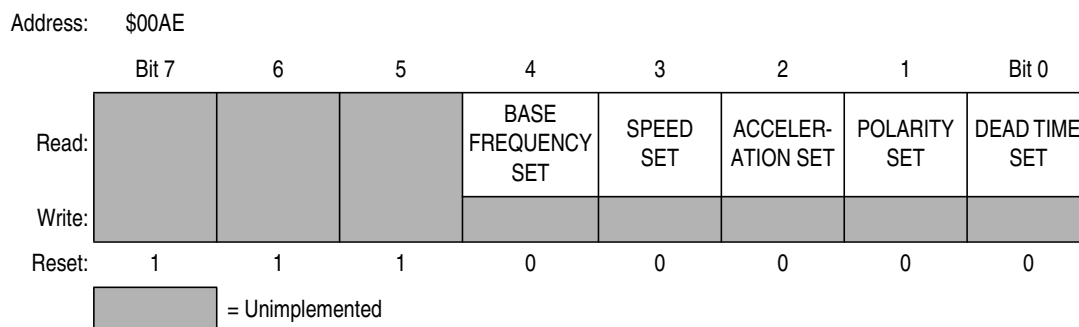
0 = The voltage applied to the DC_BUS pin is less than the preset value of V_{BUS} over voltage and a FAULT timeout is not in progress.

UNDER-VOLTAGE Bit

This read-only bit indicates if the voltage at the DC_BUS pin is less than the present value of V_{BUS} brownout located at address \$0066 and \$0067.

1 = The voltage applied to the DC_BUS pin is less than the present value of V_{BUS} under voltage and a FAULT timeout is still in progress.

0 = The voltage applied to the DC-BUS pin is greater than the preset value of V_{BUS} under voltage and a FAULT timeout is not in progress.

**Figure 15. Setup Register****BASE FREQUENCY SET Bit**

This read-only bit indicates if the base frequency parameter has been set.

1 = Base frequency parameter has been set.

0 = Base frequency parameter has not been set.

SPEED SET Bit

This read-only bit indicates if the speed parameter has been set.

1 = Speed parameter has been set.

0 = Speed parameter has not been set.

ACCELERATION SET Bit

This read-only bit indicates if the acceleration rate parameter has been set.

1 = Acceleration rate parameter has been set.

0 = Acceleration rate parameter has not been set.

POLARITY SET Bit

This read-only bit indicates if the PWM polarity parameters has been set.

1 = PWM polarity parameters has been set.

0 = PWM polarity parameters has not been set.

DEAD TIME SET Bit

This read-only bit indicates if the dead time parameter has been set.

1 = Dead time parameter has been set.

0 = Dead time parameter has not been set.

Address: \$0001

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------|-------|----------------|-----------------|---|--------------|-------------------|---|-------|
| Read: | | START/ STOP | FWD/ REVERSE | | FAULT OUT | RESISTOR BRAKE | | |
| Write: | | | | | | | | |
| Reset: | U | U | U | U | U | 0 | U | U |


 = Unimplemented
 U = Unaffected

Figure 16. Switch In Register

START/STOP Bit

This read-only bit indicates the state of the $\overline{\text{START}}$ input pin.

1 = The $\overline{\text{START}}$ input pin is at a logic 1.

0 = The $\overline{\text{START}}$ input pin is at a logic 0.

FWD/REVERSE Bit

This read-only bit indicates the state of the $\overline{\text{FWD}}$ input pin.

1 = The $\overline{\text{FWD}}$ input pin is at a logic 1

0 = The $\overline{\text{FWD}}$ input pin is at a logic 0

FAULT OUT Bit

This read-only bit indicates the state of the DT_FAULTOUT output pin.

1 = The DT_FAULTOUT output pin is indicating no fault condition.

0 = The DT_FAULTOUT output pin is indicating a fault condition.

RESISTIVE BRAKE Bit

This read-only bit indicates the state of resistive brake pin (RBRAKE).

1 = The RBRAKE output pin is active. Braking is in progress.

0 = The RBRAKE output pin is inactive and no braking is in progress.

| | | | | | | | | |
|----------|----------|-----------|--------------------------|--------------------------|---------------------------------|---|----------------------|-------|
| Address: | \$FE01 | | | | | | | |
| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| Read: | POWER UP | RESET PIN | MC3PHAC FUNCTIONAL FAULT | MC3PHAC FUNCTIONAL FAULT | PCMASTER SOFTWARE RESET COMMAND | | LOW V_{DD} VOLTAGE | |
| Write: | | | | | | | | |
| Reset: | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


 = Unimplemented

Figure 17. Reset Status Register

POWER UP Bit

This read-only bit indicates the last system reset was caused by the power-up reset detection circuit.

- 1 = The last reset was caused by an initial power-up of the MC3PHAC.
- 0 = Power-up reset was not the source of the reset or a read of the reset status register after the first read.

RESET PIN Bit

This read-only bit indicates the last system reset was caused from the $\overline{\text{RESET}}$ input pin.

- 1 = Last reset was caused by an external reset applied to the $\overline{\text{RESET}}$ input pin.
- 0 = The $\overline{\text{RESET}}$ pin was not the source of the reset or a read of the reset status register after the first read.

MC3PHAC FUNCTIONAL FAULT Bits

This read-only bit indicates if the last system reset was the result of an internal system error.

- 1 = MC3PHAC internal system error
- 0 = The FUNCTIONAL FAULT was not the source of the reset or a read of the reset status register after the first read.

PC MASTER SOFTWARE RESET COMMAND Bit

This read-only bit indicates the last system reset was the result of a PC master software reset command.

- 1 = The MC3PHAC was reset by the PC master software command reset as the result of a write of \$30 to location \$1000
- 0 = The PC master software RESET COMMAND was not the source of the reset or a read of the reset status register after the first read.

LOW V_{DD} VOLTAGE Bit

This read-only bit indicates if the last reset was the result of low V_{DD} applied to the MC3PHAC.

- 1 = The last reset was caused by the low power supply detection circuit.
- 0 = The LOW V_{DD} was not the source of the reset or a read of the reset status register after the first read.

Command State Machine

When using the PC master software mode of operation, the command state machine governs behavior of the device depending upon its current state, system parameters, any new commands received via the communications link, and the prevailing conditions of the system. The command state diagram is in [Figure 18](#). It illustrates the sequence of commands which are necessary to bring the device from the reset condition to running the motor in a steady state and depicts the permissible state transitions. The device will remain within a given state unless the conditions shown for a transition are met.

Some commands only cause a temporary state change to occur. While they are being executed, the state machine will automatically return to the state which existed prior to the command being received. For example, the motor speed may be changed from within any state by using the WRITEVAR16 command to write to the "Speed In" variable. This will cause the "Set Speed" state to be momentarily entered, the "Speed In" variable will be updated and then the original state will be re-entered. This allows the motor speed, acceleration or base frequency to be modified whether the motor is already accelerating, decelerating, or in a steady state.

Each state is described here in more detail.

- **Reset** — This state is entered when a device power-on reset (POR), pin reset, loss of crystal, internally detected error, or reset command occurs from within any state. In this state, the device is initialized and the PWM outputs are configured to high impedance. This state is then automatically exited.
- **PWMHighZ** — This state is entered from the reset state. This state is also re-entered after one and only one of the PWM dead-time or polarity parameters have been initialized. In this state the PWM outputs are configured to a high-impedance state as the device waits for both the PWM dead time and polarity to be initialized.
- **SetDeadTime** (write once) — This state is entered from the PWMHighZ state the first time that a write to the PWM dead-time variable occurs. In this state, the PWM dead time is initialized and the state is then automatically exited. This state cannot be re-entered, and hence the dead time cannot be modified, unless the reset state is first re-entered.
- **SetPolarity** (write once) — This state is entered from the PWMHighZ state the first time that the PWM polarity command is received. In this state, the PWM polarity is initialized and the state is then automatically exited. This state cannot be re-entered, and hence the polarity cannot be modified, unless the reset state is first re-entered.

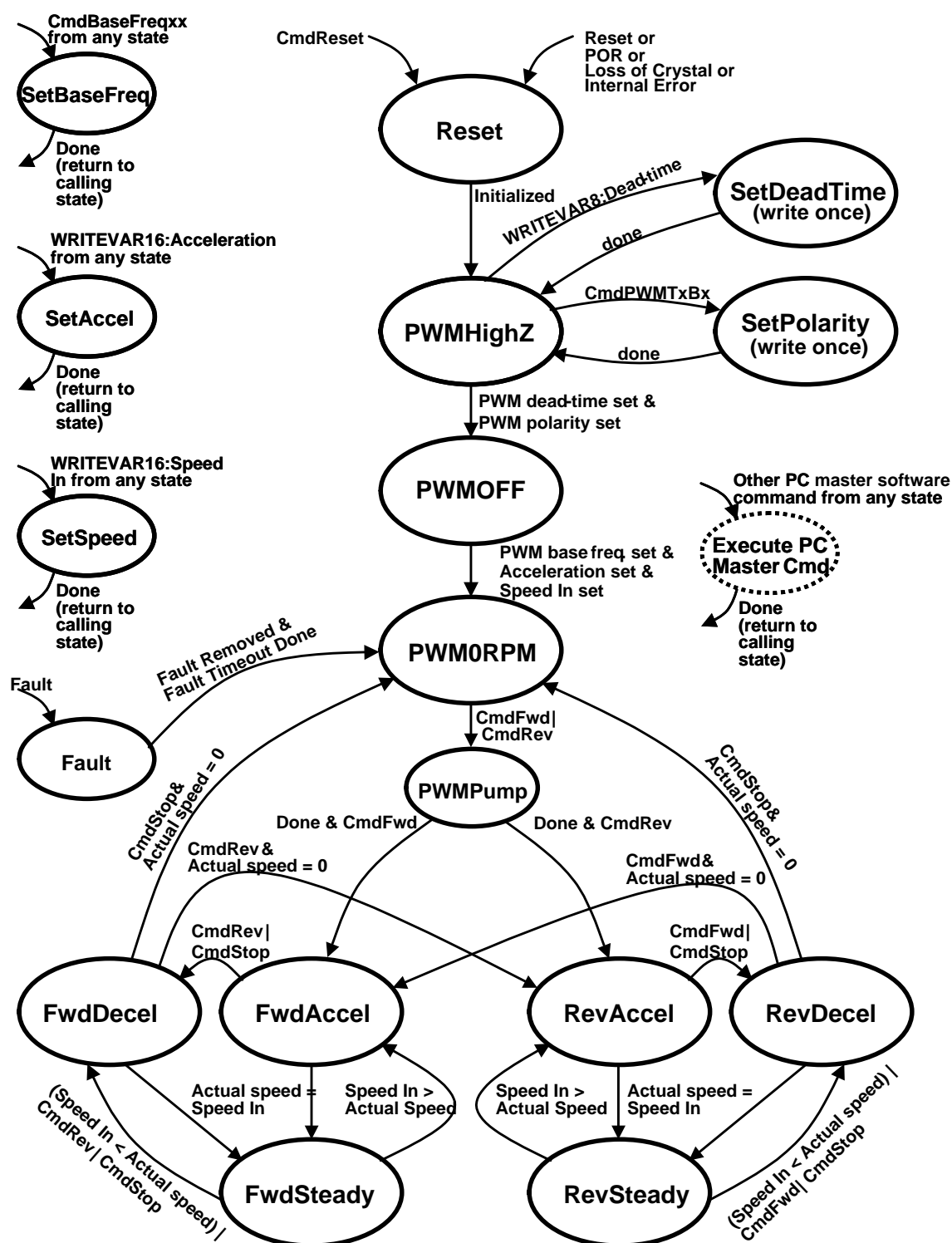


Figure 18. PC Host Software Command State Diagram

- **PWMOFF** — This state is entered from the PWMHighZ state if both the PWM dead time *and* polarity have been configured. In this state, the PWM is activated and all the PWM outputs are driven off for the chosen polarity. The device then waits for the PWM base frequency, motor speed, and acceleration to be initialized.
- **PWM0RPM** — This state is entered from the PWMOFF state when the PWM base frequency, motor speed, and acceleration have been initialized. This state can also be entered from the FwdDecel or RevDecel states if a CmdStop command has been received, and the actual motor speed has decelerated to 0 r.p.m. In this state, the PWM pins are driven to the off state for the chosen polarity. The only exit of this state is to the PWMPump state, which occurs when a CmdFwd or CmdRev command is received.
- **PWMPump** — This state is entered from the PWM0RPM state when a CmdFwd or CmdRev command is received. In this state the top PWM outputs are driven off while the bottom PWM outputs are driven with a 50 percent duty cycle. This allows high side transistor gate drive circuits which require charge pumping from the lower transistors to be charged up prior to applying full PWMs to energize the motor. This state is automatically exited after the defined amount of time t_{Pump} (see [Electrical Characteristics](#)).
- **FwdAccel** — This state is entered from the PWMPump state after a CmdFwd command is received and the timeout interval from the PWMPump state is completed. This state can also be entered from the FwdSteady state if the Speed In variable is increased above the actual current speed and the RevDecel state if the actual motor speed equals 0 r.p.m. when a CmdFwd command has been received. In this state the motor is accelerated forward according to the chosen parameters.
- **FwdSteady** — This state is entered from the FwdAccel state after the actual motor speed has reached the requested speed defined by the Speed In variable. In this state, the motor is held at a constant forward speed.
- **FwdDecel** — This state is entered from the FwdAccel or FwdSteady states whenever a CmdStop or CmdRev command is received. This state can also be entered from the FwdSteady state if the Speed In variable is decreased below the actual current speed. In this state, the motor is decelerated forward according to the chosen parameters.
- **RevAccel** — This state is entered from the PWMPump state. After a CmdRev command is received and the timeout interval from the PWMPump state is completed. This state can also be entered from the RevSteady state if the Speed In variable is increased above the actual current speed and the FwdDecel state if the actual motor speed equals 0 r.p.m. when a CmdRev command has been received. In this state, the motor is accelerated in reverse according to the chosen parameters.

- **RevSteady** — This state is entered from the RevAccel state after the actual motor speed has reached the requested speed defined by the Speed In variable. In this state, the motor is held at a constant reverse speed.
- **RevDecel** — This state is entered from the RevAccel or RevSteady states whenever a CmdStop or CmdFwd command is received. This state can also be entered from the RevSteady state if the Speed In variable is decreased below the actual current speed. In this state, the motor is decelerated in reverse according to the chosen parameters.
- **SetBaseFreq** — This state is entered from any state whenever a CmdBaseFreqxx command is received. In this state, the motor frequency at which full voltage is applied is configured and the state is then automatically exited and the original state is re-entered.
- **SetAccel** — This state is entered from any state whenever a write to the Acceleration variable occurs. In this state, the motor acceleration is configured and the state is then automatically exited and the original state is re-entered.
- **SetSpeed** — This state is entered from any state whenever a write to the Speed In variable occurs. In this state, the requested motor speed is configured and the state is then automatically exited and the original state is re-entered.
- **Fault** — This state is entered from any state whenever a fault condition occurs (see [Fault Protection](#) on [page 80](#)). In this state, the PWM outputs are driven off (unless the fault state was entered from the PWMHighZ state, in which case, the PWM outputs remain in the High Z state). When the problem causing the fault condition is removed, a timer is started which will wait a specified amount of time (which is user programmable) before exiting this state. Under normal operating conditions, this timeout will cause the Fault state to be automatically exited to the PWM0RPM state, where motion will once again be initiated if a CmdFwd or CmdRev has been received. The exceptions to this rule are the cases when the Fault state was entered from the PWMHighZ or PWMOFF states, in which case, exiting from the Fault state will return back to these states.

Optoisolated RS232 Interface Application Example

Some motor control systems have the control electronics operating at the same potential as the high voltage bus. Connecting a PC to that system could present safety issues, due to the high voltage potential between the motor control system and the PC. **Figure 19** is an example of a simple circuit that can be used with the MC3PHAC to isolate the serial port of the PC from the motor control system.

The circuit in **Figure 19** is the schematic of a half-duplex optoisolated RS232 interface. This isolated terminal interface provides a margin of safety between the motor control system and a personal computer. The EIA RS232 specification states the signal levels can range from 3 to 25 volts. A Mark is defined by the EIA RS232 specification as a signal that ranges from -3 to -25 volts. A Space is defined as a signal that ranges from +3 to +25 volts. Therefore, to meet the RS232 specification, signals to and from a terminal must transition through 0 volts as it changes from a Mark to a Space. Breaking the circuit down into an input and output section simplifies the explanation of the circuit.

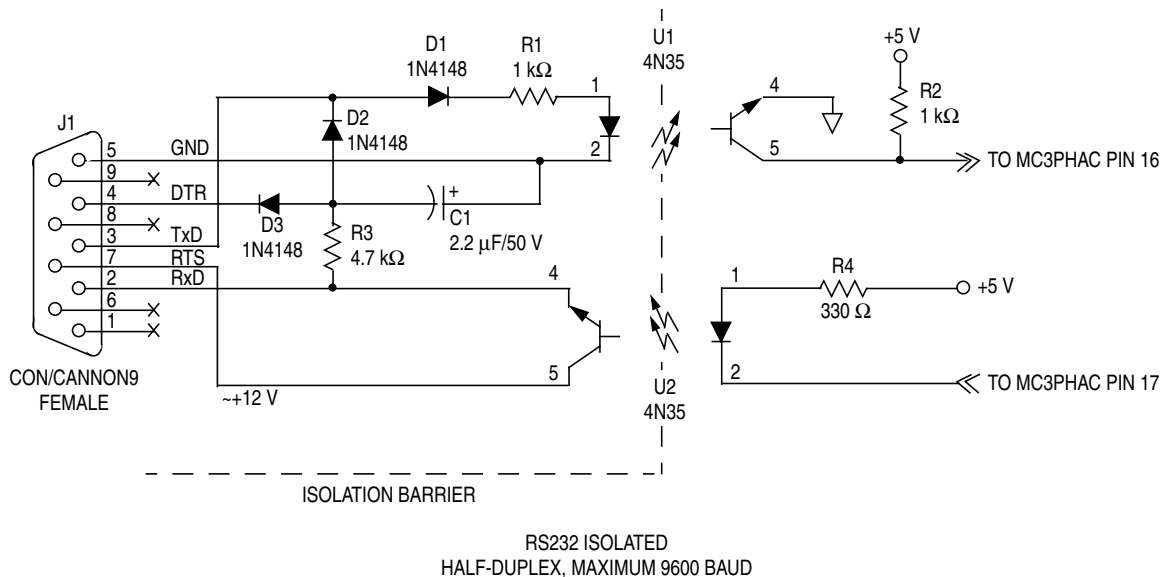


Figure 19. Optoisolated RS232 Circuit

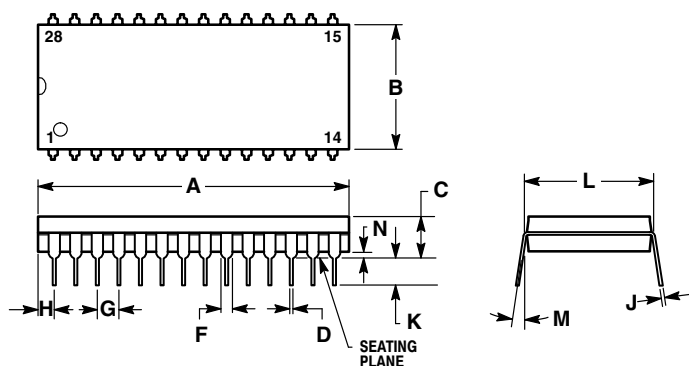
To send data from a PC to the MC3PHAC, it is necessary to satisfy the serial input of the MC3PHAC. In the idle condition, the serial input of the MC3PHAC must be at a logic 1. To accomplish that, the transistor in U1 must be turned off. The idle state of the transmit data line (TxD) from the PC serial port is a Mark (–3 to –25 volts). Therefore, the diode in U1 is off and the transistor in U1 is off, yielding a logic 1 to the MC3PHAC's serial input. When the start bit is sent to the MC3PHAC from the PC's serial port, the PC's TxD transitions from a Mark to a Space (+3 to +25 volts), thus forward biasing the diode in U1. Forward biasing the diode in D1 turns on the transistor in U1, providing a logic 0 to the serial input of the MC3PHAC. Simply stated, the input half of the circuit provides input isolation, signal inversion, and level shifting from the PC to the MC3PHAC's serial port. An RS-232 line receiver, such as an MC1489, serves the same purpose without the optoisolation function.

To send data from the MC3PHAC to the PC's serial port input, it is necessary to satisfy the PC's receive data (RxD) input requirements. In an idle condition, the RxD input to the PC must be at a Mark (–3 to –25 volts). The data terminal ready output (DTR) on the PC outputs a Mark when the port is initialized. The request to send (RTS) output is set to a Space (+3 to +25 volts) when the PC's serial port is initialized. Because the interface is half-duplex, the PC's TxD output is also at a Mark, as it is idle. The idle state of the MC3PHAC's serial port output is a logic 1. The logic 1 out of the MC3PHAC's serial port output port forces the diode in U2 to be turned off. With the diode in U2 turned off, the transistor in U2 is also turned off. The junction of D2 and D3 are at a Mark (–3 to –25 volts). With the transistor in U2 turned off, the input is pulled to a Mark through current limiting resistor R3, satisfying the PC's serial input in an idle condition. When a start bit is sent from the MC3PHAC's serial port, it transitions to a logic 0. That logic 0 turns on the diode in U2, thus turning on the transistor in U2. The conducting transistor in U2 passes the voltage output from the PC's RTS output, that is now at a Space (+3 to +25 volts), to the PC's receive data (RxD) input. Capacitor C1 is a bypass capacitor used to stiffen the Mark signal. The output half of the circuit provides output isolation, signal inversion, and level shifting from the MC3PHAC's serial output port to the PC's serial port. An RS-232 line driver, such as a MC1488, serves the same purpose without the optoisolation function.

Mechanical Data

This subsection provides case outline drawings for:

- Plastic 28-pin DIP, [Figure 20](#)
- Plastic 28-pin SOIC, [Figure 21](#)
- Plastic 32-pin QFP, [Figure 22](#)

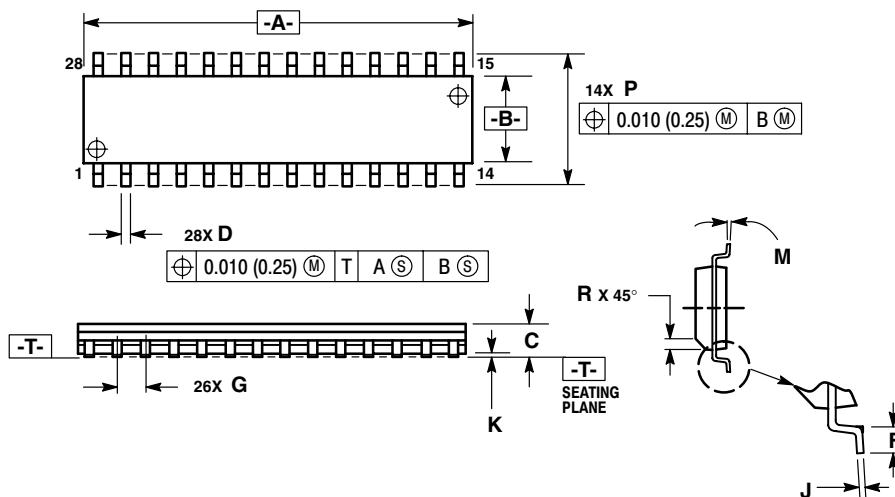


NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 36.45 | 37.21 | 1.435 | 1.465 |
| B | 13.72 | 14.22 | 0.540 | 0.560 |
| C | 3.94 | 5.08 | 0.155 | 0.200 |
| D | 0.36 | 0.56 | 0.014 | 0.022 |
| F | 1.02 | 1.52 | 0.040 | 0.060 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.65 | 2.16 | 0.065 | 0.085 |
| J | 0.20 | 0.38 | 0.008 | 0.015 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 15.24 BSC | | 0.600 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

Figure 20. Plastic 28-Pin DIP (Case 710)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 17.80 | 18.05 | 0.701 | 0.711 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.41 | 0.90 | 0.016 | 0.035 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.23 | 0.32 | 0.009 | 0.013 |
| K | 0.13 | 0.29 | 0.005 | 0.011 |
| M | 0° | 8° | 0° | 8° |
| P | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |

Figure 21. Plastic 28-Pin SOIC (Case 751F)

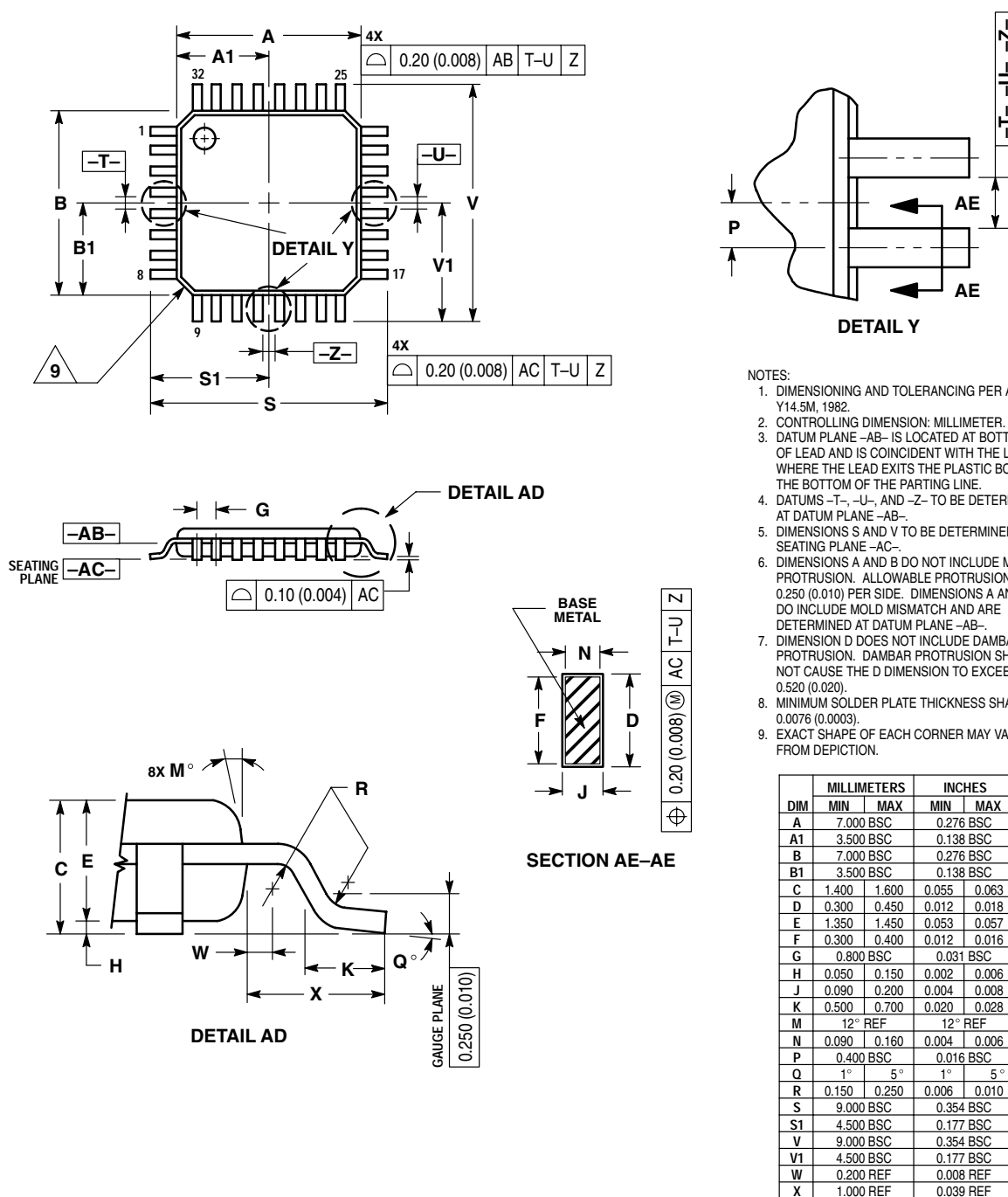


Figure 22. Plastic 32-Pin QFP (Case 873A)

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