EIE2050
Digital Logic and Systems

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Office: Room 404, Research A Building

Latches and Flip-Flops

- Latches
- Flip-flops
- Applications

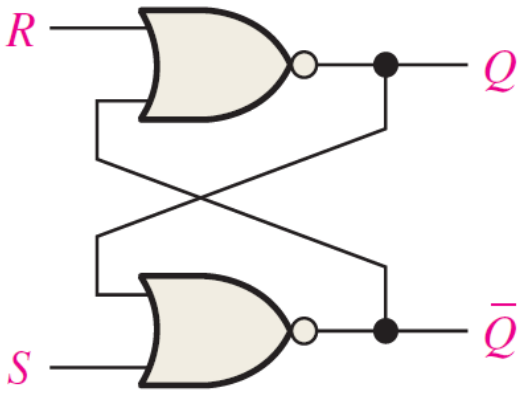
Reading material: Chapter 7 of Textbook:
Textbook: *Digital Fundamentals (global edition, 11th edition)*, by Thomas Floyd, Pearson 2015.
The examples used in the lecture are based on the textbook.

Latches and Flip-Flops

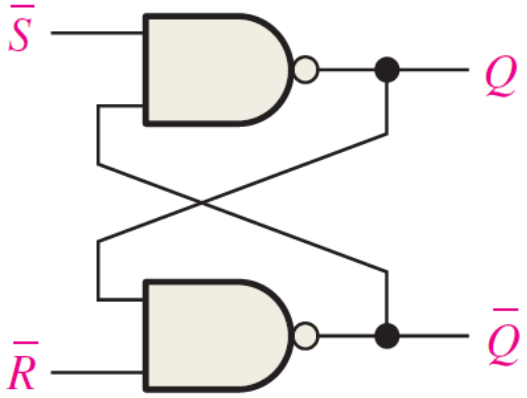
- Latches
    - S-R latch
    - Gated S-R latch
    - Gated D latch

Latches and Flip-Flops

- S-R Latch (set-reset latch): Logic diagram



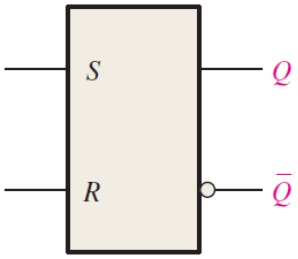
Active-HIGH input S-R latch



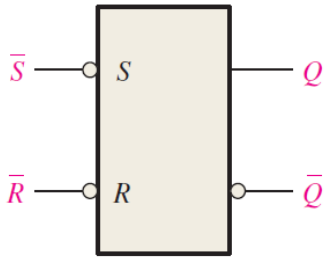
Active-LOW input $\bar{S}$-$\bar{R}$ latch

Latches and Flip-Flops

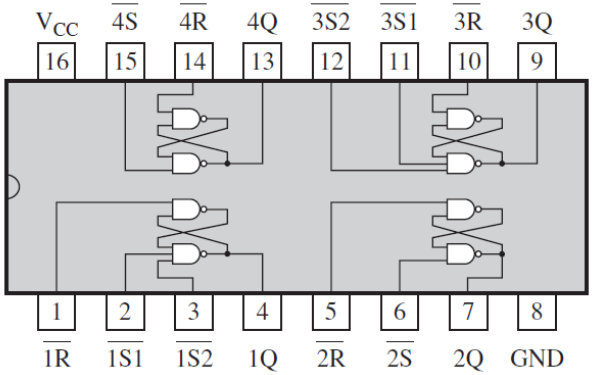
- S-R Latch: Logic symbols



Active-HIGH input
S-R latch



Active-LOW input
$\overline{S}$-$\overline{R}$ latch



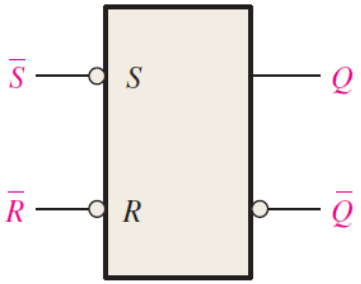
74HC279A, a quad $\overline{S}$-$\overline{R}$ latch

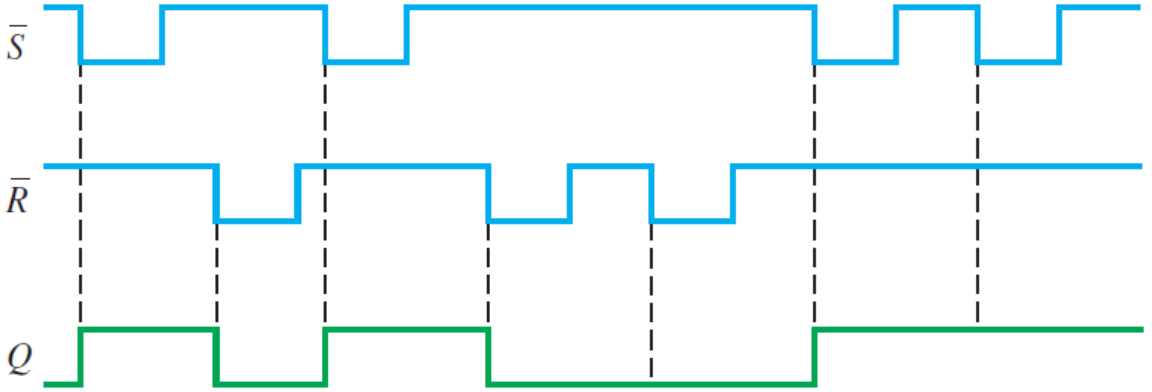
Truth table for an active-LOW input $\overline{S}$-$\overline{R}$ latch.

Inputs		Outputs		
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	Comments
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

Latches and Flip-Flops

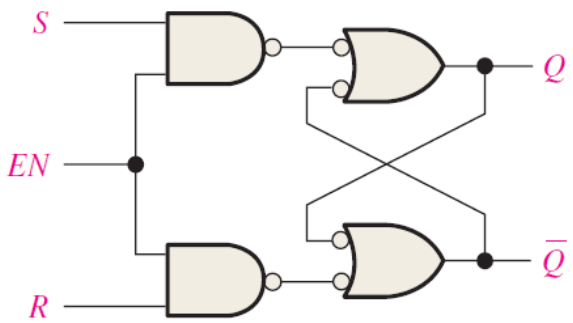
- Active LOW $\overline{S}$-$\overline{R}$ Latch: waveform analysis



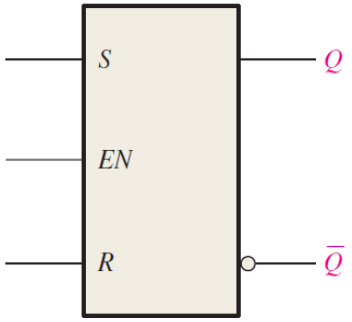


Latches and Flip-Flops

- Gated S-R Latch

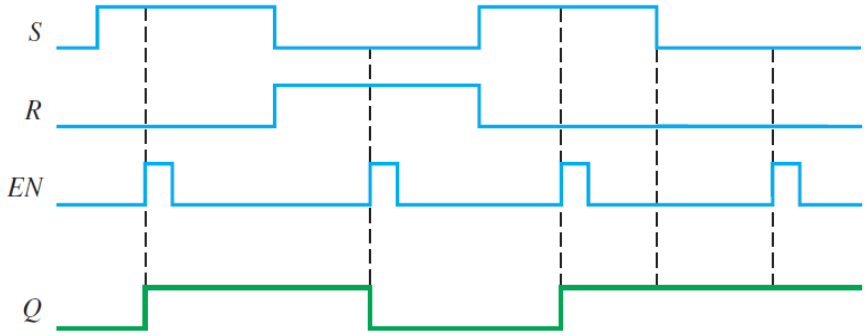


Logic diagram



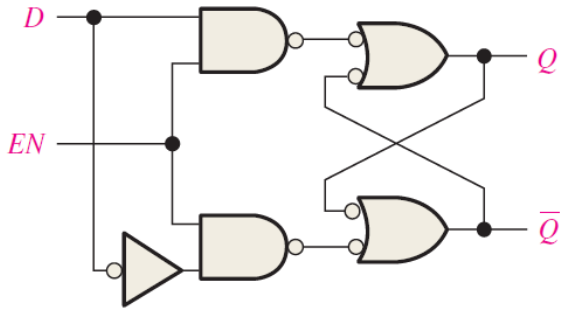
Logic symbol

Waveform analysis

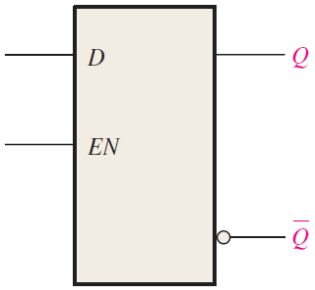


Latches and Flip-Flops

- Gated D Latch

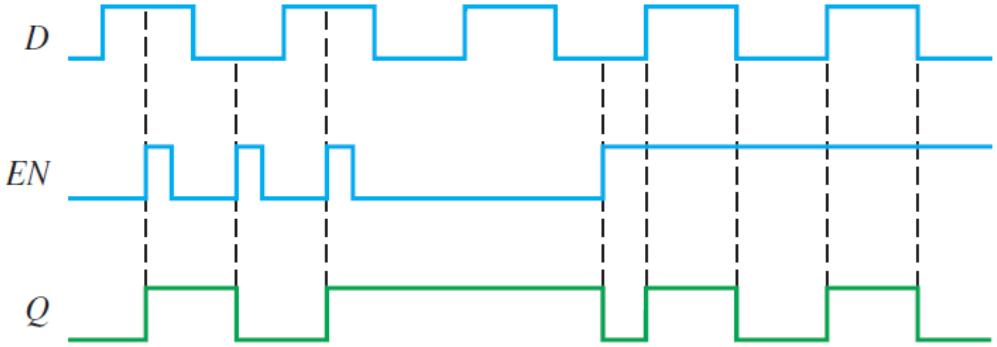


Logic diagram



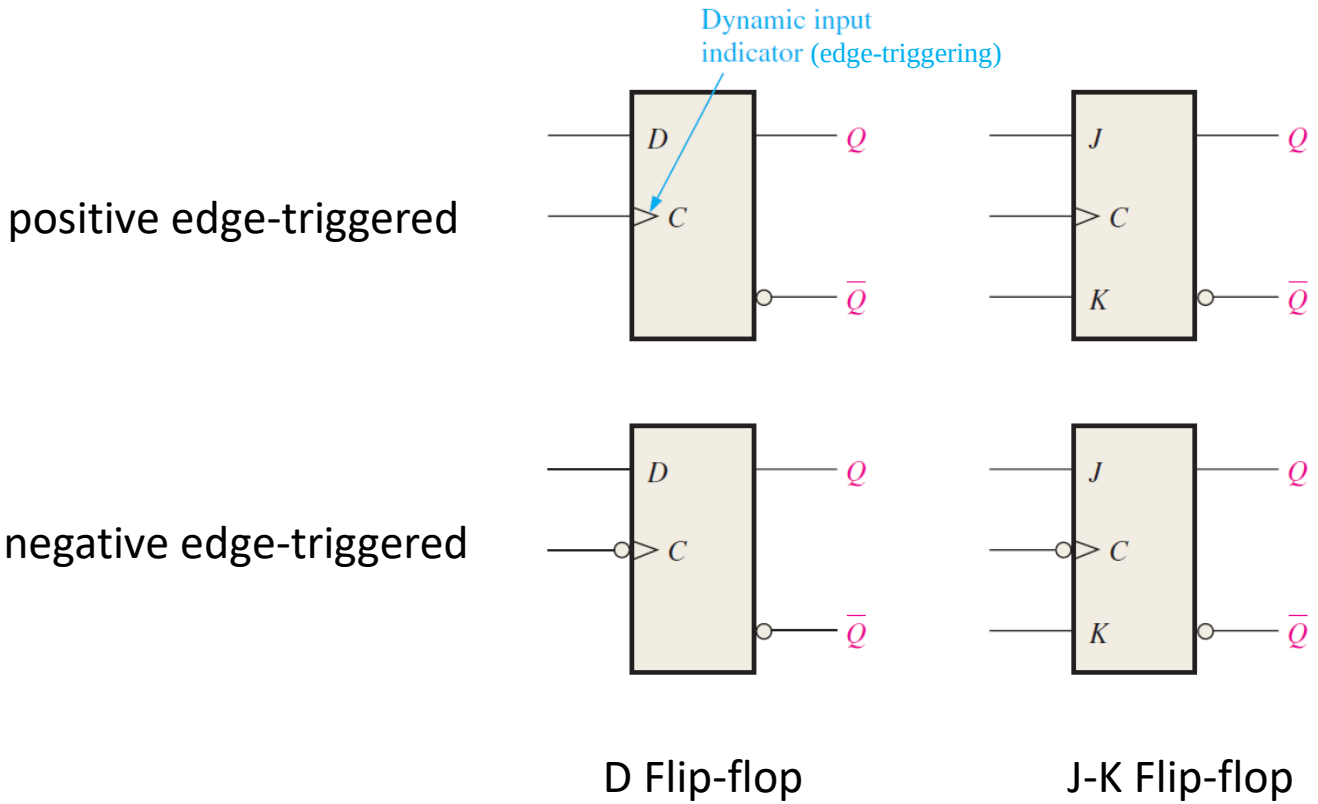
Logic symbol

Waveform analysis



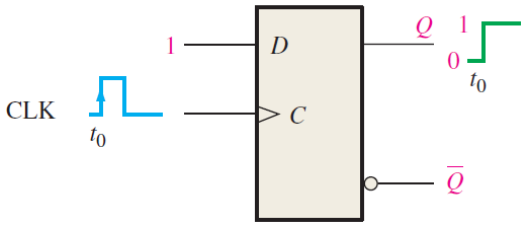
Latches and Flip-Flops

- Edge triggered Flip-Flops
  - D Flip-flop
  - J-K Flip-flop

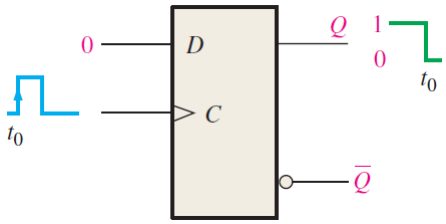


Latches and Flip-Flops

- D Flip-Flops



D=1 (SET)

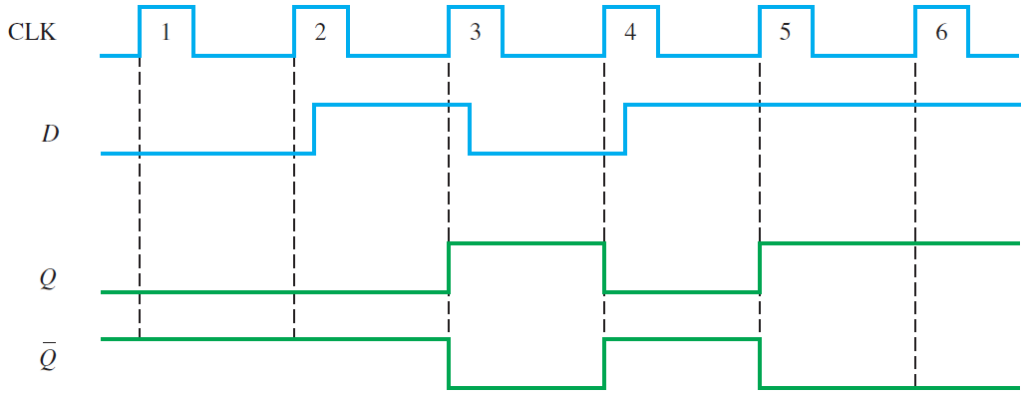


D=0 (RESET)

Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		
D	CLK	*Q*	$\overline{Q}$	Comments
0	↑	0	1	RESET
1	↑	1	0	SET

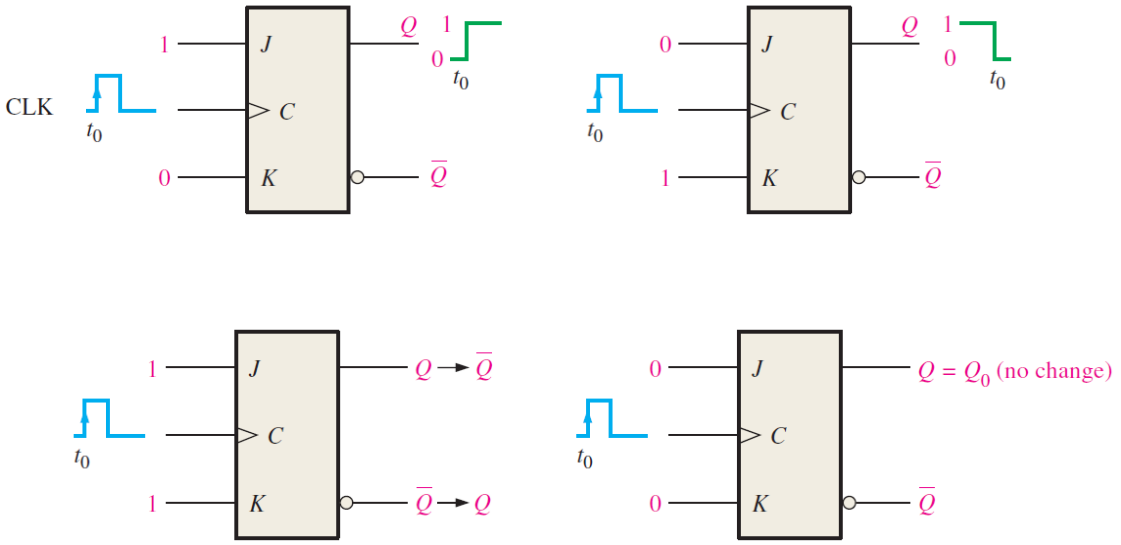
↑ = clock transition LOW to HIGH



Waveform analysis

Latches and Flip-Flops

- J-K Flip-Flops
  (J-K: Jack Kilby)



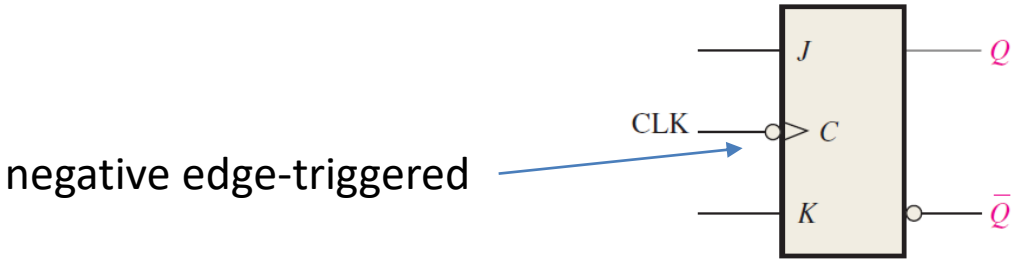
Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		
J	*K*	CLK	*Q*	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

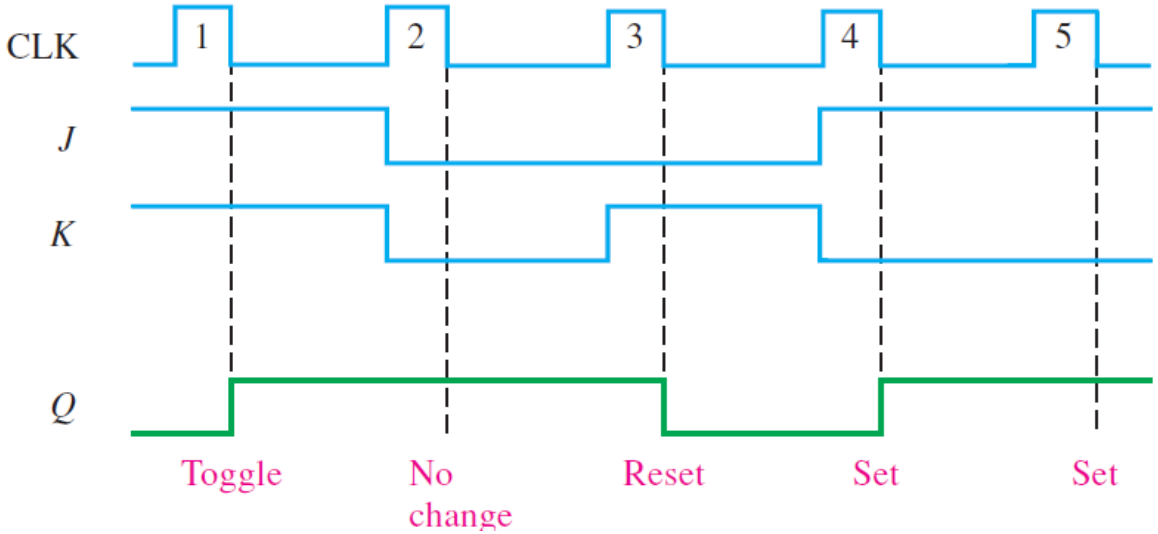
↑ = clock transition LOW to HIGH
Q_0 = output level prior to clock transition

Latches and Flip-Flops

- J-K Flip-Flops

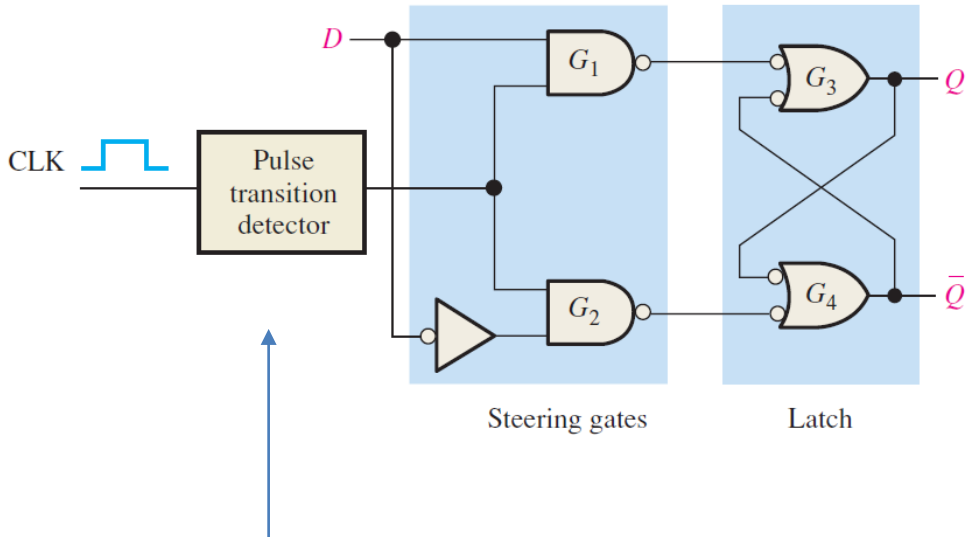


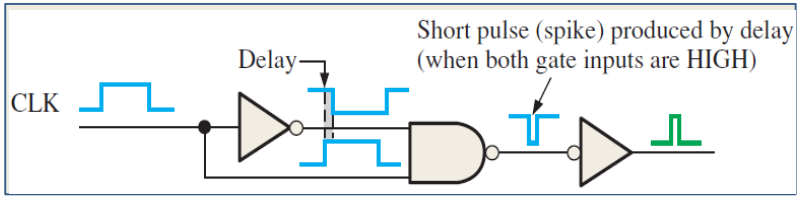
Waveform analysis



Latches and Flip-Flops

- Edge-Triggered Operation: D Flip-Flops



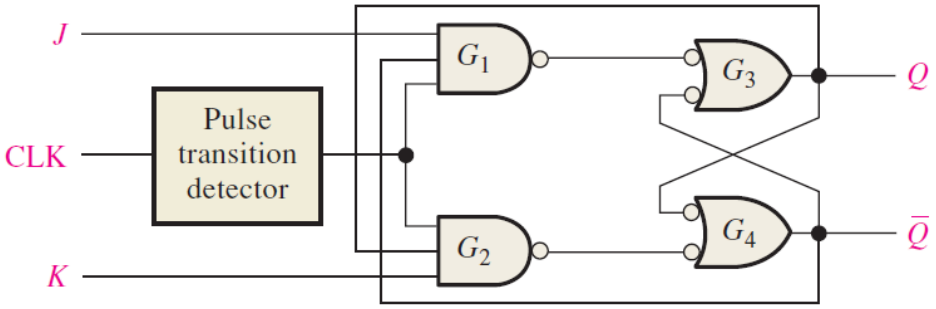


Pulse transition detector

Because the triggering effect by this short pulse (spike), D needs to maintain its intended value only for a short duration.

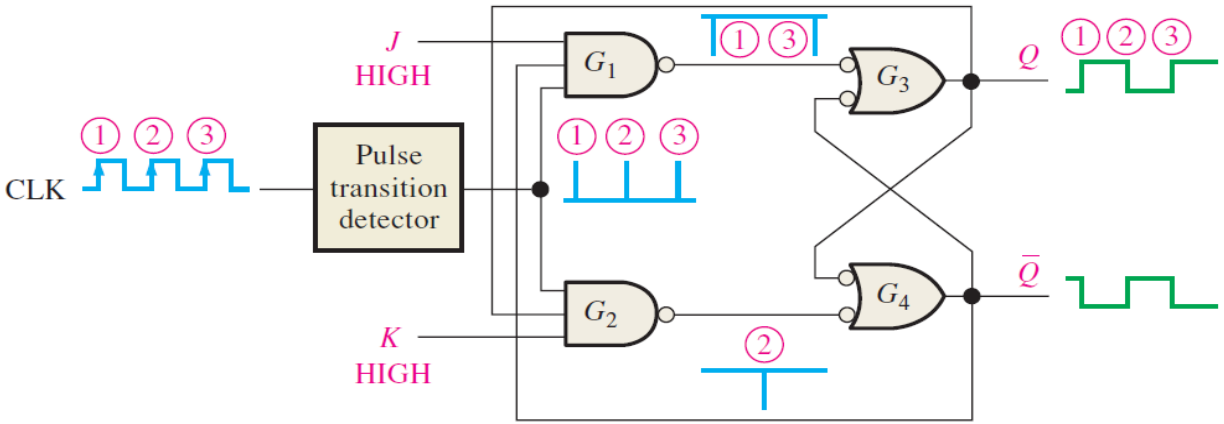
Latches and Flip-Flops

- Edge-Triggered Operation: J-K Flip-Flops



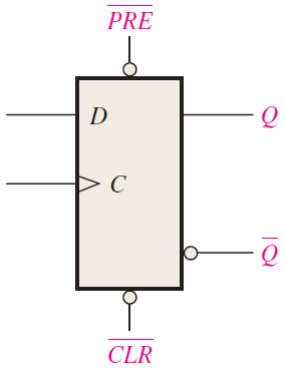
Simplified logic diagram

Operation Example:
J=K=1,
Q and $\bar{Q}$ toggles

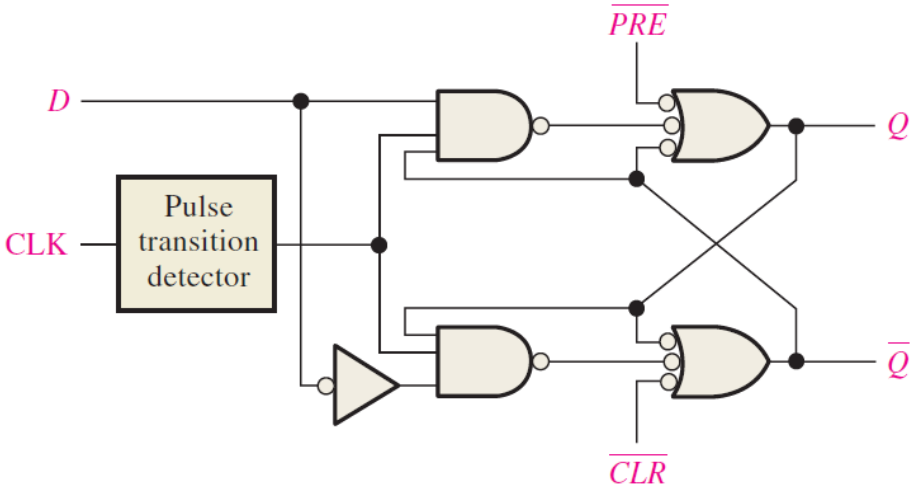


Latches and Flip-Flops

- D Flip-Flop with Active-LOW Preset and Clear Inputs



Logic symbol



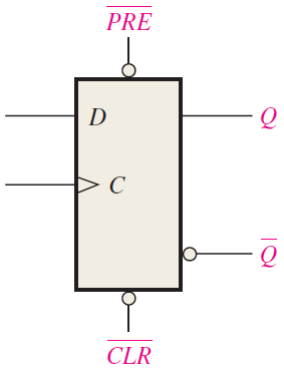
logic diagram

Synchronous inputs: D
Asynchronous inputs: PRE, CLR

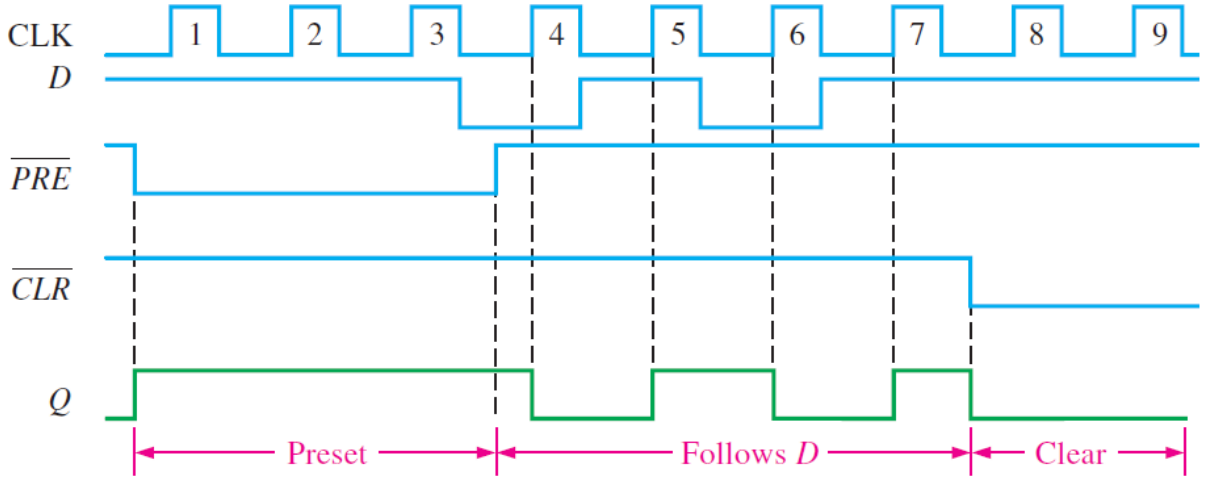
PRE: to set Q=1
CLR: to set Q=0

Latches and Flip-Flops

- D Flip-Flop with Active-LOW Preset and Clear Inputs



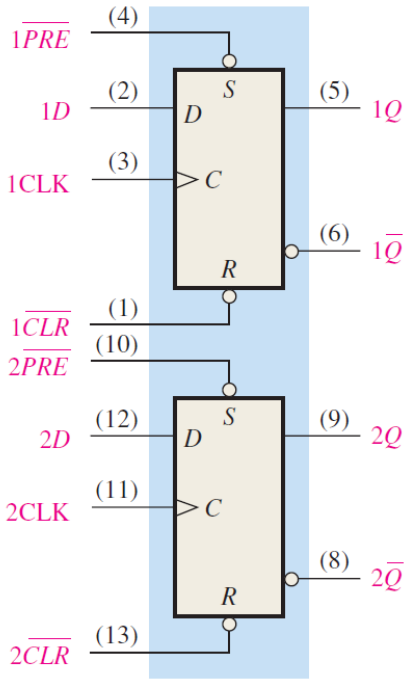
Logic symbol



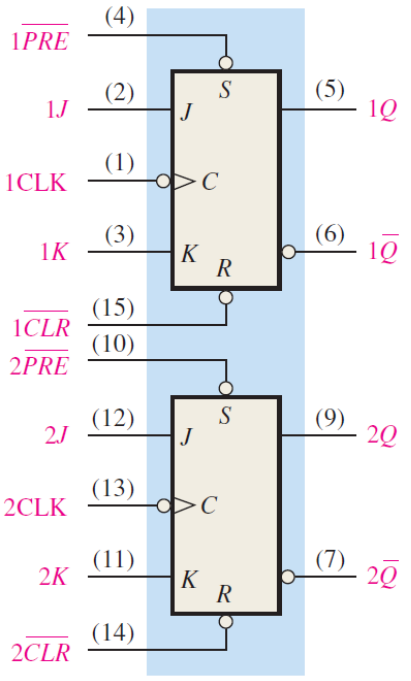
Waveform analysis

Latches and Flip-Flops

- Flip-flops in 74 Series



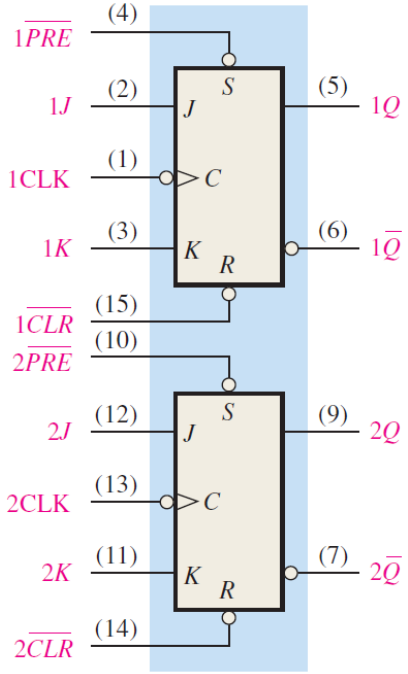
74HC74
Dual
positive edge-triggered
D flip-flops



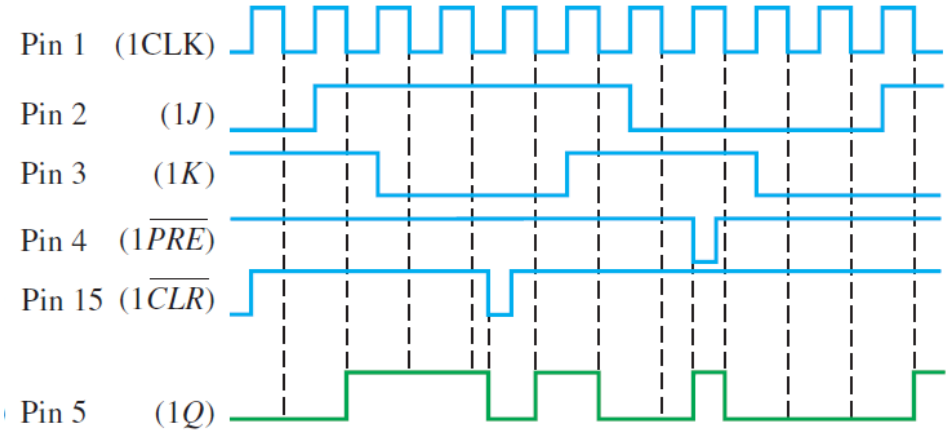
74HC112
Dual
negative edge-triggered
J-K flip-flops

Latches and Flip-Flops

- J-K Flip-flop Example



74HC112
Dual
negative edge-triggered
J-K flip-flops



Waveform analysis

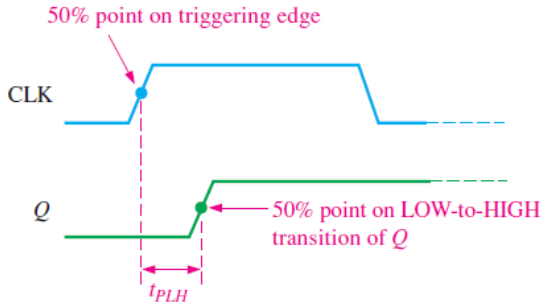
Synchronous inputs: J, K
Asynchronous inputs: PRE, CLR

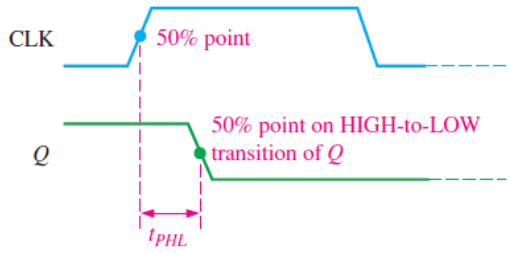
Latches and Flip-Flops

- Flip-Flop Operating Characteristics

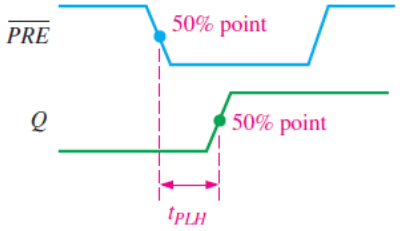
Propagation Delays:

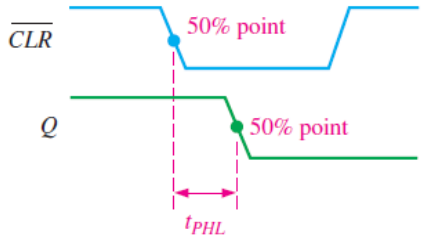
Clock to output



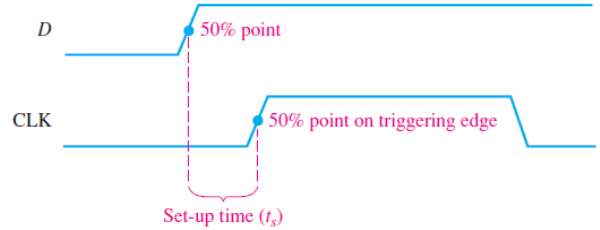


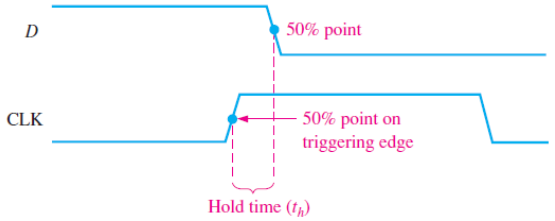
PRE/CLR to output





Setup time, hold time





Latches and Flip-Flops

- Flip-Flop Operating Characteristics: example

Comparison of operating parameters for four IC families of flip-flops of the same type at 25°C.

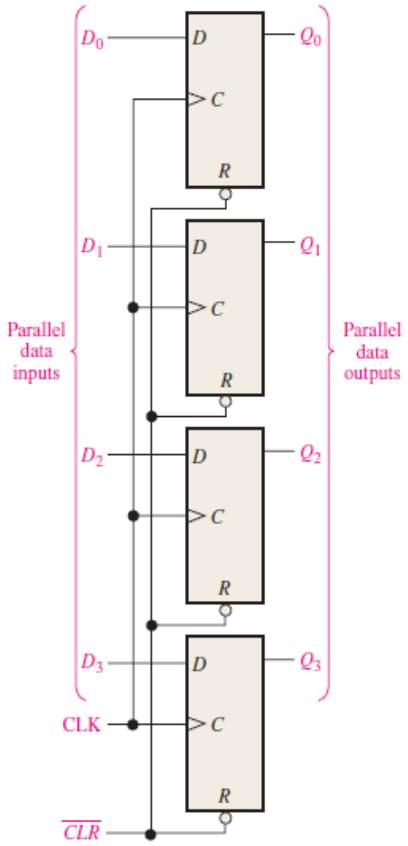
	CMOS		Bipolar (TTL)	
Parameter	**74HC74A**	**74AHC74**	**74LS74A**	**74F74**
t_{PHL} (CLK to Q)	17 ns	4.6 ns	40 ns	6.8 ns
t_{PLH} (CLK to Q)	17 ns	4.6 ns	25 ns	8.0 ns
$t_{PHL}(\overline{CLR}$ to $Q)$	18 ns	4.8 ns	40 ns	9.0 ns
$t_{PLH}(\overline{PRE}$ to $Q)$	18 ns	4.8 ns	25 ns	6.1 ns
t_s (set-up time)	14 ns	5.0 ns	20 ns	2.0 ns
t_h (hold time)	3.0 ns	0.5 ns	5 ns	1.0 ns
t_W (CLK HIGH)	10 ns	5.0 ns	25 ns	4.0 ns
t_W (CLK LOW)	10 ns	5.0 ns	25 ns	5.0 ns
$t_W(\overline{CLR}/\overline{PRE})$	10 ns	5.0 ns	25 ns	4.0 ns
f_{max}	35 MHz	170 MHz	25 MHz	100 MHz
Power, quiescent	0.012 mW	1.1 mW		
Power, 50% duty cycle			44 mW	88 mW

Latches and Flip-Flops

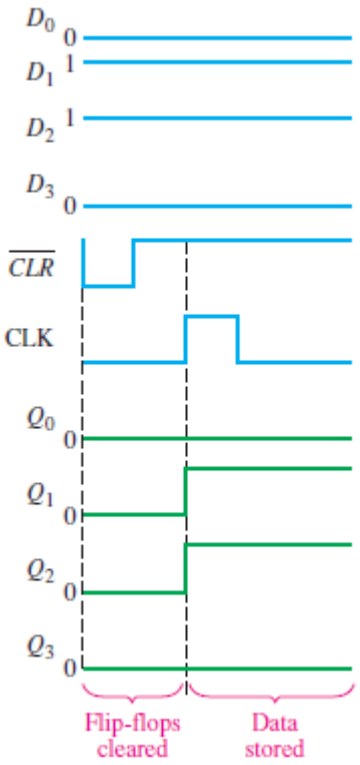
- Flip-Flop Application Examples
  - Parallel data storage
  - Frequency division
  - Counting
  - 555 timer as astable multivibrator

Latches and Flip-Flops

- Flip-Flop Application Examples – parallel data storage



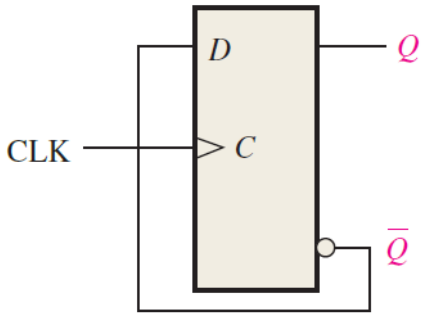
A 4–bit register for data storage

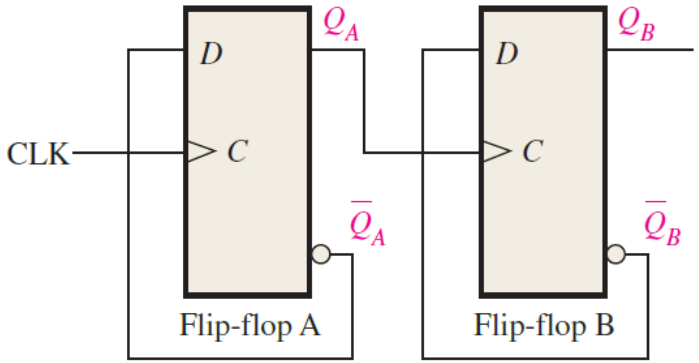


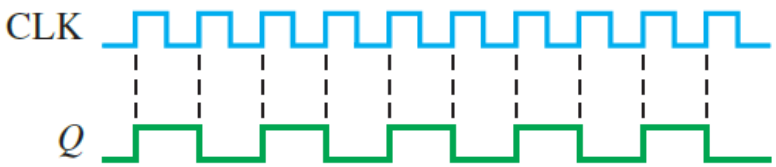
Waveform analysis

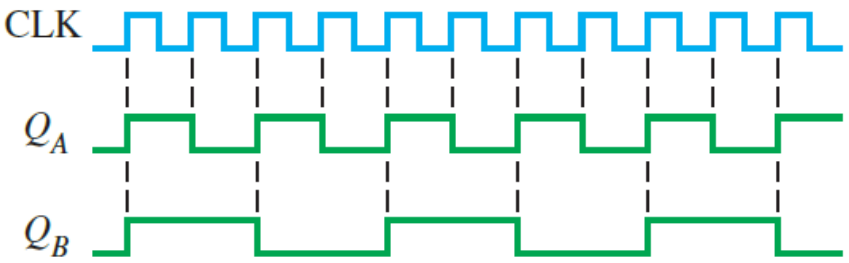
Latches and Flip-Flops

- Flip-Flop Application Examples – frequency division









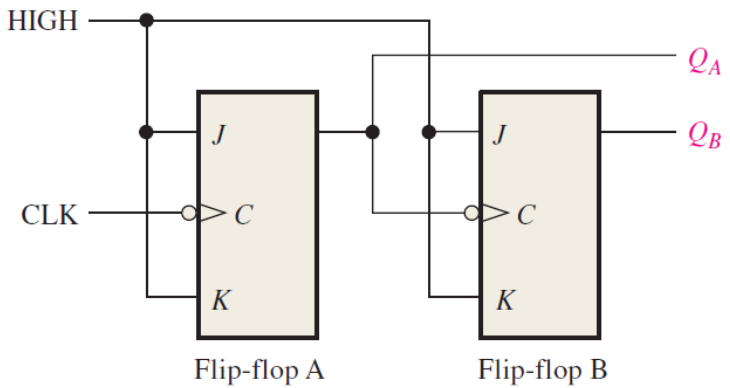
Divide the frequency by 2

Divide the frequency by 4

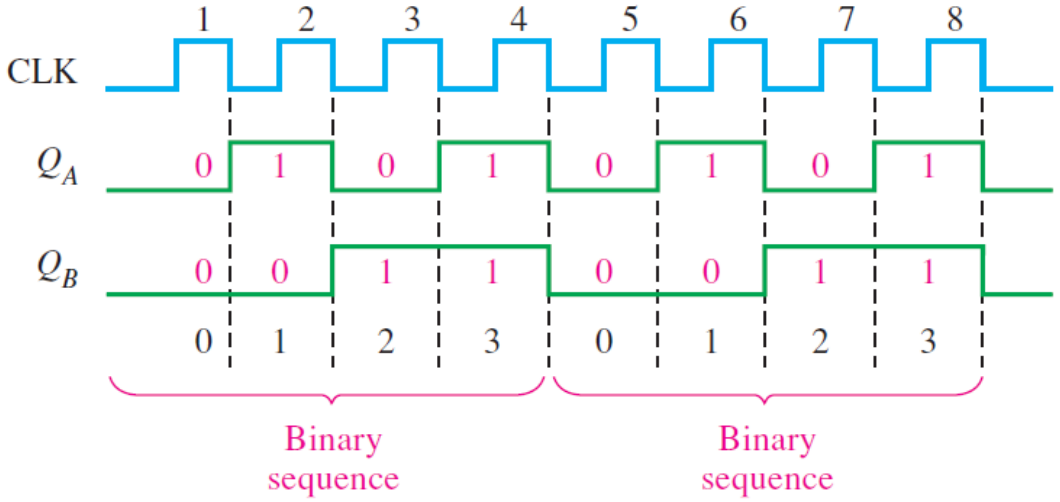
Latches and Flip-Flops

- Flip-Flop Application Examples – counting

J-K flip-flops used to generate a binary counting sequence (00, 01, 10, 11)

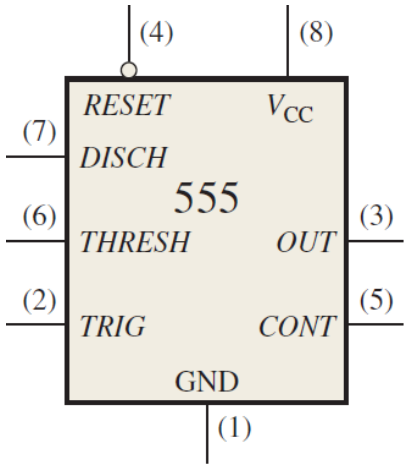


To count the number of pulses in CLK

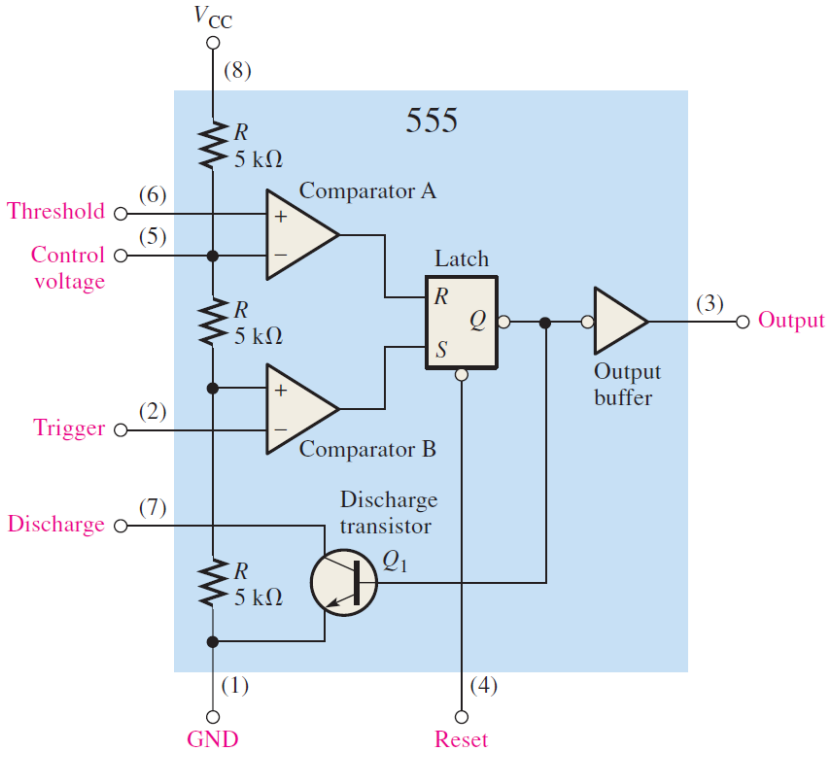


Latches and Flip-Flops

- Flip-Flop Application Examples – 555 timer



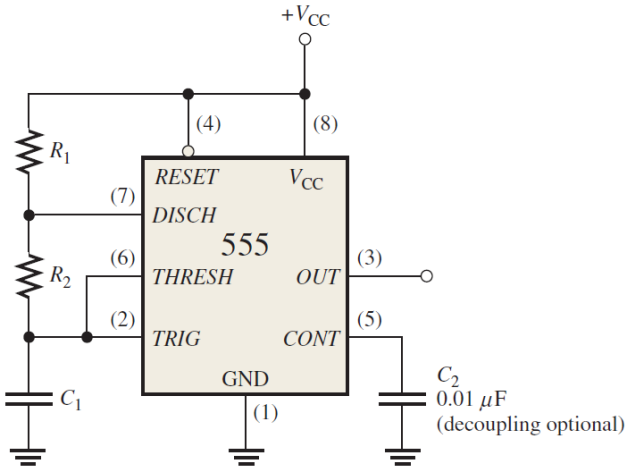
555 timer external view

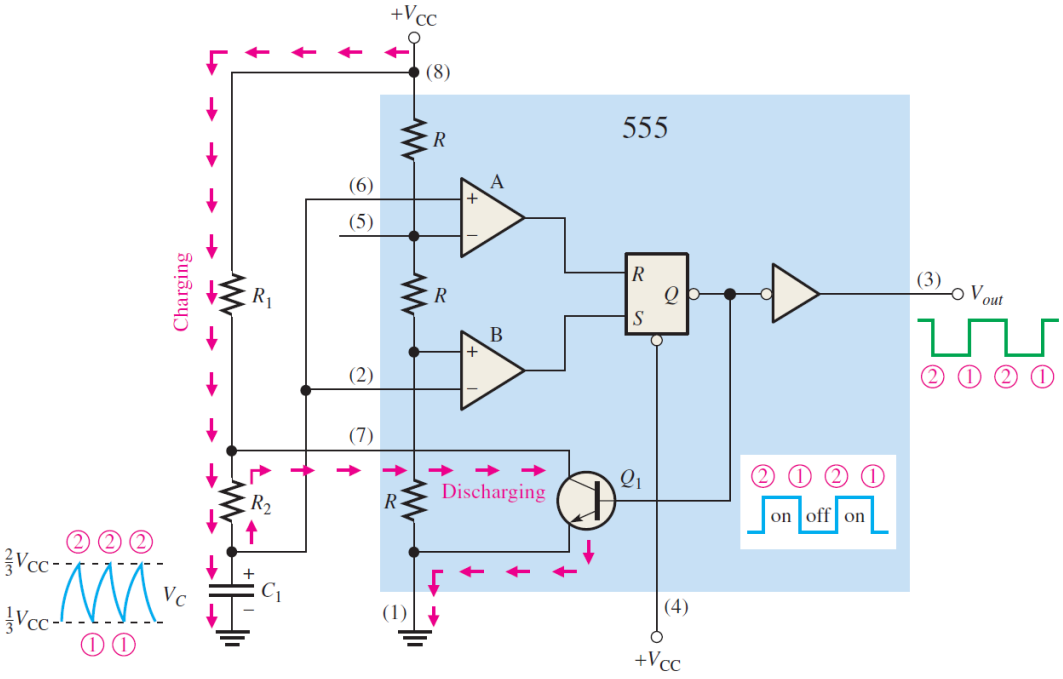


Internal view of 555 timer

Latches and Flip-Flops

- Flip-Flop Application Example
  - 555 timer connected as an astable multivibrator (oscillator)





frequency of the pulses = $\frac{1.44}{(R_1+2R_2)C_1}$