EIE2050
Digital Logic and Systems

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Combinational Logic Analysis

- Basic combinational logic circuits
- Implementing combinational logic
- The universal gates

Reading material: Chapter 5 of Textbook:
Textbook: *Digital Fundamentals (global edition, 11th edition)*, by Thomas Floyd, Pearson 2015.
The examples used in the lecture are based on the textbook.

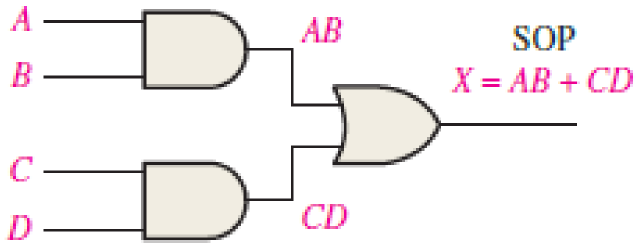
Combinational Logic Analysis

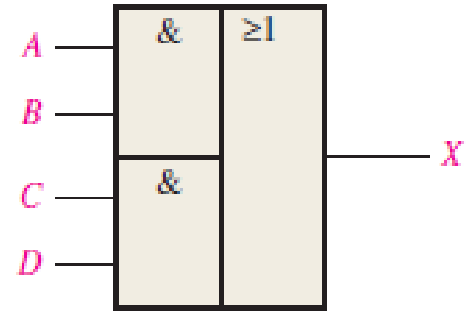
- Basic combinational logic circuits

    - ADD-OR logic
    - ADD-OR-Invert logic
    - Exclusive OR logic
    - Exclusive NOR logic

Combinational Logic Analysis

- Basic combinational logic circuits
  - ADD-OR logic



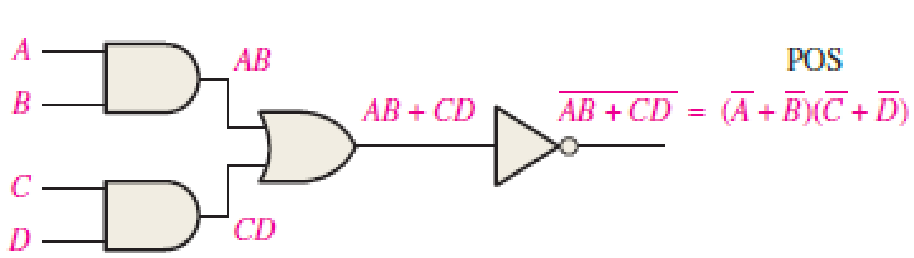


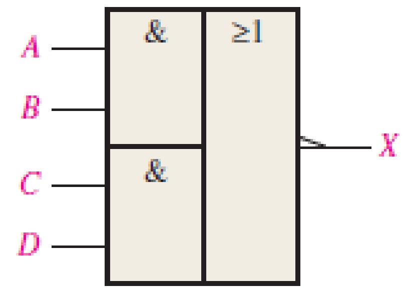
$X = AB + CD$

AND-OR logic directly implements SOP expression

Combinational Logic Analysis

- Basic combinational logic circuits
  - ADD-OR-Invert logic



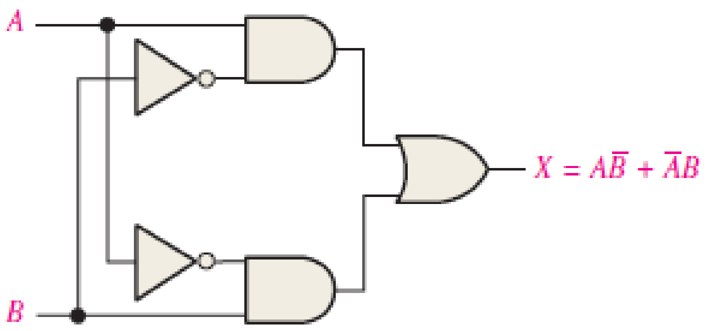


$X = \overline{AB + CD} = (\overline{A} + \overline{B})(\overline{C} + \overline{D})$

AND-OR-Invert logic produces a POS output

Combinational Logic Analysis

- Basic combinational logic circuits
  - Exclusive-OR logic (XOR)



Symbols for XOR

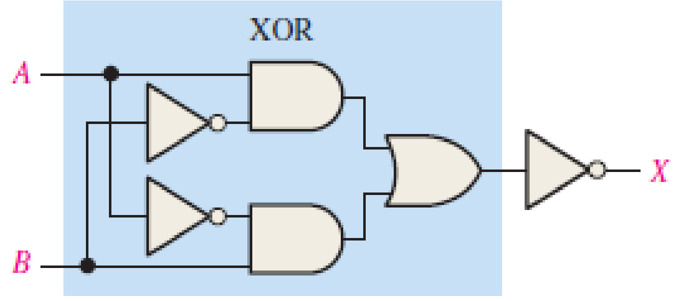
$X = A \oplus B$

$X = A\overline{B} + \overline{A}B$

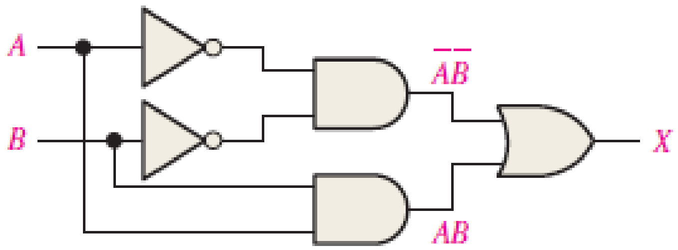
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

Combinational Logic Analysis

- Basic combinational logic circuits
  - Exclusive-NOR logic



$X = A\overline{B} + \overline{A}B$



$X = \overline{A}\overline{B} + AB$

$$X = \overline{A\overline{B} + \overline{A}B} = \overline{A}\overline{B} + AB$$

A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

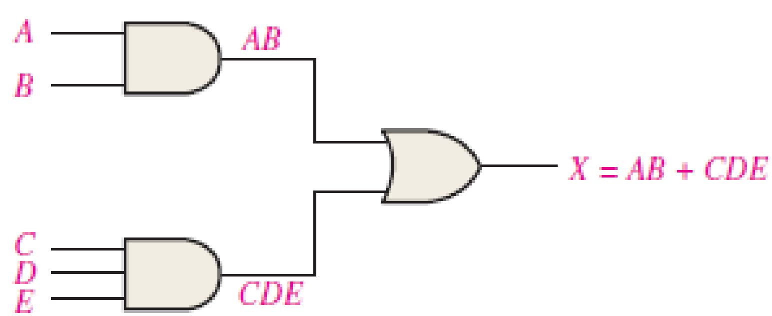
Combinational Logic Analysis

- Implementing combinational logic
  - From Boolean expression to logic circuit

Given expression: $X = AB + CDE$

Analyze: $X = \overset{\text{AND}}{AB} \underset{\text{OR}}{+} \overset{\text{AND}}{CDE}$

Resulting logic circuit:

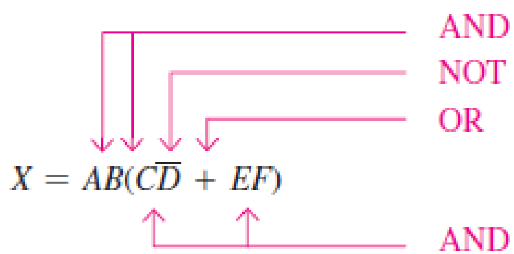


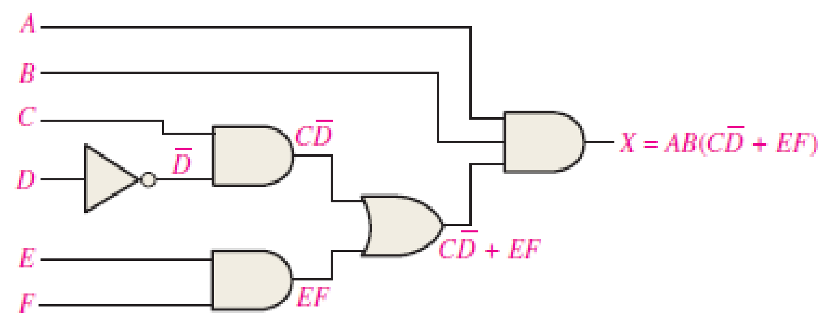
Combinational Logic Analysis

- Implementing combinational logic
  - From Boolean expression to logic circuit

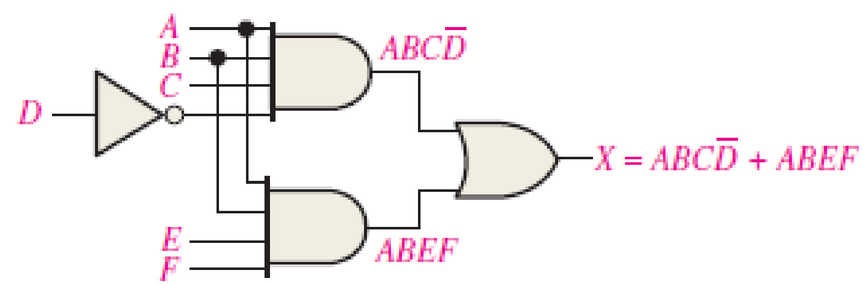
Given expression: $X = AB(C\overline{D} + EF)$

Analysis and results:





SOP implementation: $AB(C\overline{D} + EF) = ABC\overline{D} + ABEF$



Combinational Logic Analysis

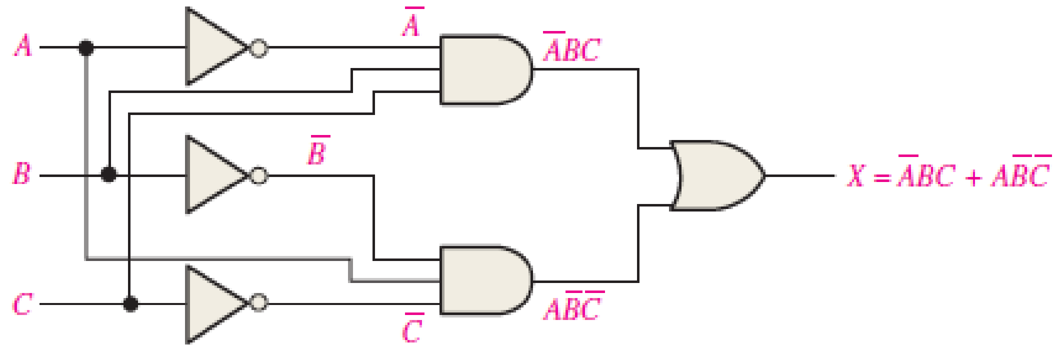
- Implementing combinational logic
  - From truth table to logic circuit

Given truth table:

Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

$\overline{A}BC$
$A\overline{B}\,\overline{C}$

Resulting logic circuit:



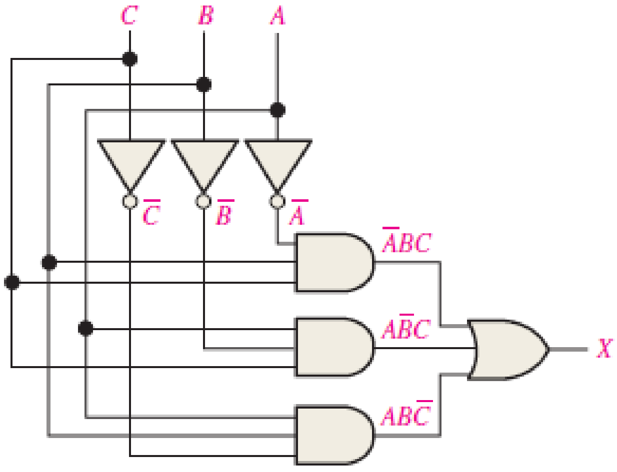
Combinational Logic Analysis

- Implementing combinational logic
  - From truth table to logic circuit

Given truth table:

Inputs			Output	
A	B	C	X	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	$\overline{A}BC$
1	0	0	0	
1	0	1	1	$A\overline{B}C$
1	1	0	1	$AB\overline{C}$
1	1	1	0	

Resulting logic circuit:

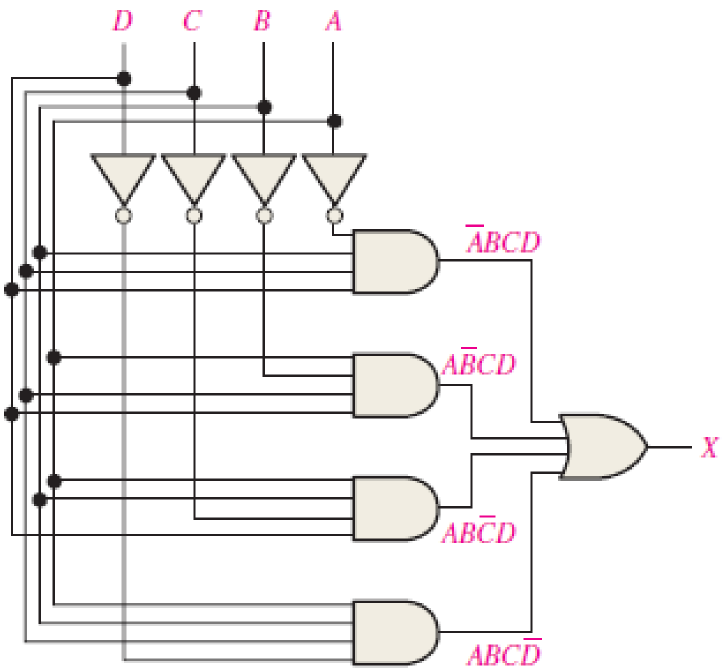


Combinational Logic Analysis

- Implementing combinational logic
  - Example: develop a logic circuit with four variables that will only produce a 1 output when exactly three input variables are 1s.

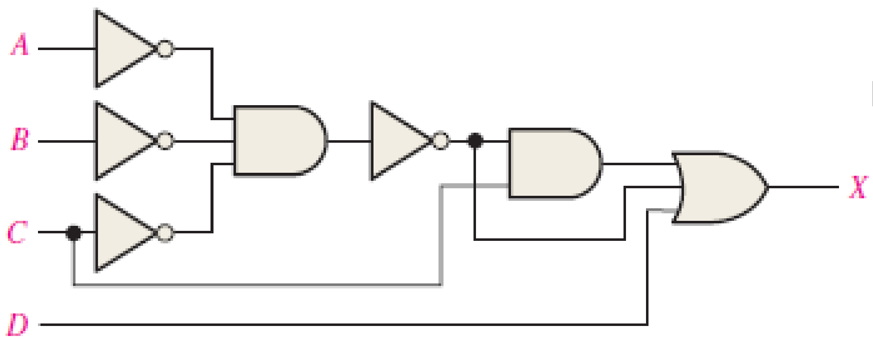
A	B	C	D	Product Term
0	1	1	1	$\overline{A}BCD$
1	0	1	1	$A\overline{B}CD$
1	1	0	1	$AB\overline{C}D$
1	1	1	0	$ABC\overline{D}$

$$X = \overline{A}BCD + A\overline{B}CD + AB\overline{C}D + ABC\overline{D}$$



Combinational Logic Analysis

- Implementing combinational logic
  - Simplify the logic circuit to minimum form



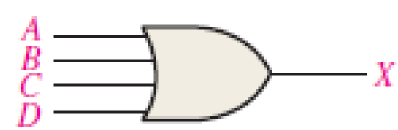
Boolean expression:

$$X = (\overline{\overline{A}\,\overline{B}\,\overline{C}})C + \overline{\overline{A}\,\overline{B}\,\overline{C}} + D$$

Simplify the Boolean expression:

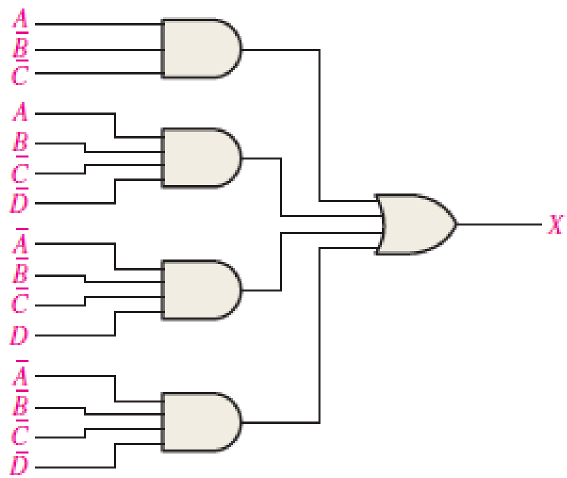
$$\begin{aligned} X &= (\overline{\overline{A}\,\overline{B}\,\overline{C}})C + \overline{\overline{A}\,\overline{B}\,\overline{C}} + D \\ &= A + B + C + D \end{aligned}$$

Simplified logic circuit:



Combinational Logic Analysis

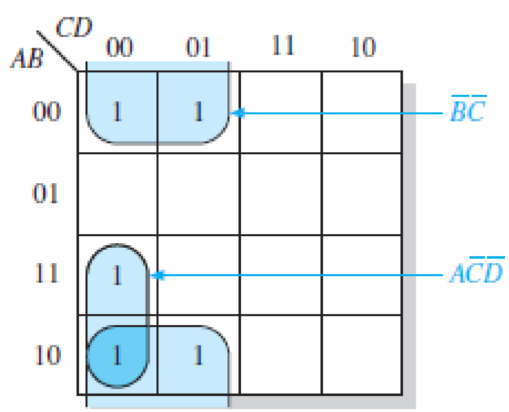
- Implementing combinational logic
  - Simplify the logic circuit to minimum form



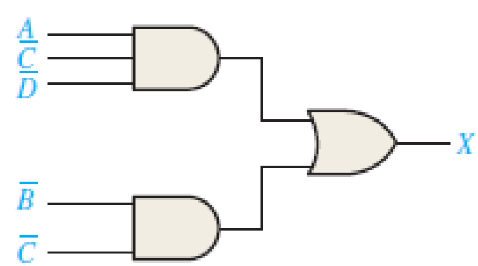
Boolean expression:

$$X = A\overline{B}\,\overline{C} + AB\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}D + \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$$

Karnaugh map:



Minimum logic circuit:



Combinational Logic Analysis

- Implementing combinational logic
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A	B	C	D	Product Term
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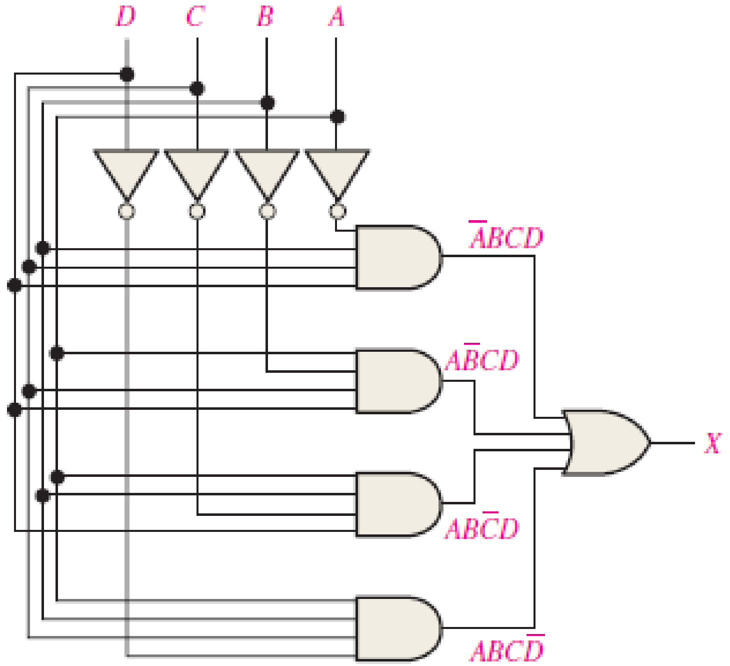
1	0	1	1	$A\overline{B}CD$
1	1	0	1	$AB\overline{C}D$
1	1	1	0	$ABC\overline{D}$

$$X = \overline{A}BCD + A\overline{B}CD + AB\overline{C}D + ABC\overline{D}$$



Combinational Logic Analysis

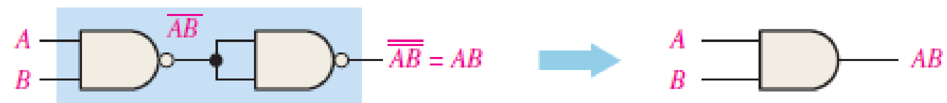
- Universal gates
  - NAND gate
  - NOR gate

Combinational Logic Analysis

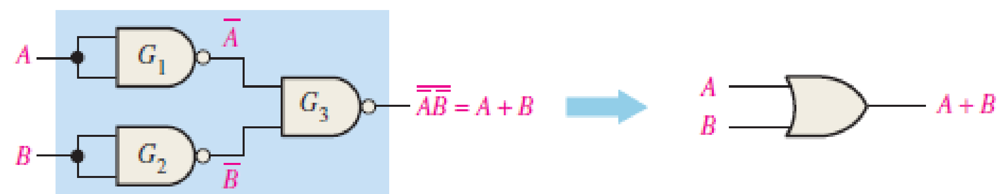
- Universal gates
  - NAND gate as a universal logic element

One NAND gate used as an inverter:

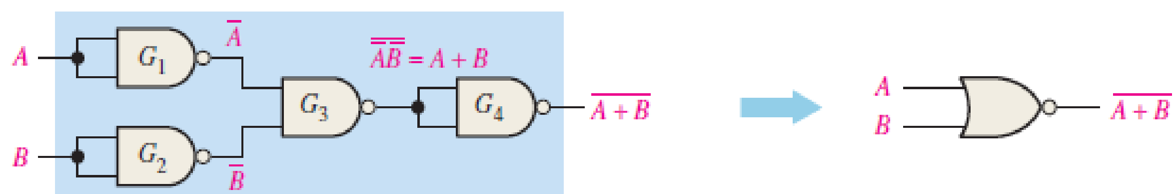
Two NAND gates used as an AND gate:



Three NAND gates used as an OR gate:



Four NAND gates used as a NOR gate:

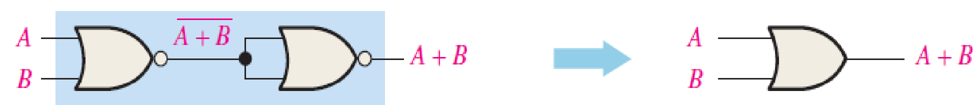


Combinational Logic Analysis

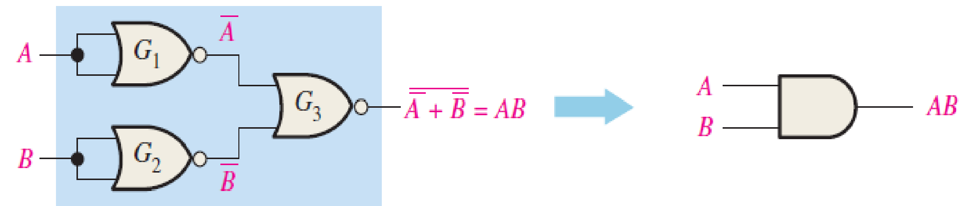
- Universal gates
  - NOR gate as a universal logic element

One NOR gate used as an inverter:

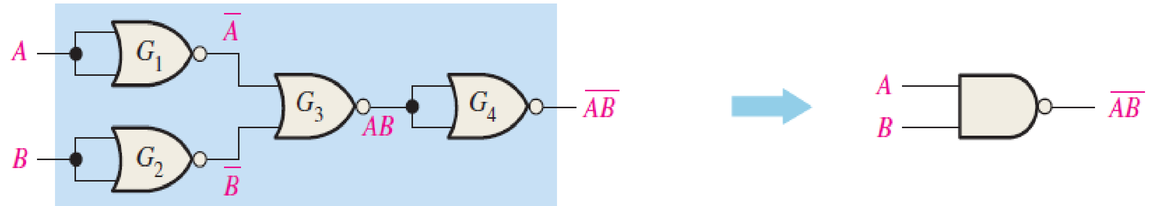
Two NOR gates used as an OR gate:



Three NOR gates used as an AND gate:



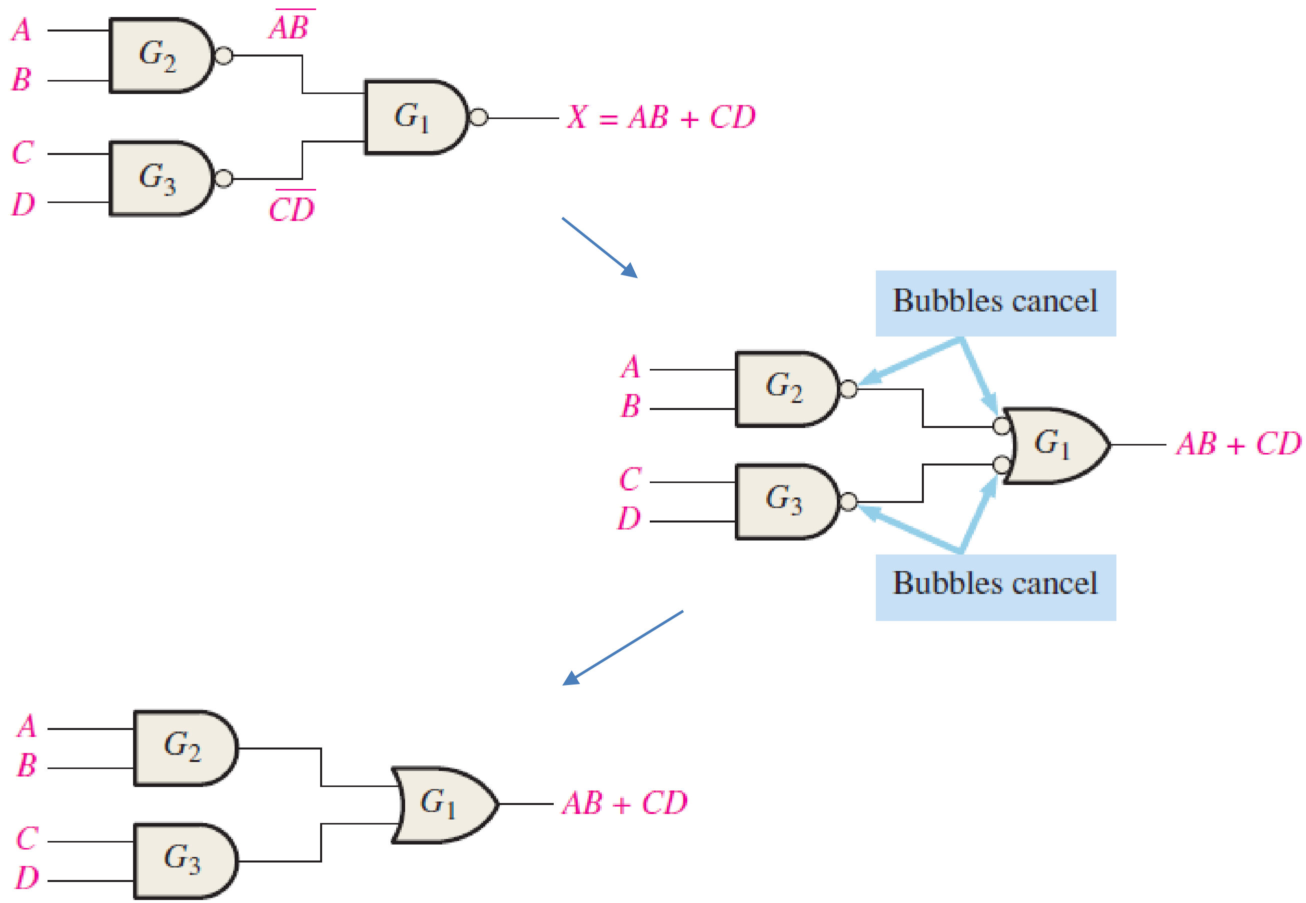
Four NOR gates used as a NAND gate:



Combinational Logic Analysis

- Universal gates
  - Combinational logic using NAND gates

Logic circuit using NAND gates:

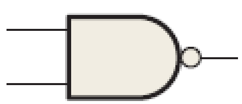


AND-OR equivalent:

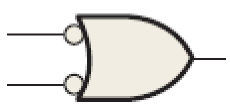
Combinational Logic Analysis

- Universal gates
  - Dual symbols for NAND logic:

    NAND symbol

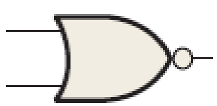
    

    negative-OR symbol

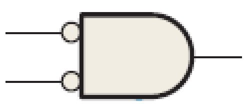
    

    Dual symbols for NOR logic:

    NOR symbol

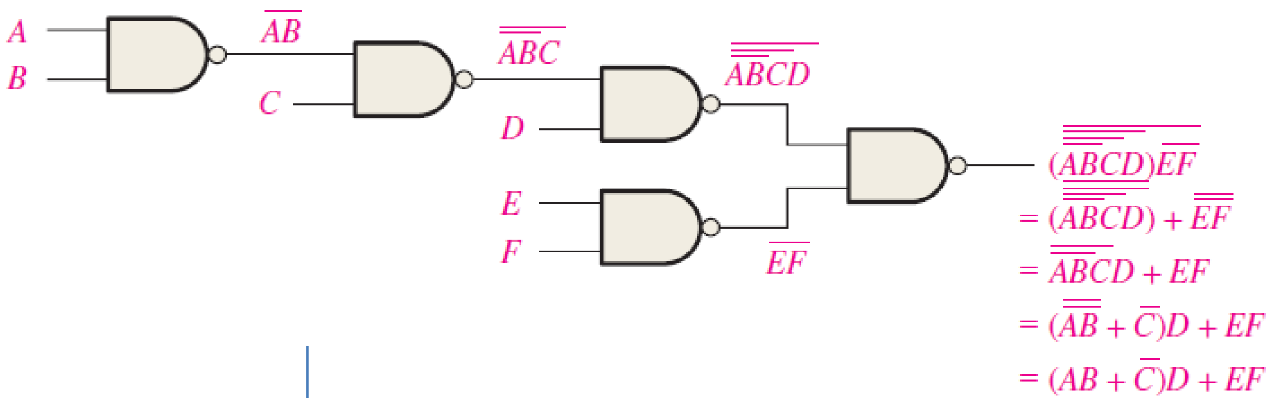
    negative-AND symbol

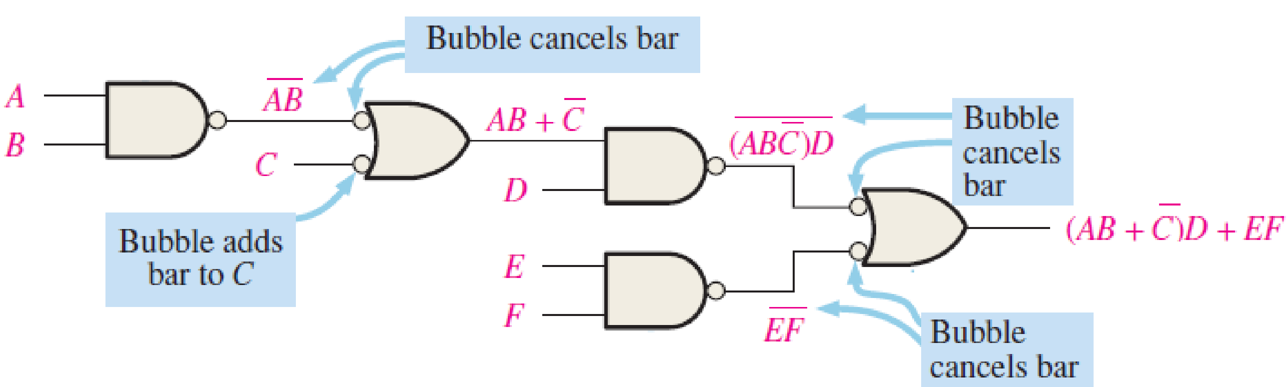
    

  - logic diagrams using dual symbols, Guidelines for connections:
    - bubble-to-bubble ← yes
    - nonbubble-to-nonbubble ← yes
    - bubble-to-nonbubble ← no
    - nonbubble-to-bubble ← no

Combinational Logic Analysis

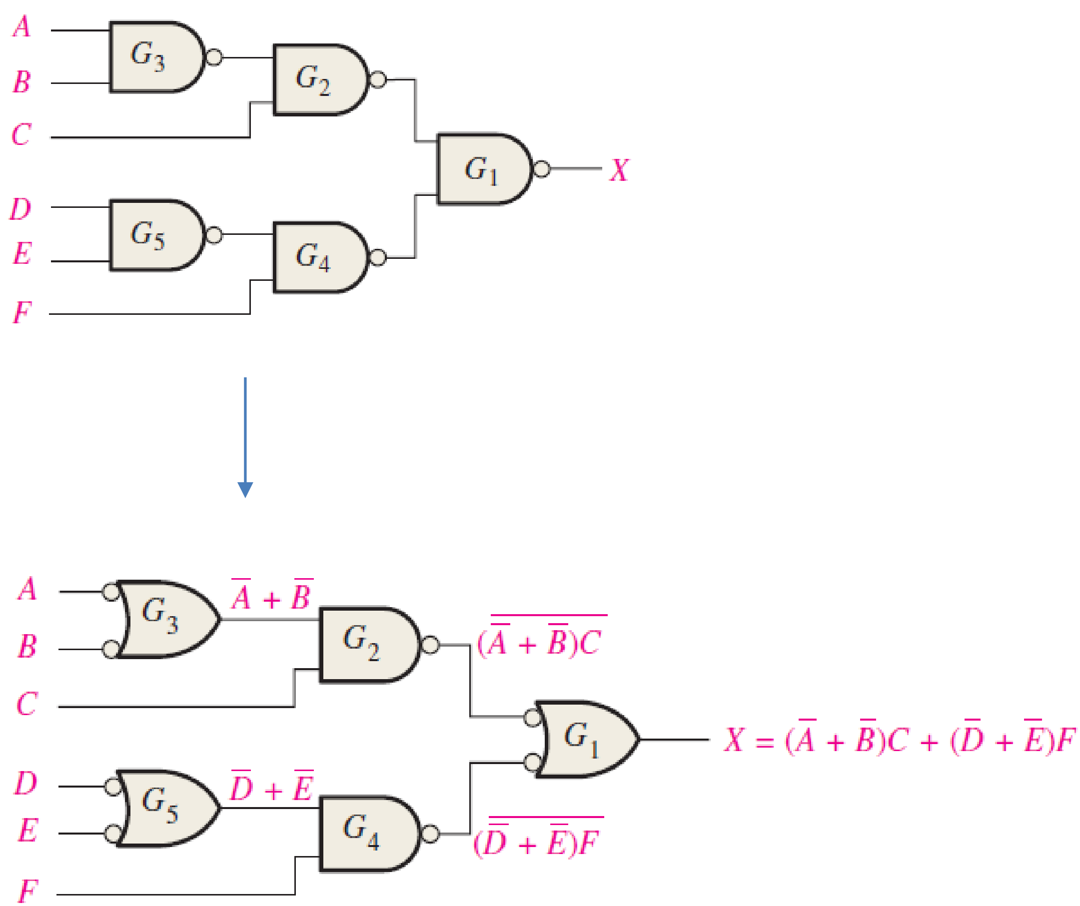
- Universal gates
  - NAND logic diagrams using dual symbols





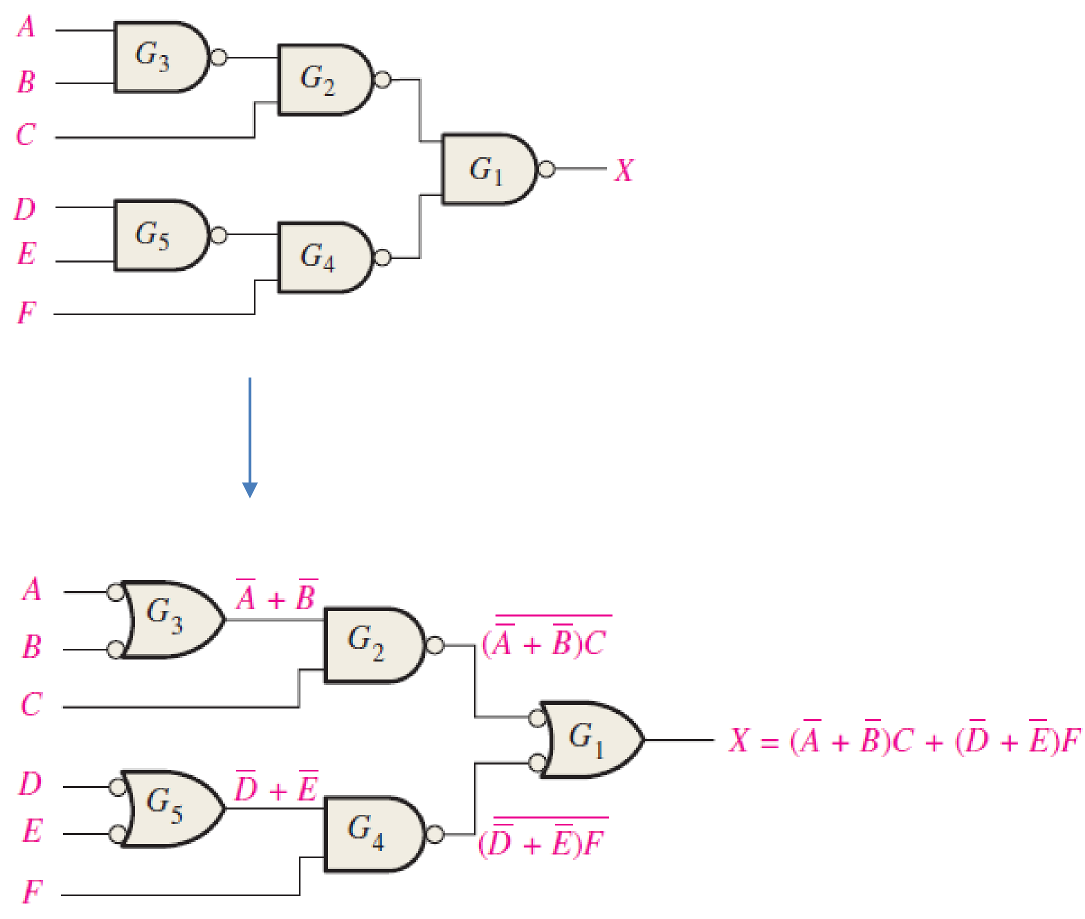
Combinational Logic Analysis

- Universal gates
  - NAND logic diagrams using dual symbols



Combinational Logic Analysis

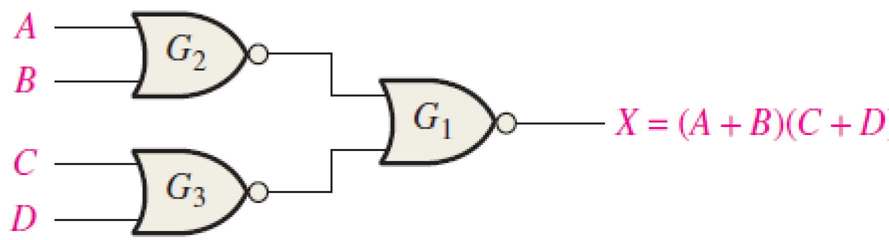
- Universal gates
  - NAND logic diagrams using dual symbols



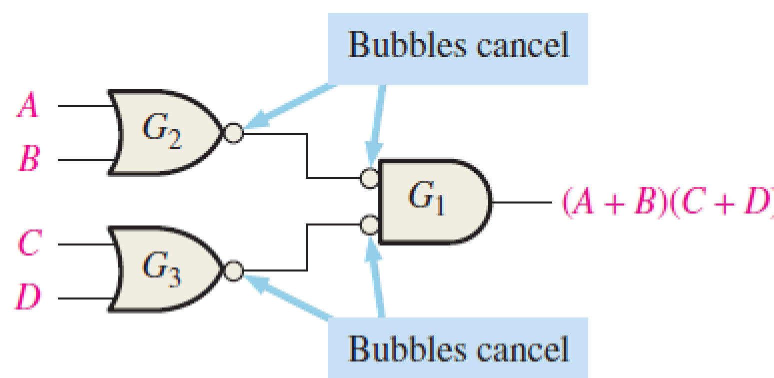
Combinational Logic Analysis

- Universal gates
  - Combinational logic using NOR gates

Logic circuit using NOR gates:

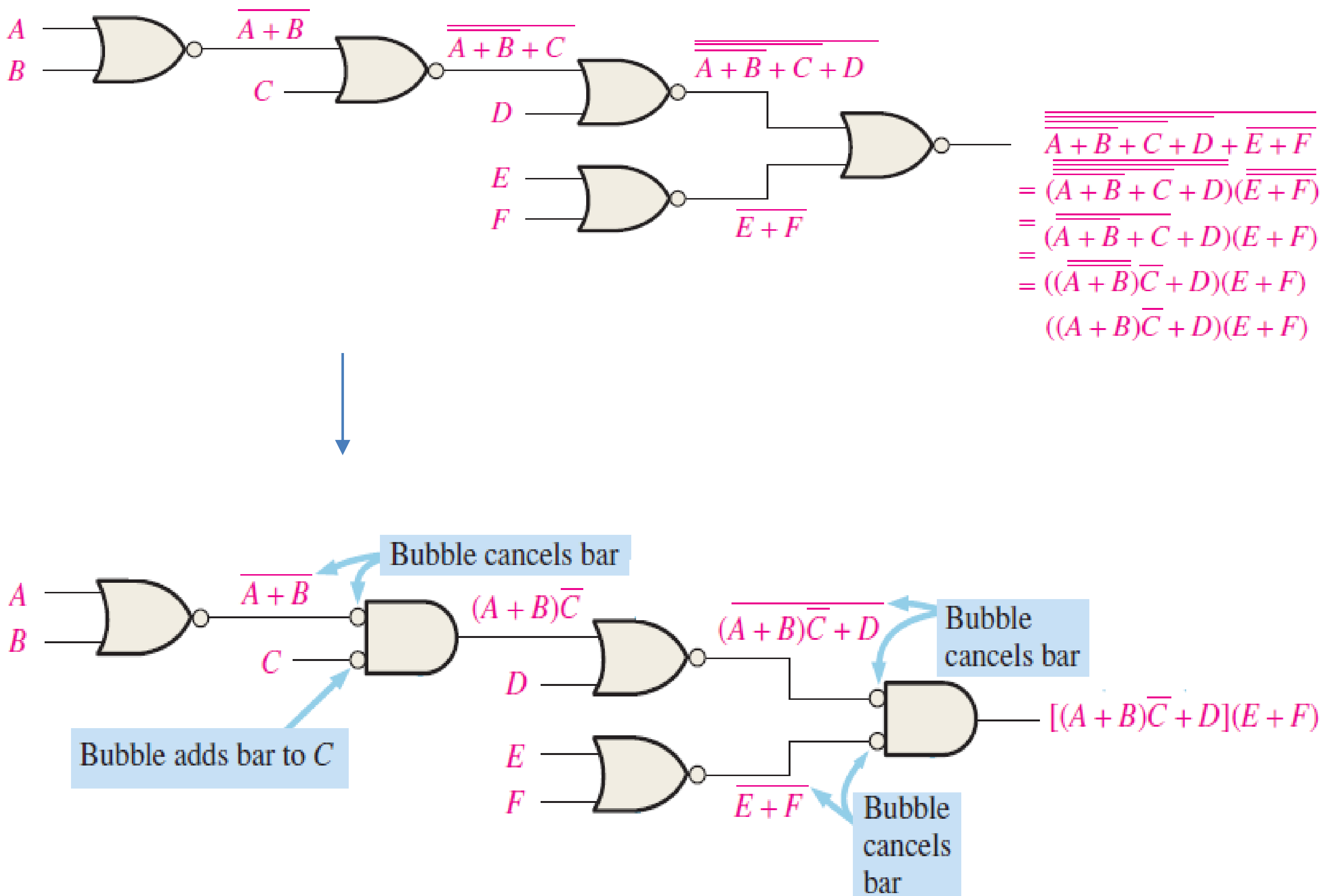


Redrawn with negative AND symbol for G_1 :



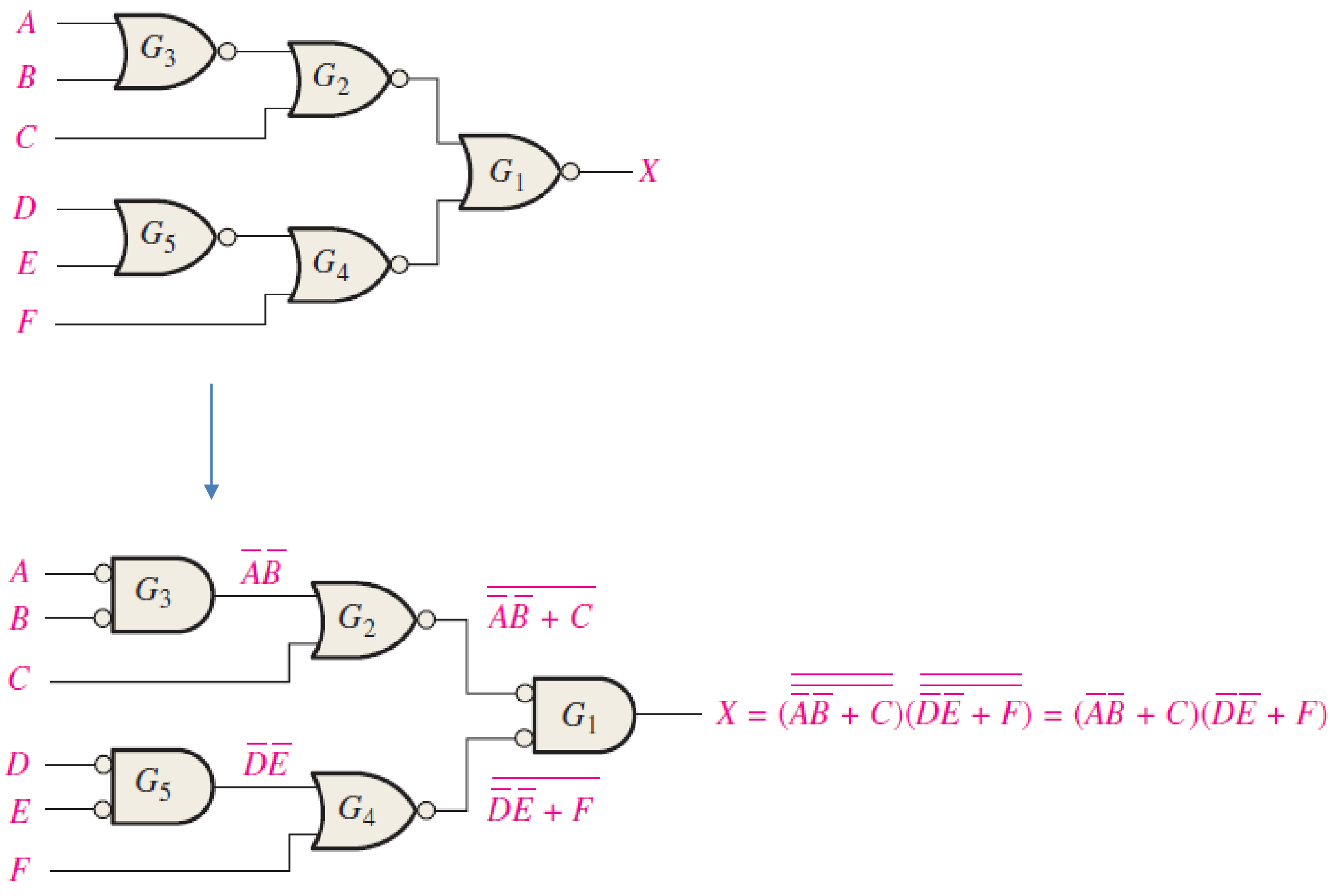
Combinational Logic Analysis

- Universal gates
  - NOR logic diagrams using dual symbols



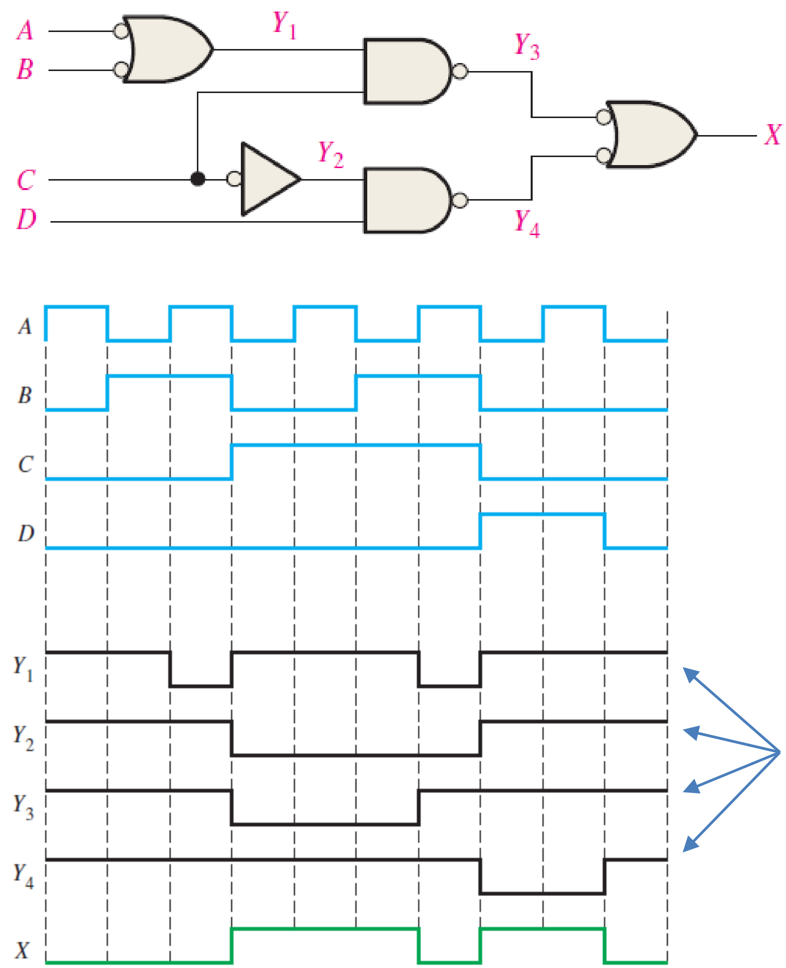
Combinational Logic Analysis

- Universal gates
  - NOR logic diagrams using dual symbols



Combinational Logic Analysis

- Waveform operations



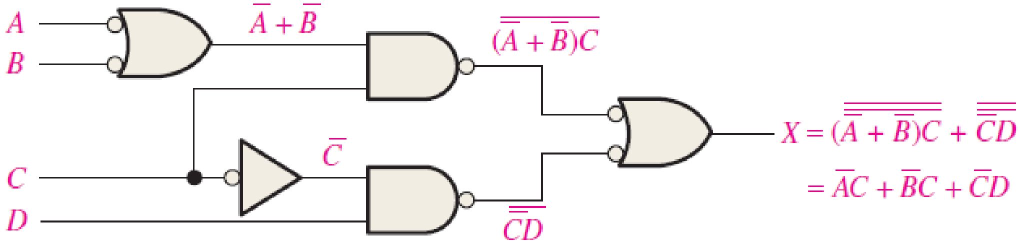
Given input waveforms:

Evaluate Intermediate waveforms

Determine output waveform:

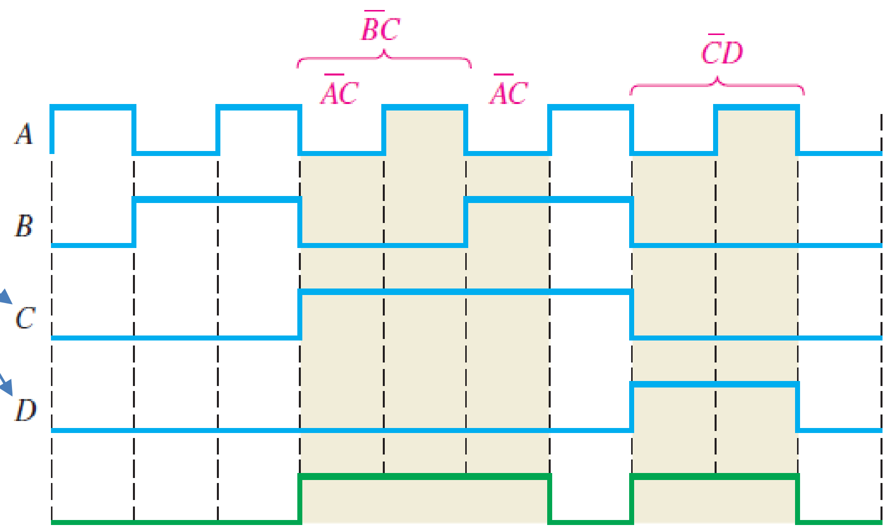
Combinational Logic Analysis

- Waveform operations



Derive output expression
Simplify the expression

Given input waveforms:



Determine output waveform according to simplified logic Expression:

$X = \overline{A}C + \overline{B}C + \overline{C}D$