EIE2050
Digital Logic and Systems

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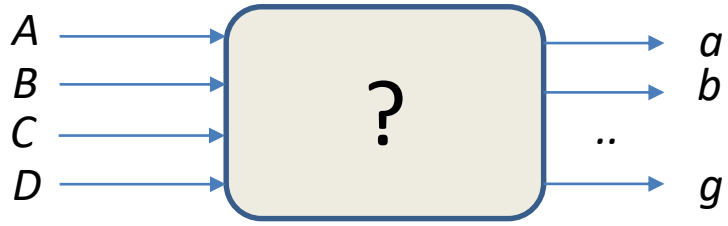
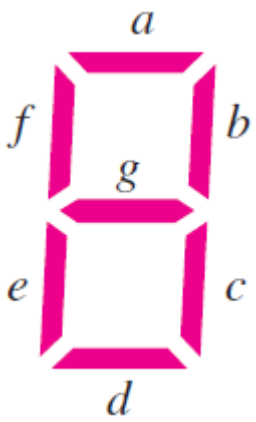
VHDL Basics

- Programmable Logic Devices
- VHDL

7-Segment Display Example





Segment a: 0, 2, 3, 5, 6, 7, 8, 9

b: 0, 1, 2, 3, 4, 7, 8, 9

Standard SOP:

$$Xa = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + \bar{A}BCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D$$

$$Xb = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + \bar{A}BCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D$$

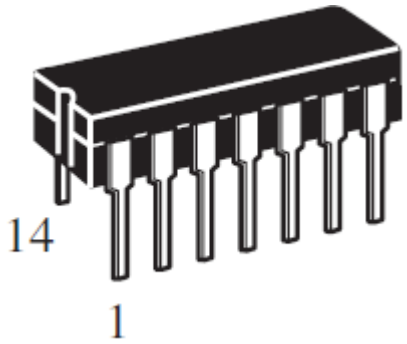
Minimum SOP:

$$Xa = A + C + BD + \bar{B}\bar{D}$$

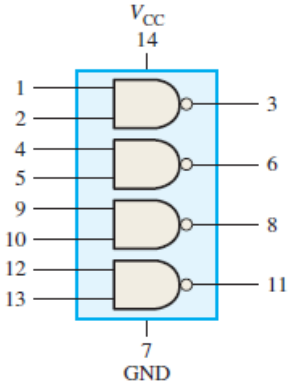
$$Xb = \bar{B} + CD + \bar{C}\bar{D}$$

Fixed Function Logic Gates

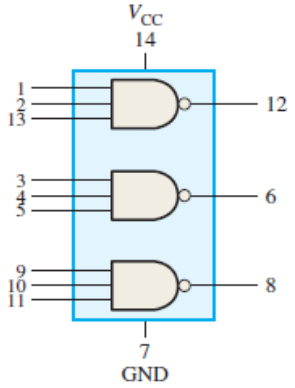
- They are non-programmable:

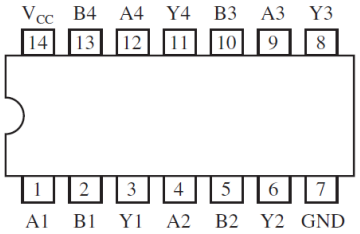


74HC00

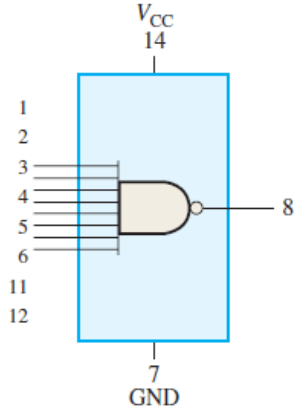


74LS10

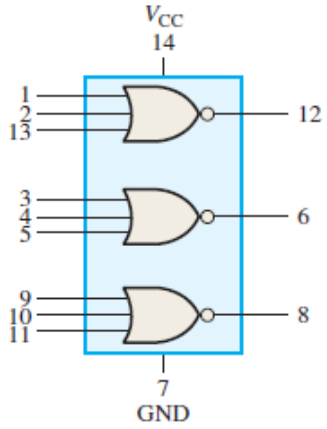




74HC30

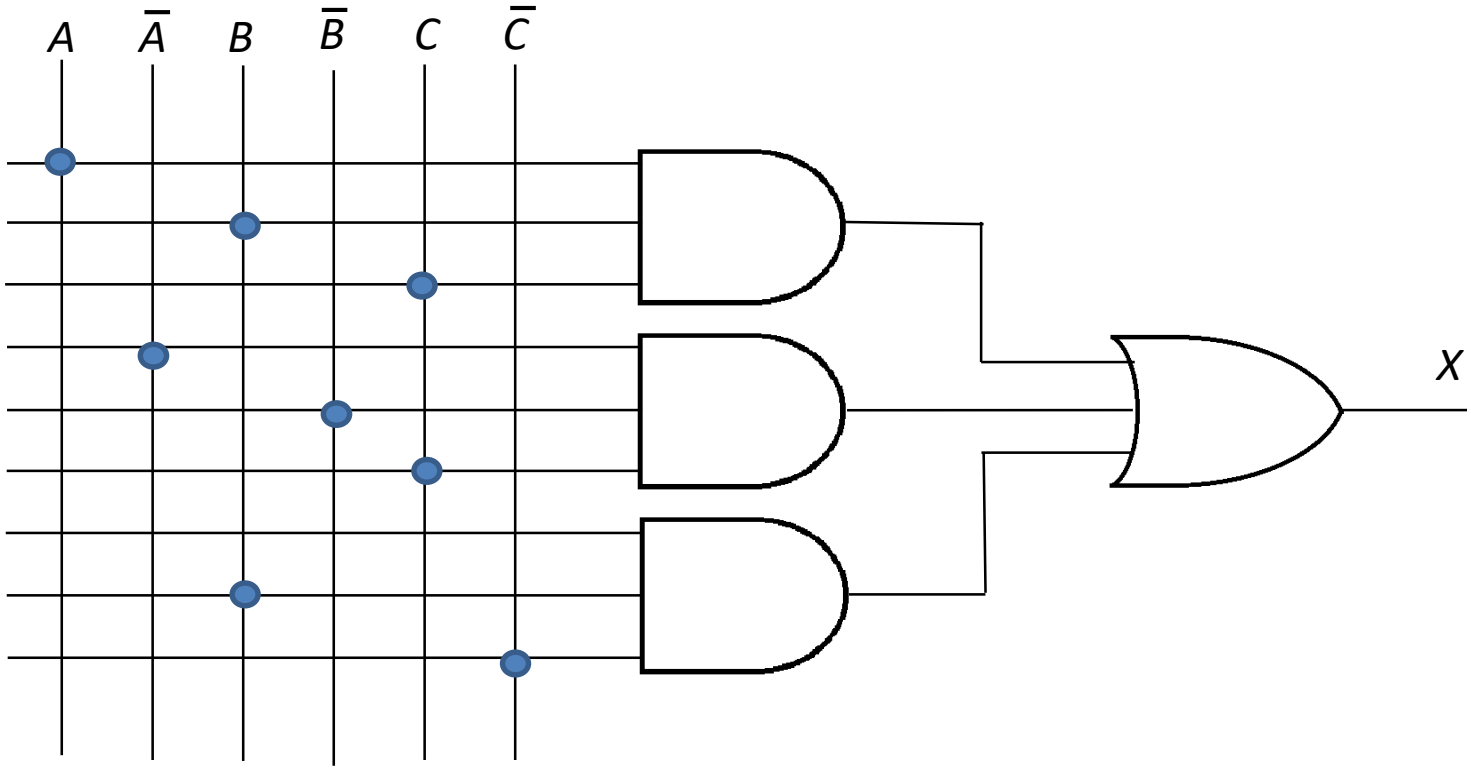


74LS27



Programmable Logic Devices

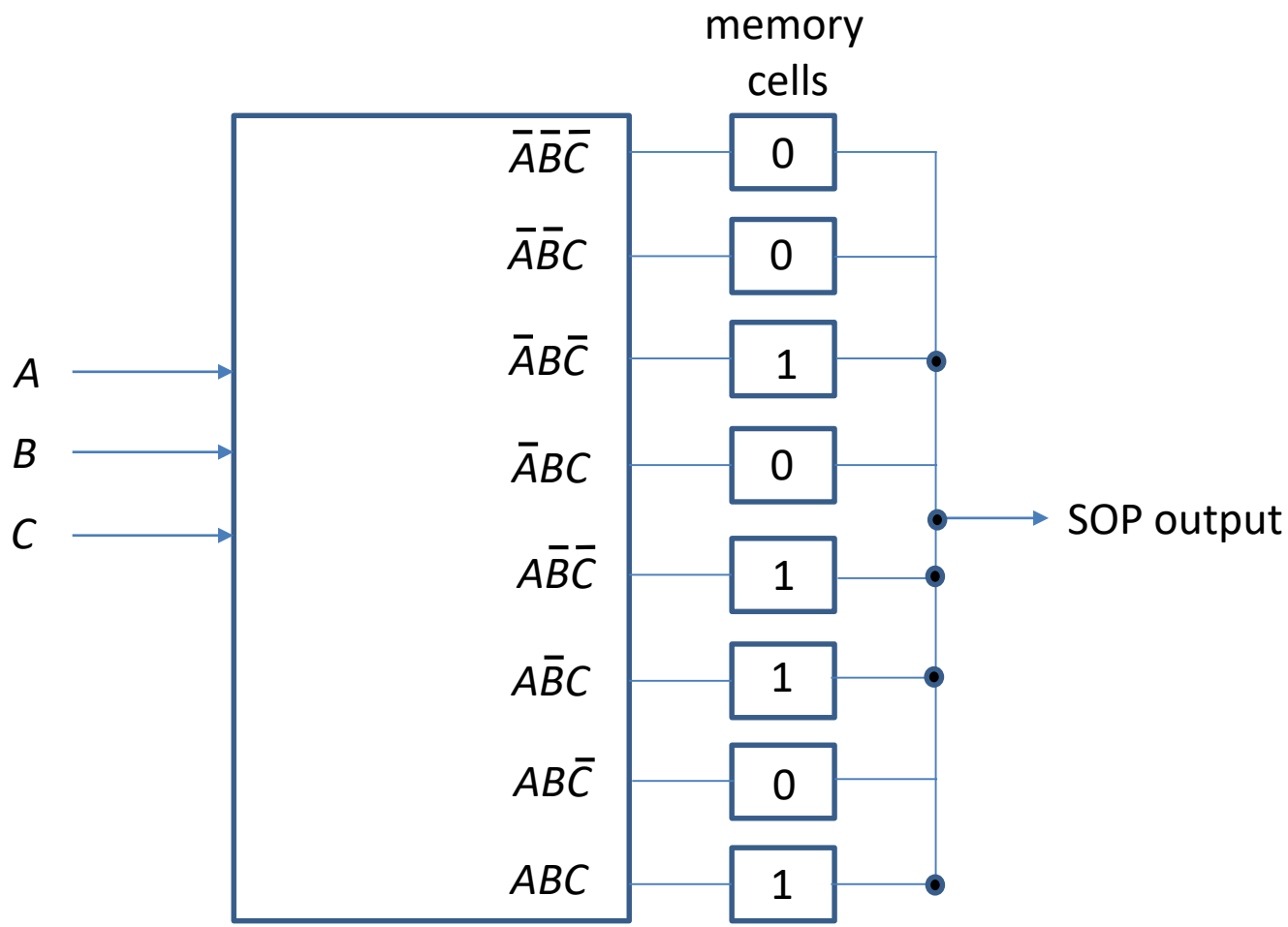
- Programmable Array Logic



The connections can be “programmed”

Programmable Logic Devices

- LUT (look up table):



The values in the memory cells are “programmed”

Programmable Logic Devices

- Simple Programmable Logic Devices (SPLD)
- Complex Programmable Logic Devices (CPLD)

  e.g., with 10-1700 macrocells

  10-1156 I/Os

- Field Programmable Gate Array (FPGA)

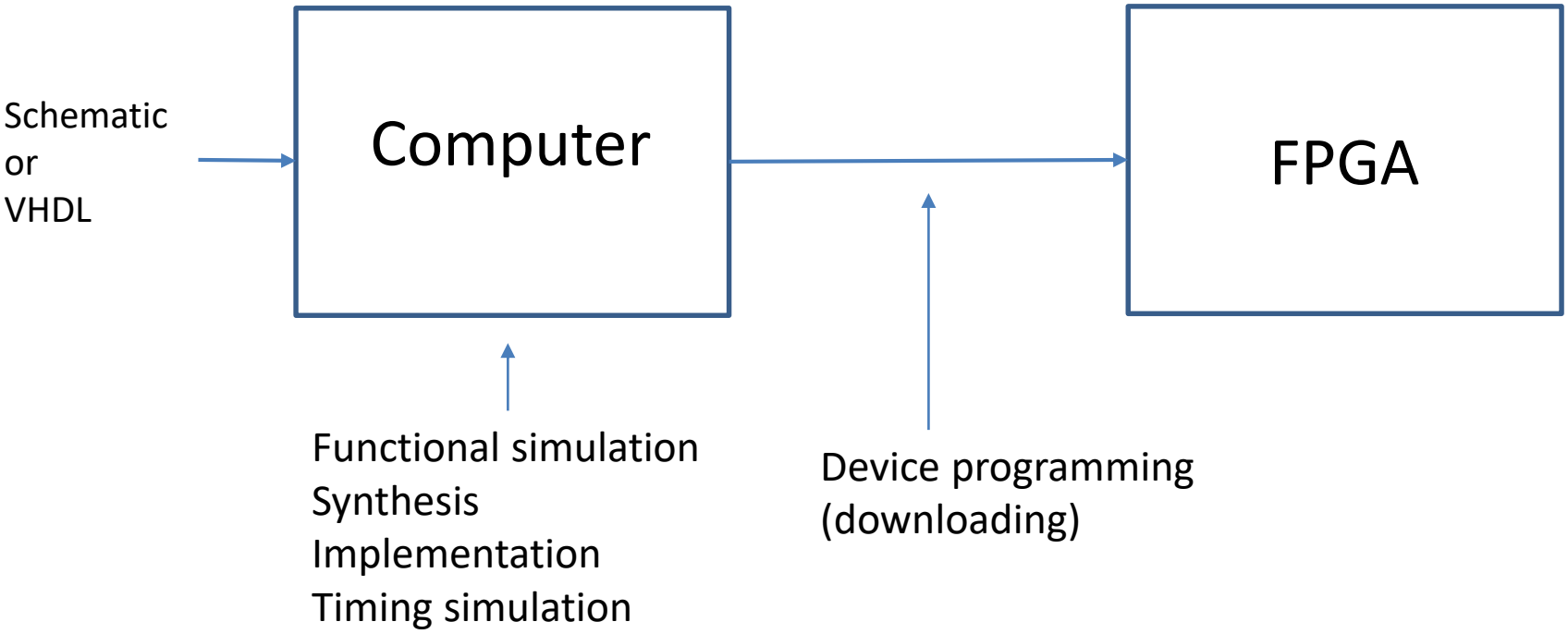
  e.g., with 26 to 359,000 CLBs (configurable logic block)

  each CLB consists of several logic modules

  18-1200 I/Os

  with 50 million gates

Programming FPGA



VHDL

- VHDL is a hardware description language

For example, a 7-segment display:

$X_a = A + C + BD + \bar{B}\bar{D}$

$X_b = \bar{B} + CD + \bar{C}\bar{D}$

VHDL program is

```
entity DisplaySegments is
        port (A, B, C, D: in bit; Xa, Xb: out bit);
end entity DisplaySegments
architecture Expression1 of DisplaySegments is
begin
        Xa <= A or C or (B and D) or (not B and not D);
        Xb <= not B or (C and D) or (not C and not D);
end architecture Expression1
```