

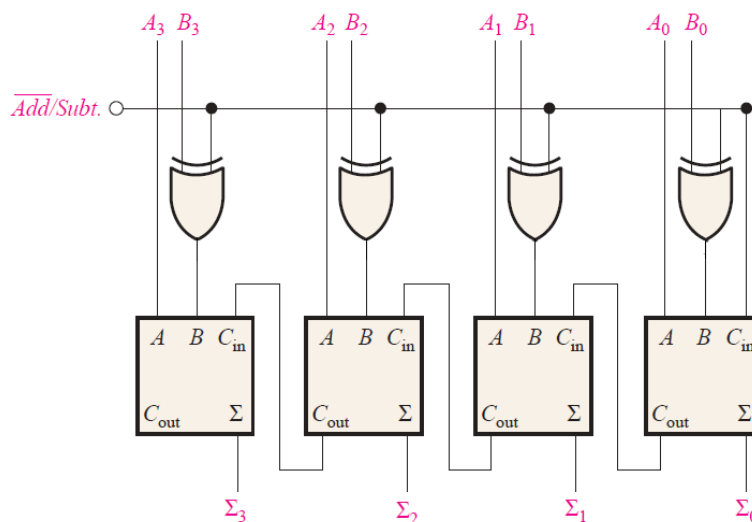
## EIE2050 Assignment 3

Answer the questions and submit hardcopy to TC fifth floor before **5:30pm, 5th December**.

Note: 1. There are 15 questions.  
2. A zero mark will be given if any plagiarism is found.

1.

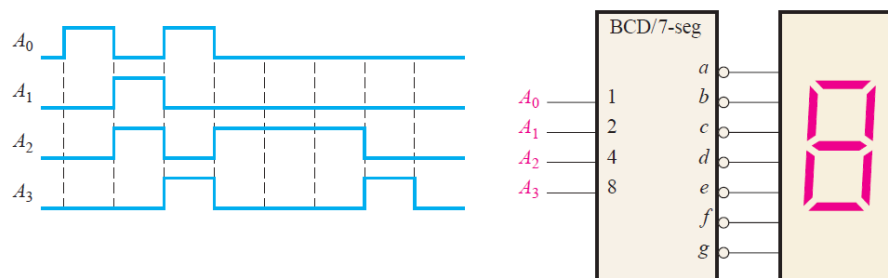
The circuit shown in Figure 6–71 is a 4-bit circuit that can add or subtract numbers in a form used in computers (positive numbers in true form; negative numbers in complement form). (a) Explain what happens when the  $\overline{Add/Subt.}$  input is HIGH. (b) What happens when  $\overline{Add/Subt.}$  is LOW?



**FIGURE 6-71**

2.

A 7-segment decoder/driver drives the display in Figure 6–78. If the waveforms are applied as indicated, determine the sequence of digits that appears on the display.



**FIGURE 6-78**

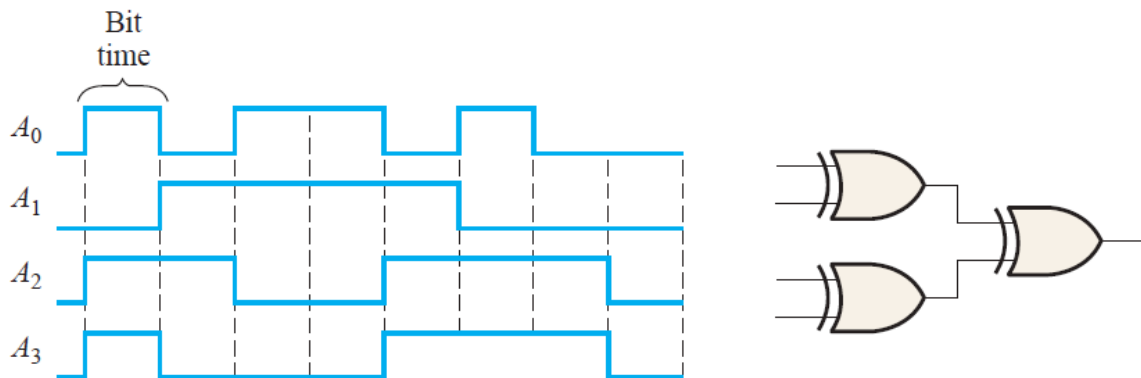
3.

Show the logic required to convert a 10-bit binary number to Gray code and use that logic to convert the following binary numbers to Gray code:

(a) 1010111100      (b) 1111000011      (c) 1011110011      (d) 1000000001

4.

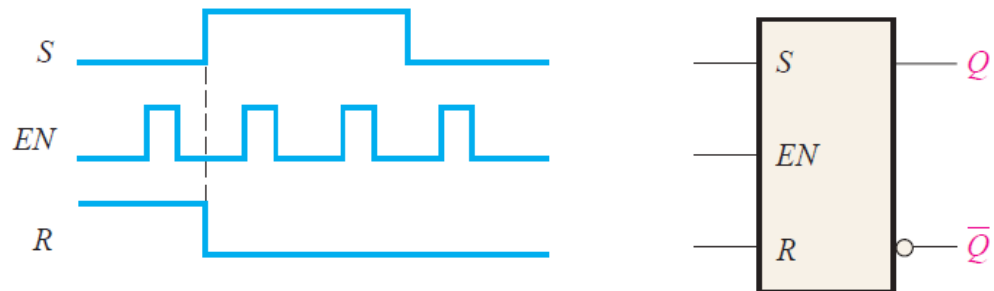
The waveforms in Figure 6–82 are applied to the 4-bit parity logic. Determine the output waveform in proper relation to the inputs. For how many bit times does even parity occur, and how is it indicated? The timing diagram includes eight bit times.



**FIGURE 6–82**

5.

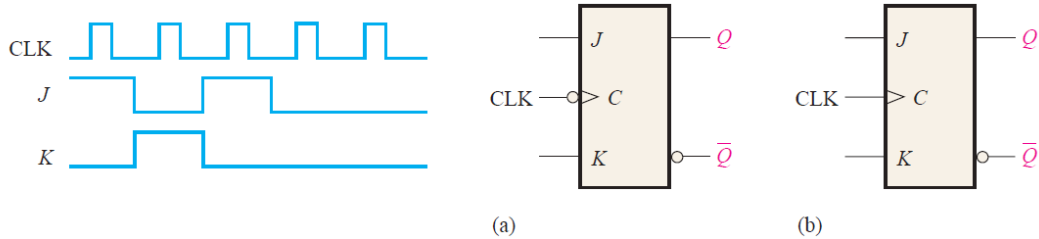
For a gated S-R latch, determine the  $Q$  and  $\bar{Q}$  outputs for the inputs in Figure 7–73. Show them in proper relation to the enable input. Assume that  $Q$  starts LOW.



**FIGURE 7–73**

6.

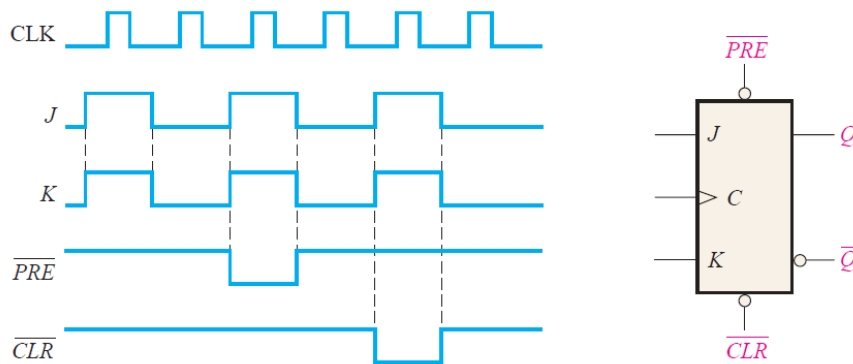
Two edge-triggered J-K flip-flops are shown in Figure 7-77. If the inputs are as shown, draw the  $Q$  output of each flip-flop relative to the clock, and explain the difference between the two. The flip-flops are initially RESET.



**FIGURE 7-77**

7.

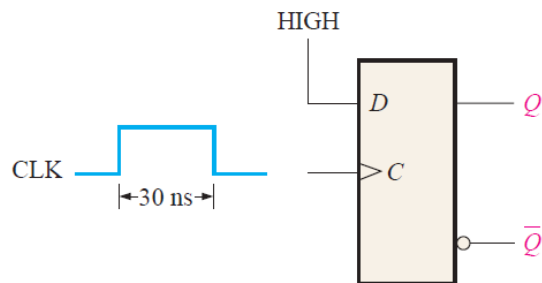
Determine the  $Q$  waveform relative to the clock if the signals shown in Figure 7-83 are applied to the inputs of the J-K flip-flop. Assume that  $Q$  is initially LOW.



**FIGURE 7-83**

8.

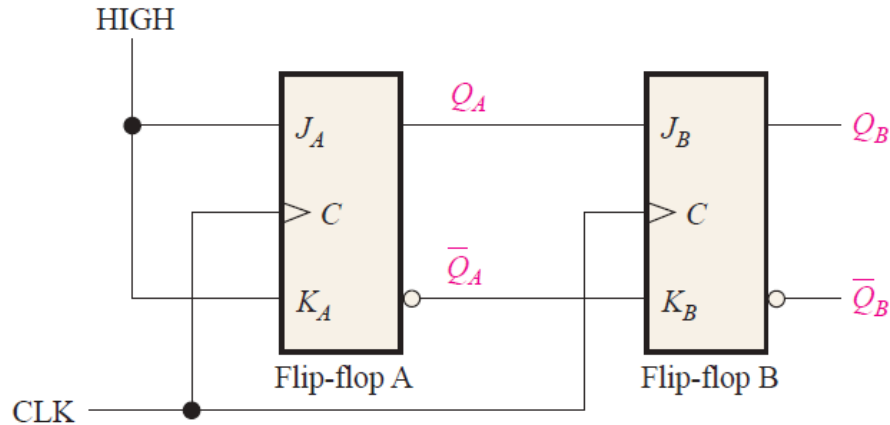
The flip-flop in Figure 7-88 is initially RESET. Show the relation between  $Q$  output and the clock pulse if the propagation delay  $t_{PLH}$  (clock to  $Q$ ) is 5 ns.



**FIGURE 7-88**

9.

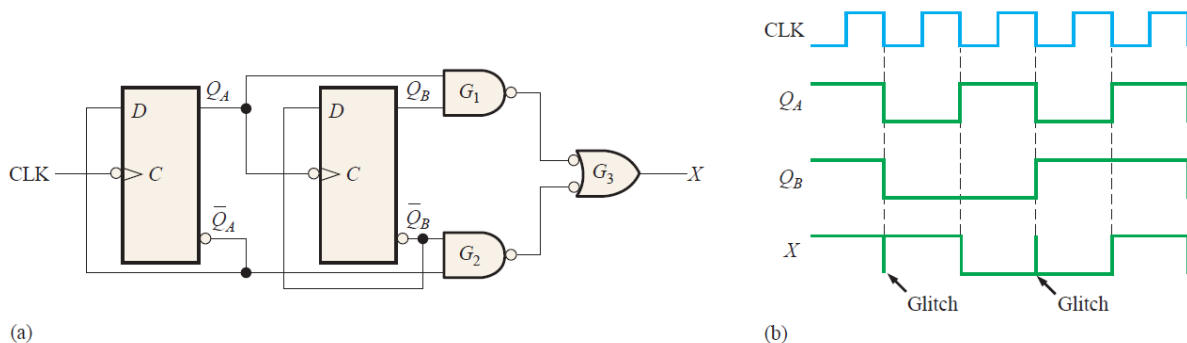
For the circuit in Figure 7–89, determine the maximum frequency of the clock signal for reliable operation if the set-up time for each flip-flop is 3 ns and the propagation delays ( $t_{PLH}$  and  $t_{PHL}$ ) from clock to output are 6 ns for each flip-flop.



**FIGURE 7–89**

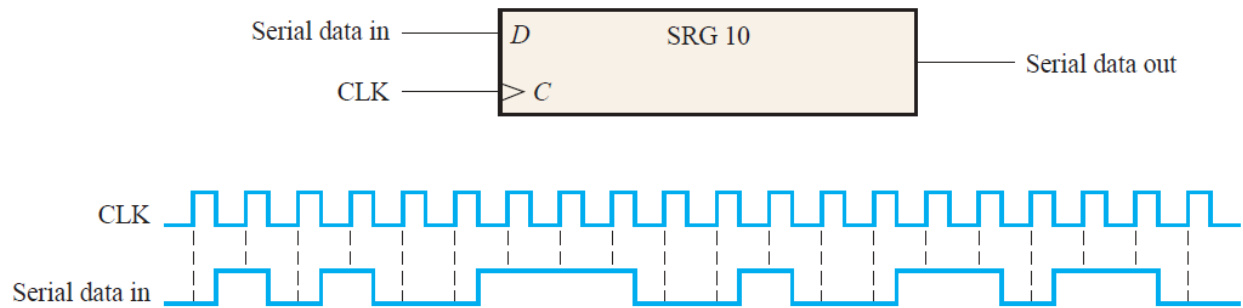
10.

The flip-flop circuit in Figure 7–95(a) is used to generate a binary count sequence. The gates form a decoder that is supposed to produce a HIGH when a binary zero or a binary three state occurs (00 or 11). When you check the  $Q_A$  and  $Q_B$  outputs, you get the display shown in part (b), which reveals glitches on the decoder output ( $X$ ) in addition to the correct pulses. What is causing these glitches, and how can you eliminate them?

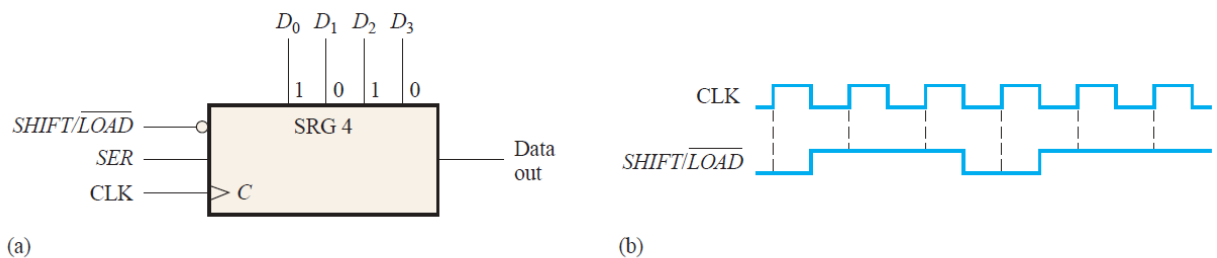


**FIGURE 7–95**

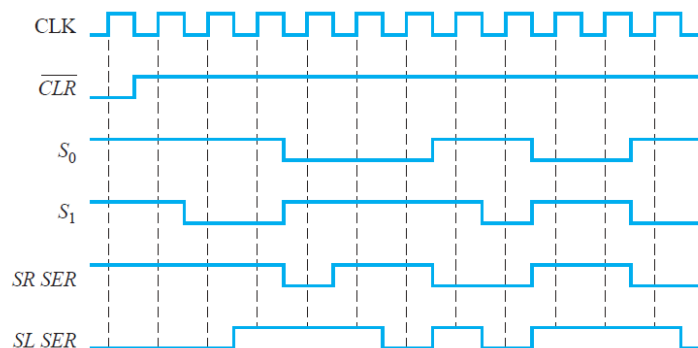
For the serial in/serial out shift register, determine the data-output waveform for the data-input and clock waveforms in Figure 8–50. Assume that the register is initially cleared.



The shift register in Figure 8–54(a) has  $SHIFT/\overline{LOAD}$  and CLK inputs as shown in part (b). The serial data input ( $SER$ ) is a 0. The parallel data inputs are  $D_0 = 1$ ,  $D_1 = 0$ ,  $D_2 = 1$ , and  $D_3 = 0$  as shown. Develop the data-output waveform in relation to the inputs.

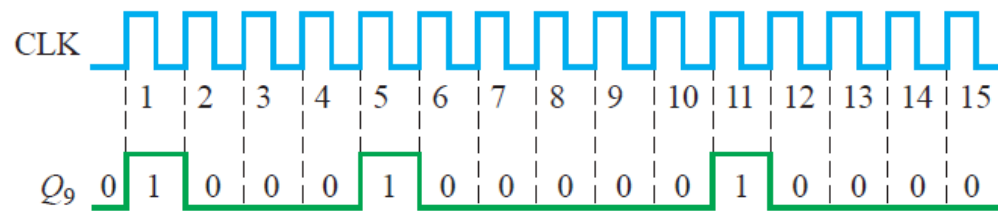


Determine the  $Q$  outputs of a 74HC194 with the inputs shown in Figure 8–59. Inputs  $D_0$ ,  $D_1$ ,  $D_2$ , and  $D_3$  are all HIGH.



14.

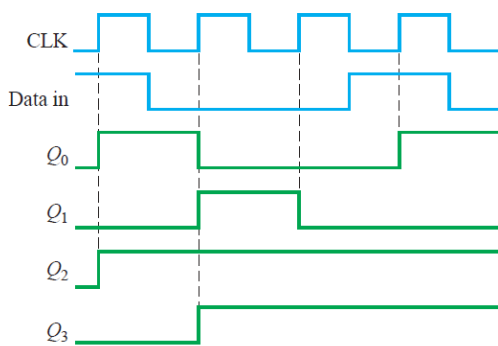
The waveform pattern in Figure 8–61 is required. Devise a ring counter, and indicate how it can be preset to produce this waveform on its  $Q_9$  output. At CLK16 the pattern begins to repeat.



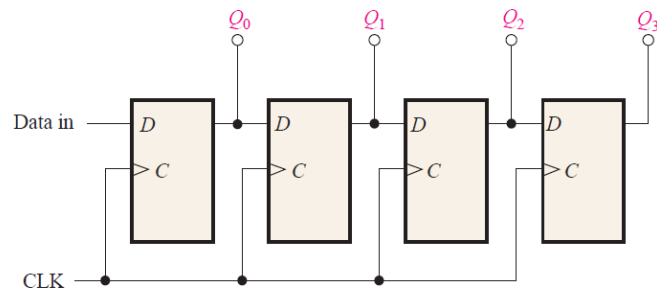
**FIGURE 8-61**

15.

Based on the waveforms in Figure 8–62(a), determine the most likely problem with the register in part (b) of the figure.



(a)



(b)

**FIGURE 8-62**