CUHK(SZ)-EIE2050 Final Exam

1st Semester, 2016-2017

Note:

a. No notes or calculators are allowed in the exam.
b. The exam carries 50% in the total evaluation of the course.
c. Answer all 10 questions within 150 minutes in a separate answer book.

1. (5 points) List the major differences between a latch and a flip-flop.
2. (5 points) List the major differences between read-only memory (ROM) and random-access memory (RAM).
3. (5 points) Use exclusive-OR gates only to implement an even-parity generator for 4-bit input code, which outputs 1 if the number of 1's in the input code is an odd number, and outputs 0 otherwise.
4. (5 points) Simplify the function $X = \bar{A}\bar{B}C + A\bar{C} + ACD + AC\bar{D} + \bar{A}\bar{B}\bar{D}$ as a sum of products with a minimum number of literals. Then implement its logic diagram using NAND gates only.
5. (10 points) Simplify the logic function

$$F(w,x,y,z) = (\overline{y} + w\overline{y}(xz + x\overline{z}))\, z + \overline{x\overline{y} + \overline{\overline{x+y}} + \overline{z}} + y(z + w\overline{x}(\overline{w} + z))$$

   based on logic rules. Show the result as a sum of products with a minimum number of literals. (Note: The intermediate steps are required to be shown.)
6. (10 points) With the following description, design a logic diagram for a gated D latch. *A gated D latch has an EN input, and a D input. When D input is HIGH and EN is HIGH, the latch will set. When D is LOW and EN is HIGH, the latch will reset.*
7. (15 points) Design the logic diagram of a circuit to expand $64K \times 4$ ROMs (ref. Figure 1) to form a $128K \times 8$ ROM.

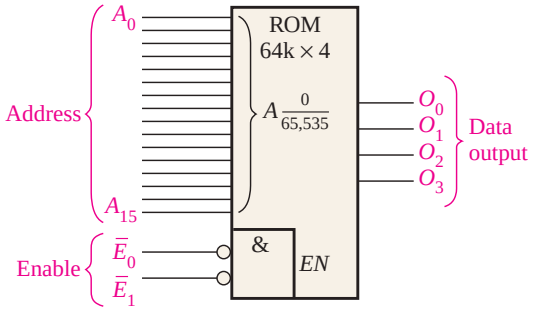

Figure 1: $64K \times 4$ ROM.

8. (15 points) Design the internal logic diagram of a 4-bit parallel in/serial out shift register (ref. Figure 2), by using D flip-flops and AND/OR/NOT gates.

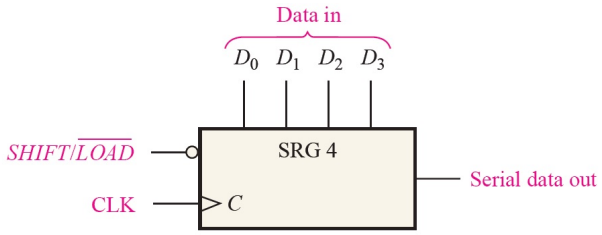

Figure 2: 4-bit parallel in/serial out shift register.

9. (15 points) Design the logic diagram of a full adder with inputs A, B, C_{in} and outputs Σ, C_{out}, by using 4-to-1 multiplexers (ref. Figure 3) and NOT gates.

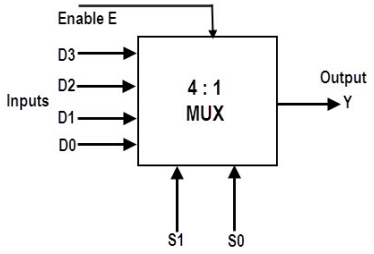

Figure 3: 4-to-1 multiplexer.

10. (15 points) Design the logic diagram of a circuit that has a state diagram as in Figure 4, using two J-K flip-flops and necessary logic gates. (Note: The Karnaugh maps and simplification results are required to be shown explicitly in your answer.)

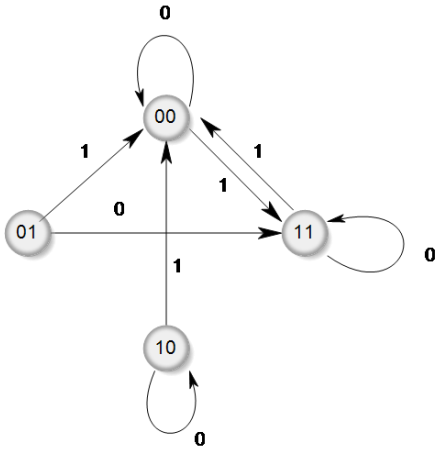

Figure 4: State diagram.