EIE2050 Assignment 3

1.

The circuit shown in Figure 6–71 is a 4-bit circuit that can add or subtract numbers in a form used in computers (positive numbers in true form; negative numbers in complement form). (a) Explain what happens when the $\overline{Add}/Subt.$ input is HIGH. (b) What happens when $\overline{Add}/Subt.$ is LOW?

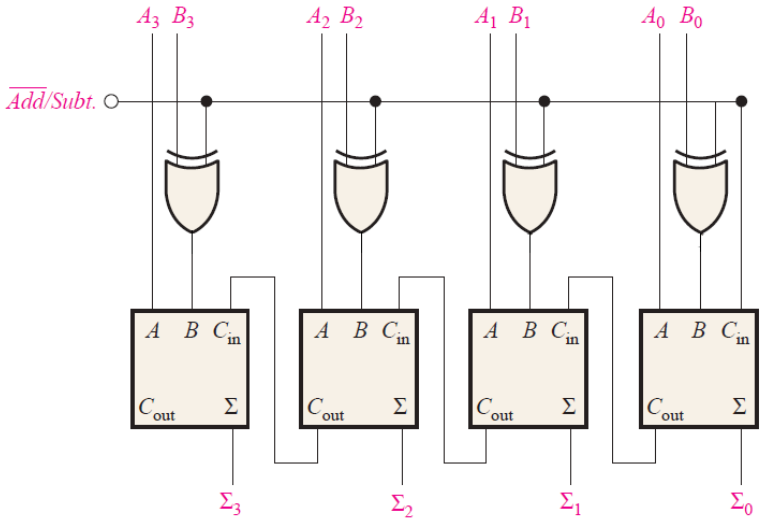


FIGURE 6–71

(a) When the $\overline{Add}/Subt$ is HIGH, the two numbers are subtracted.

(b) When the input is LOW, the numbers are added.

2.

A 7-segment decoder/driver drives the display in Figure 6–78. If the waveforms are applied as indicated, determine the sequence of digits that appears on the display.

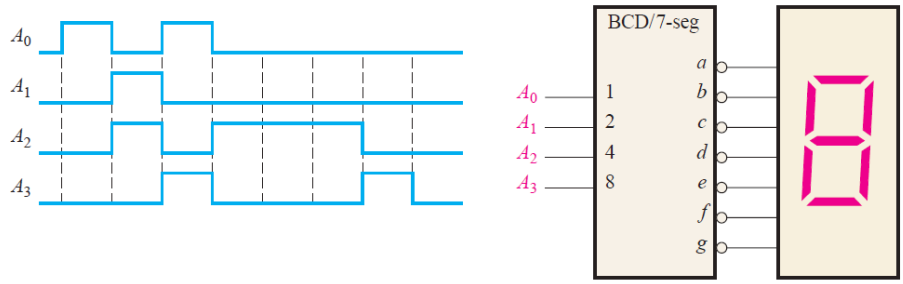


FIGURE 6–78

0 1 6 9 4 4 4 8 0

3.

Show the logic required to convert a 10-bit binary number to Gray code and use that logic to convert the following binary numbers to Gray code:

(a) 1010111100 **(b)** 1111000011 **(c)** 1011110011 **(d)** 1000000001

(a) 1010111100 binary
1111100010 gray

(b) 1111000011 binary
1000100010 gray

(c) 1011110011 binary
1110001010 gray

(d) 1000000001 binary
1100000001 gray

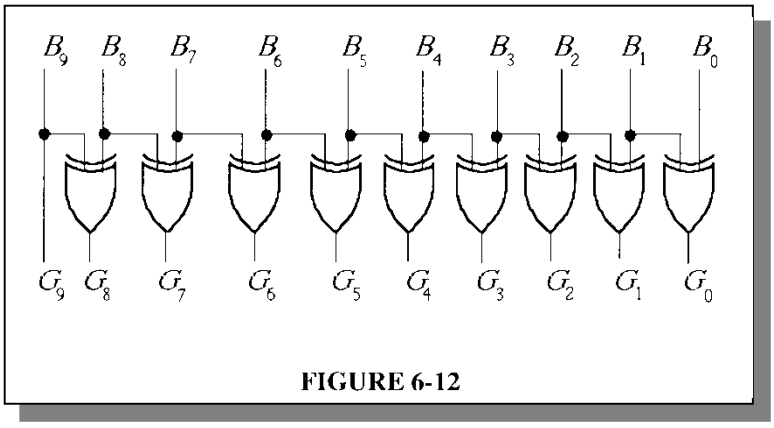


FIGURE 6-12

4.

The waveforms in Figure 6–82 are applied to the 4-bit parity logic. Determine the output waveform in proper relation to the inputs. For how many bit times does even parity occur, and how is it indicated? The timing diagram includes eight bit times.

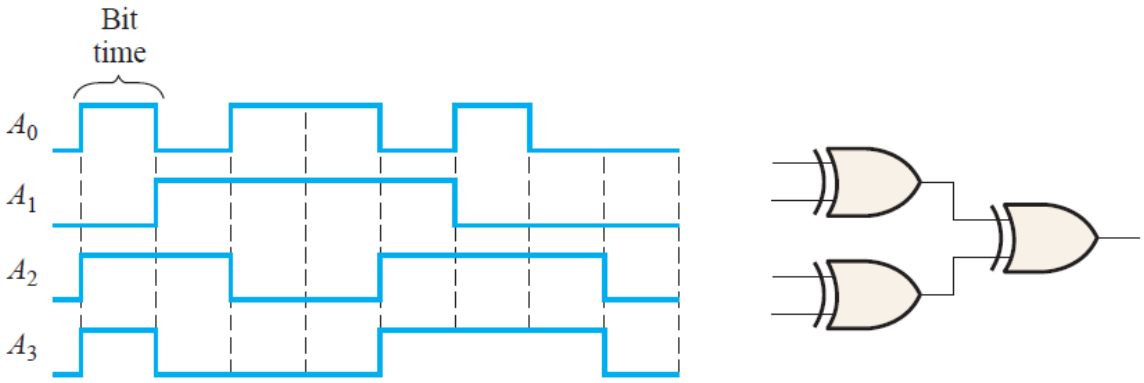


FIGURE 6–82

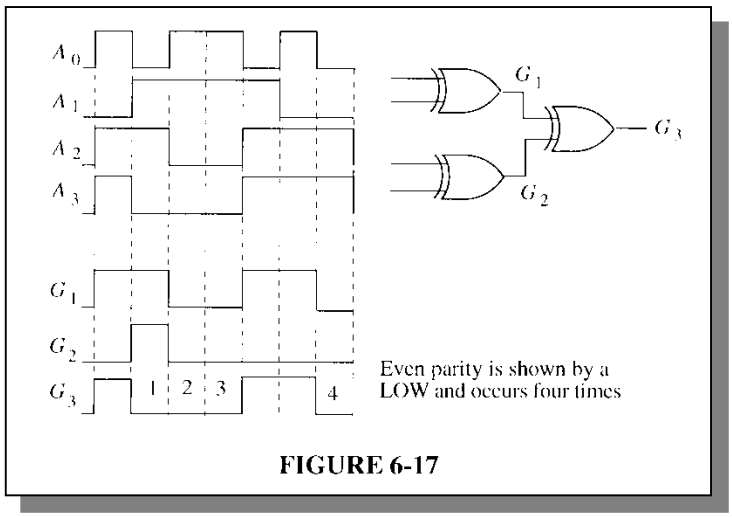


FIGURE 6-17

5.

For a gated S-R latch, determine the Q and $\overline{Q}$ outputs for the inputs in Figure 7–73. Show them in proper relation to the enable input. Assume that Q starts LOW.

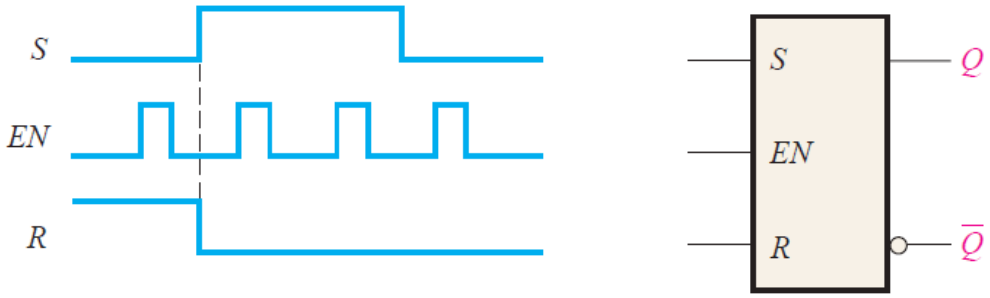


FIGURE 7–73

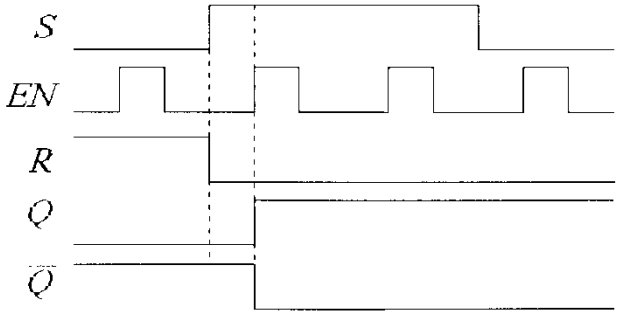


FIGURE 8-4

6.

Two edge-triggered J-K flip-flops are shown in Figure 7–77. If the inputs are as shown, draw the Q output of each flip-flop relative to the clock, and explain the difference between the two. The flip-flops are initially RESET.

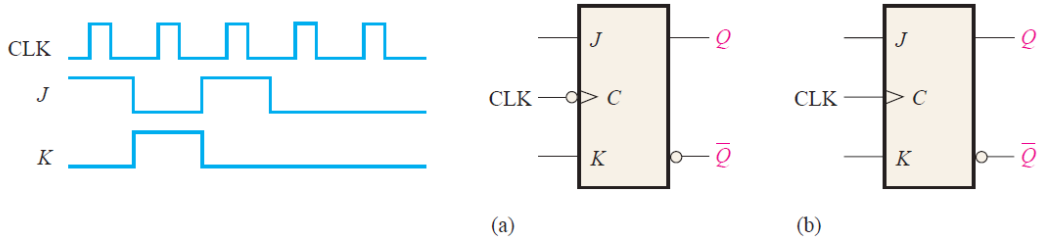
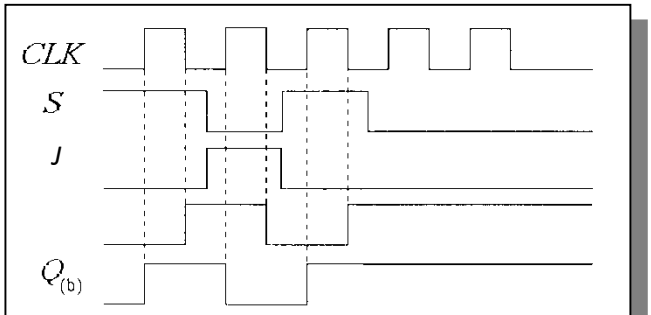


FIGURE 7–77



(a) The flip-flop triggers on the negative edge of the clock pulse

(b) The flip-flop triggers on the positive edge of the clock pulse.

FIGURE 8-8

7.

Determine the Q waveform relative to the clock if the signals shown in Figure 7–83 are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW.

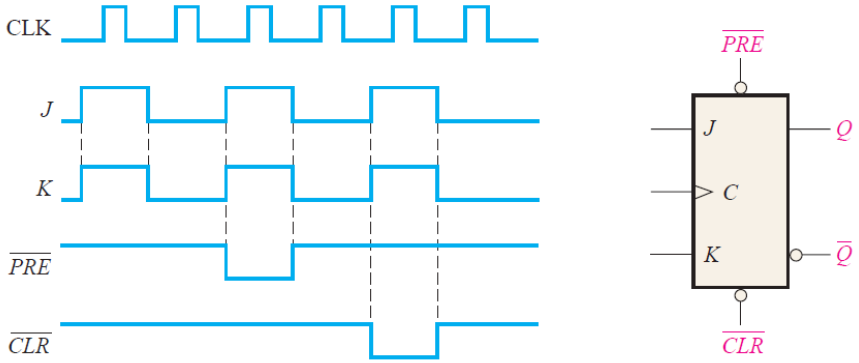


FIGURE 7–83

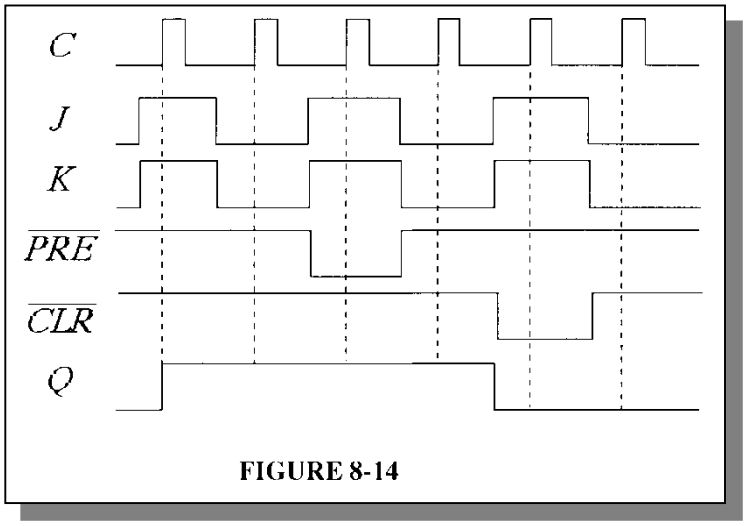


FIGURE 8-14

8.

The flip-flop in Figure 7–88 is initially RESET. Show the relation between Q output and the clock pulse if the propagation delay t_{PLH} (clock to Q) is 5 ns.

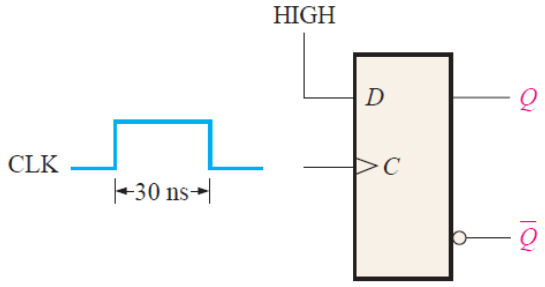
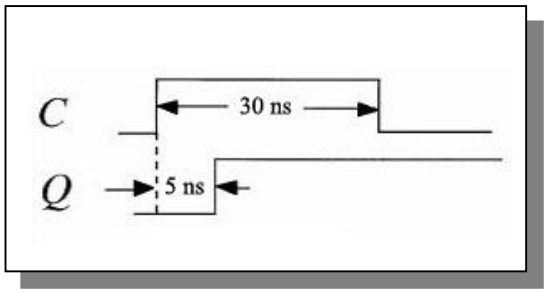


FIGURE 7–88



9.

For the circuit in Figure 7–89, determine the maximum frequency of the clock signal for reliable operation if the set-up time for each flip-flop is 3 ns and the propagation delays (t_{PLH} and t_{PHL}) from clock to output are 6 ns for each flip-flop.

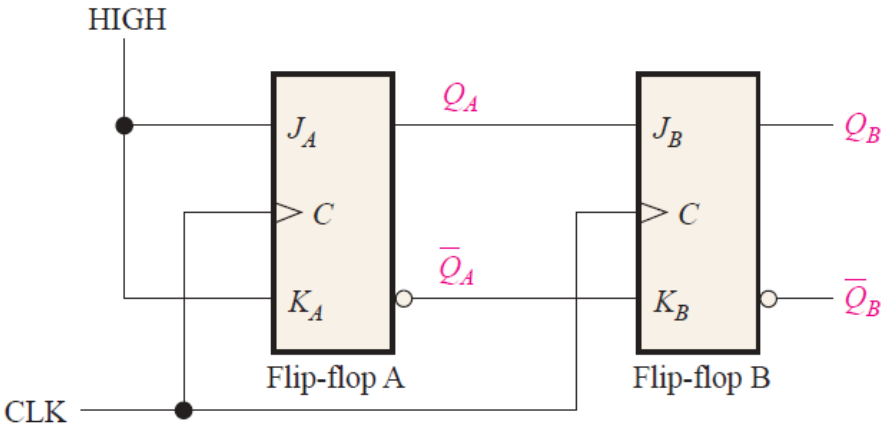


FIGURE 7–89

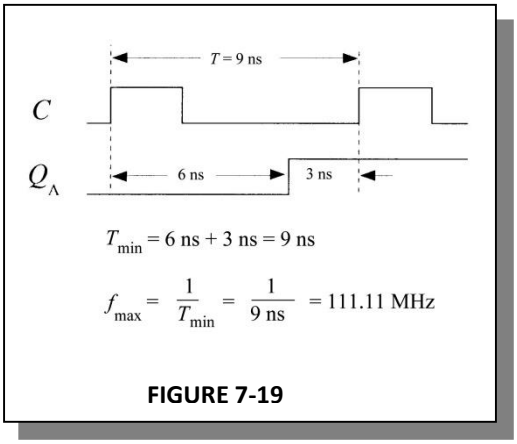


FIGURE 7-19

10.

The flip-flop circuit in Figure 7–95(a) is used to generate a binary count sequence. The gates form a decoder that is supposed to produce a HIGH when a binary zero or a binary three state occurs (00 or 11). When you check the Q_A and Q_B outputs, you get the display shown in part (b), which reveals glitches on the decoder output (X) in addition to the correct pulses. What is causing these glitches, and how can you eliminate them?

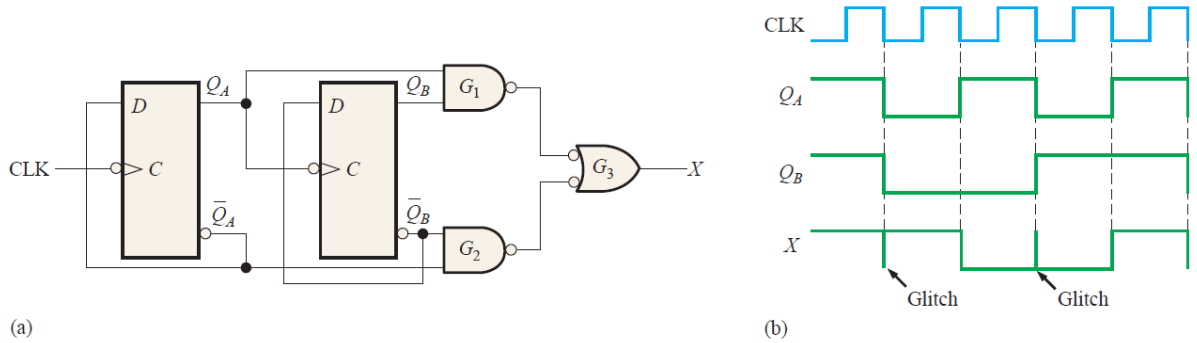


FIGURE 7–95

Small differences in the switching times of flip-flop A and flip-flop B due to propagation delay cause the glitches as shown in the expanded timing diagram. The delays are exaggerated greatly for purposes of illustration. Use synchronous clocking.

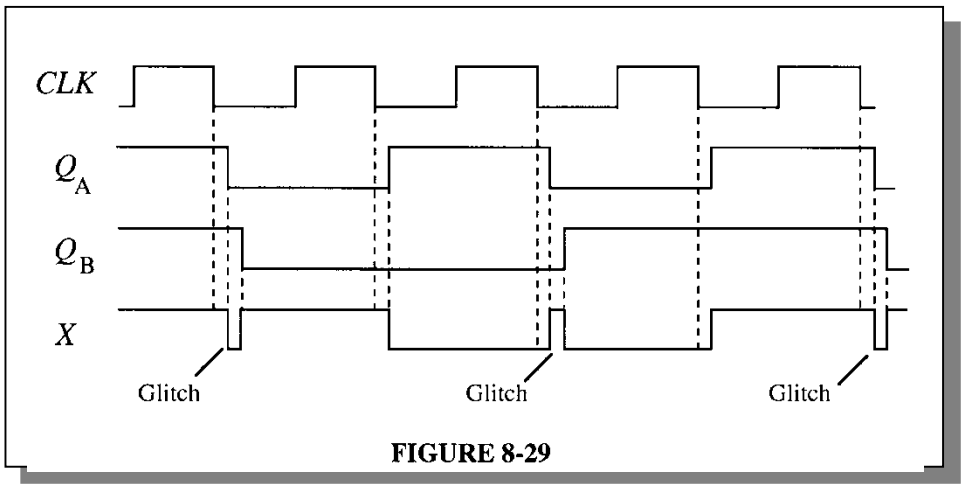
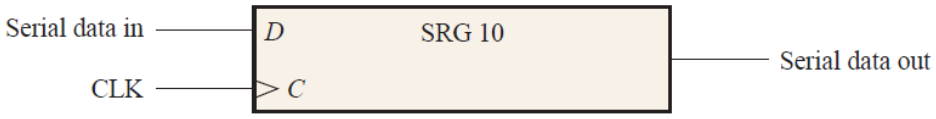


FIGURE 8-29

11.

For the serial in/serial out shift register, determine the data-output waveform for the data-input and clock waveforms in Figure 8–50. Assume that the register is initially cleared.



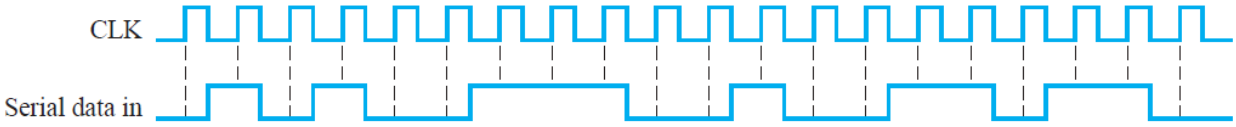


FIGURE 8–50

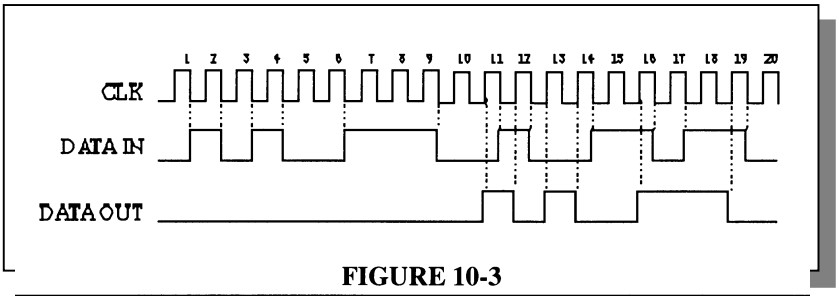


FIGURE 10-3

12.

The shift register in Figure 8–54(a) has $SHIFT/\overline{LOAD}$ and CLK inputs as shown in part (b). The serial data input (SER) is a 0. The parallel data inputs are $D_0 = 1$, $D_1 = 0$, $D_2 = 1$, and $D_3 = 0$ as shown. Develop the data-output waveform in relation to the inputs.

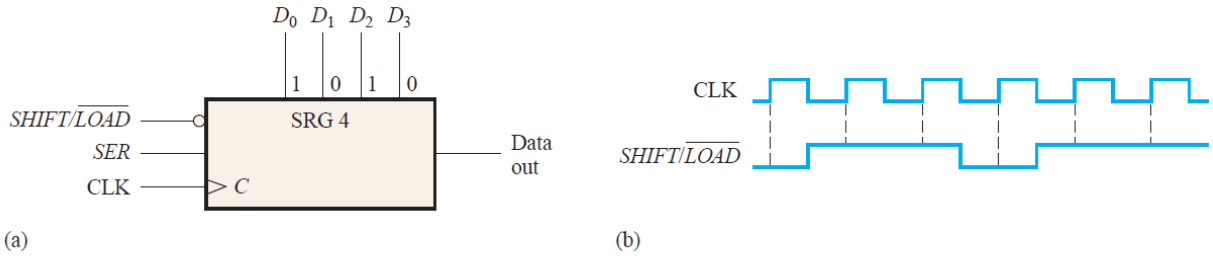


FIGURE 8–54

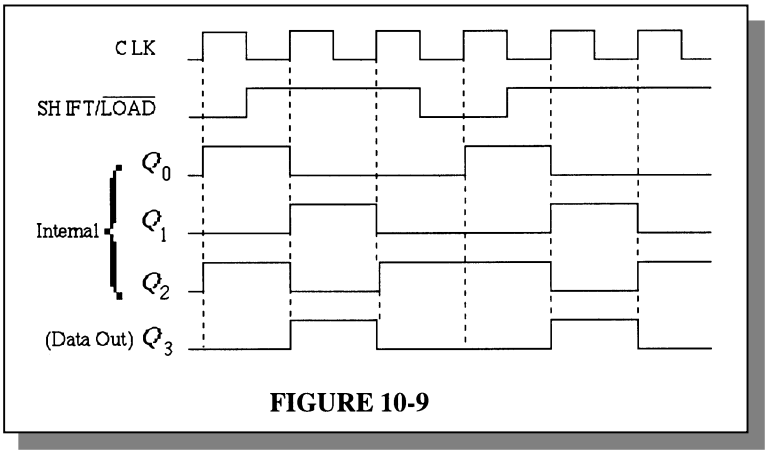


FIGURE 10-9

13.

Determine the Q outputs of a 74HC194 with the inputs shown in Figure 8–59. Inputs D_0, D_1, D_2, and D_3 are all HIGH.

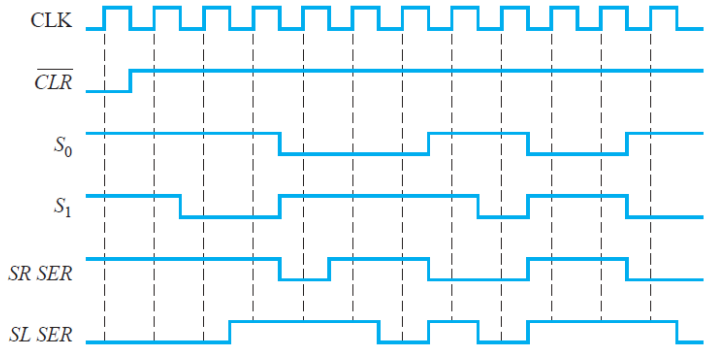


FIGURE 8–59

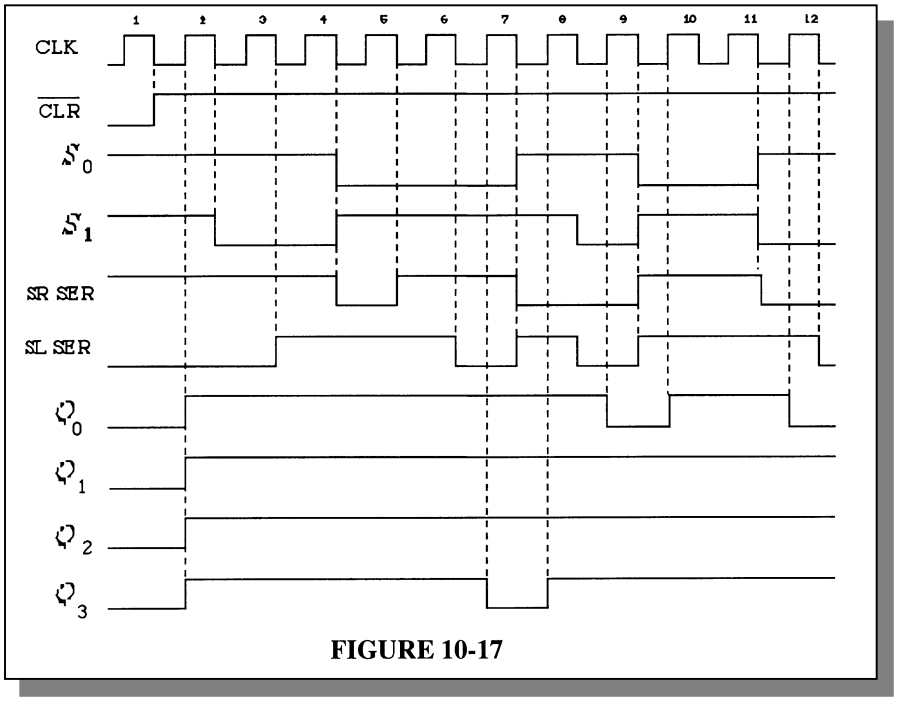


FIGURE 10-17

14.

The waveform pattern in Figure 8–61 is required. Devise a ring counter, and indicate how it can be preset to produce this waveform on its Q_9 output. At CLK16 the pattern begins to repeat.

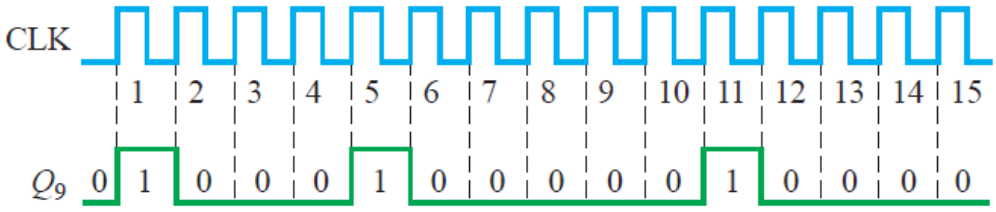


FIGURE 8–61

A 15-bit ring counter with stages **3**, **7**, and **12** SET and the remaining stages RESET.

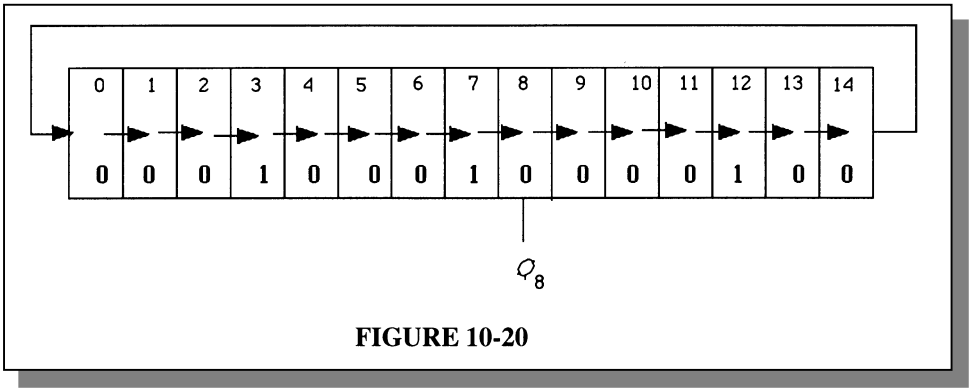


FIGURE 10-20

15.

Based on the waveforms in Figure 8–62(a), determine the most likely problem with the register in part (b) of the figure.

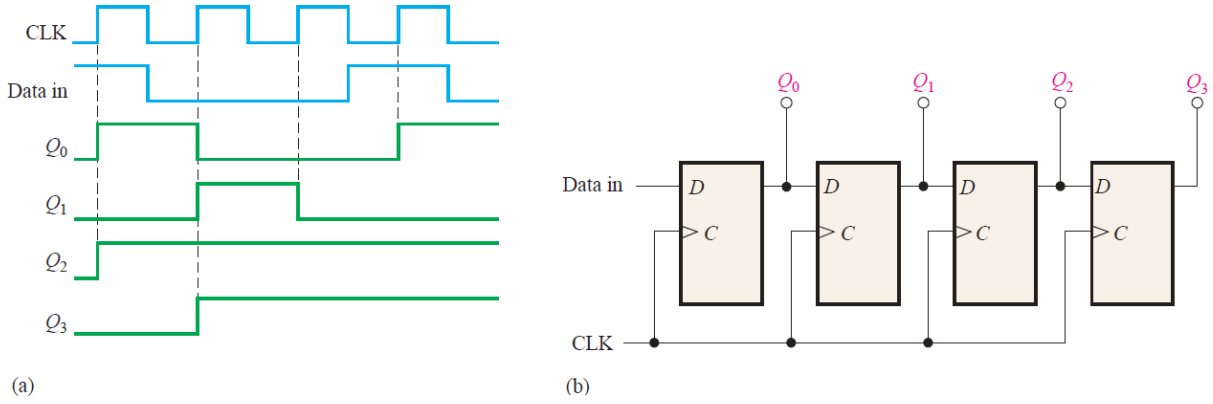


FIGURE 8–62

Q_2 goes HIGH on the first clock pulse indicating that the *D* input is open.

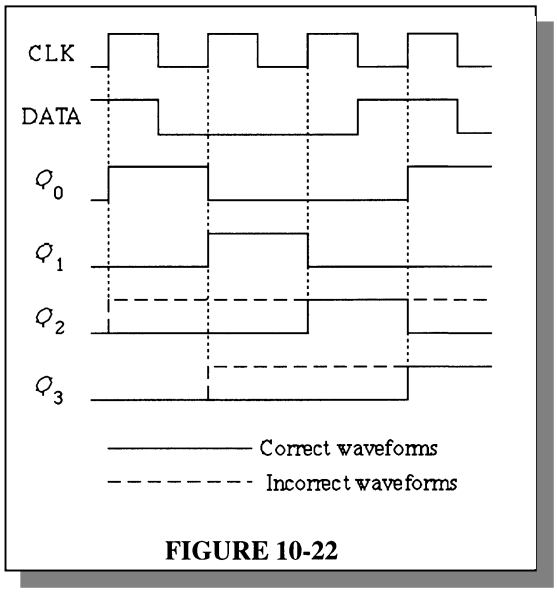


FIGURE 10-22