# CUHK(SZ)-EIE2050 Final Exam

2nd Semester, 2016-2017

**Note:**

a. No notes or calculators are allowed in the exam.
b. The exam carries 50% in the total evaluation of the course.
c. Answer all 10 questions within 150 minutes in a separate answer book.

1. (5 points) What are the *Universal Gates*?

2. (5 points) List the typical *Memory Hierarchy*.

3. (10 points) Draw the logic diagram of a full adder circuit by using a 3-to-8 decoder (ref. Figure 1) and OR gates.

4. (10 points) Simplify the logic function

$$f(A,B,C,D,E) = (AB + C + D)\left(\overline{C} + D\right)\left(\overline{C} + D + E\right)$$

   to obtain the minimized form as sum of products based on logic rules. (Note: The intermediate steps are required to be shown.)

5. (10 points) Draw the logic diagram of a D flip-flop (ref. Figure 2) with active-LOW PRESET and CLEAR inputs. (Note: the internal logic of the pulse transition detector does NOT need to be shown.)

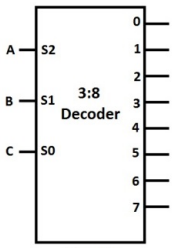


Figure 1: 3-to-8 decoder.

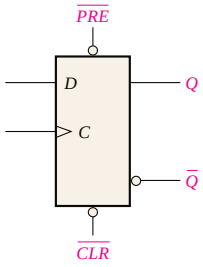


Figure 2: D flip-flop.

6. (10 points) Read the VHDL program in Figure 3, and
   1). Draw the corresponding logic diagram (5 points);
   2). Explain the function of the program briefly (5 points).

```vhdl
library ieee;
    use ieee.std_logic_1164.all;

entity parity_using_assign is
    port (
        data_in     :in  std_logic_vector (7 downto 0);
        parity_out  :out std_logic
    );
end entity;

architecture rtl of parity_using_assign is
begin
    parity_out <= (data_in(0) xor data_in(1)) xor
                  (data_in(2) xor data_in(3)) xor
                  (data_in(4) xor data_in(5)) xor
                  (data_in(6) xor data_in(7));
end architecture;
```

Figure 3: VHDL program.

7. (10 points) *A multiplexer is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination.* Design the internal logic diagram for a multiplexer (ref. Figure 4).

8. (10 points) Design a magnitude comparator circuit for 2-bit binary numbers $A = A_1A_0$ and $B = B_1B_0$. The outputs are $F$, $G$ and $H$, where $F$ is 1 if $A > B$, $G$ is 1 if $A = B$, and $H$ is 1 if $A < B$. Draw the logic diagram.

9. (15 points) Design a combinational circuit that takes as input an unsigned 2-bit number, $X = X_1X_0$, and outputs the square of the number, $Y = X^2$. You need to:
   1). Show the truth table (5 points);
   2). Determine the minimized output functions (5 points);
   3). Draw the logical diagram (5 points).

10. (15 points) Based on the state diagram shown in Figure 5, design the logic diagram of a 3-bit Gray code counter, using J-K flip-flops and AND/OR/NOT gates.

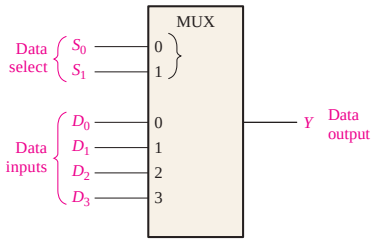


Figure 4: Multiplexer.

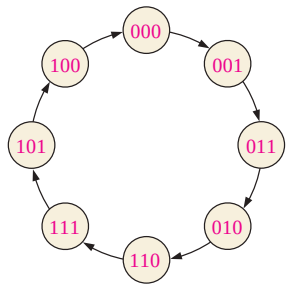


Figure 5: Gray counter.