EIE2050 Assignment 4

Answer the questions and submit to TC fifth floor **before 5:30pm, 12th December.**

Note: 1. There are 10 questions.
2. A zero mark will be given if any plagiarism is found.

1.

For the ripple counter in Figure 9–66, show the complete timing diagram for sixteen clock pulses. Show the clock, Q_0, Q_1, and Q_2 waveforms.

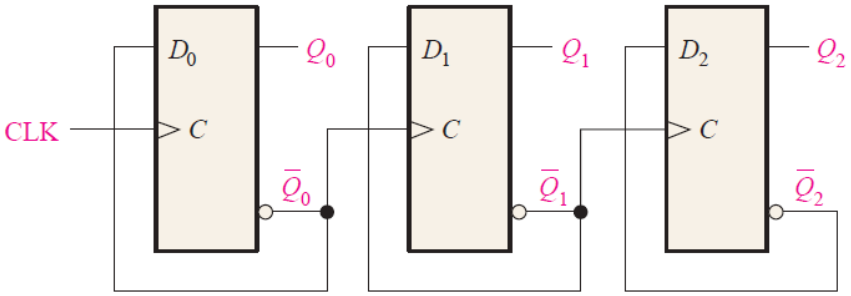

FIGURE 9–66

2.

Show the complete timing diagram for the 5-stage synchronous binary counter in Figure 9–67. Verify that the waveforms of the Q outputs represent the proper binary number after each clock pulse.

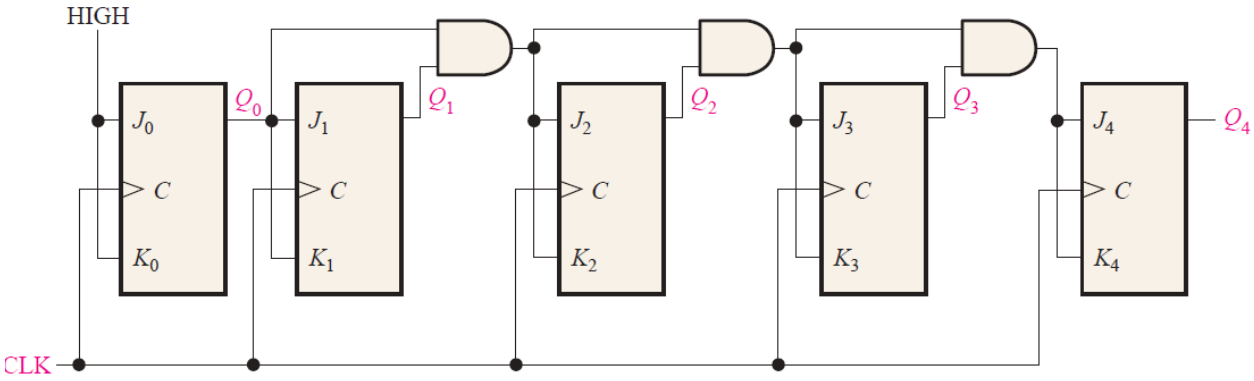

FIGURE 9–67

3.

Design a counter to produce the following sequence. Use J-K flip-flops.

00, 10, 01, 11, 00, . . .

4.

Design a counter to produce the following binary sequence. Use J-K flip-flops.

0, 9, 1, 8, 2, 7, 3, 6, 4, 5, 0, . . .

5.

For the 4-bit binary counter connected to the decoder in Figure 9–77, determine each of the decoder output waveforms in relation to the clock pulses.

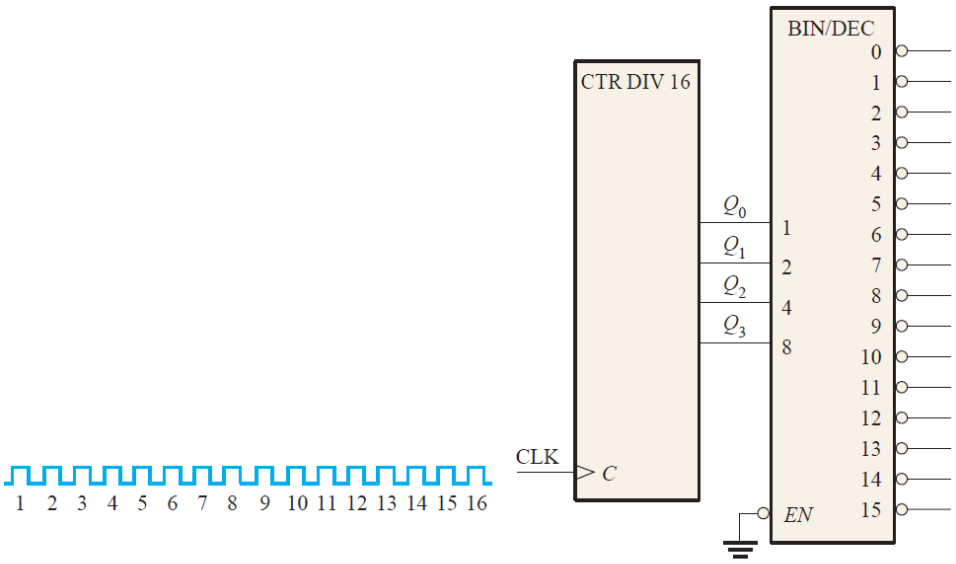

FIGURE 9–77

6.

Show how the PAL-type array in Figure 10–64 should be programmed to implement each of the following SOP expressions. Use an X to indicate a connected link.

(a) $Y = A\overline{B}C + \overline{A}B\overline{C} + ABC$

(b) $Y = A\overline{B}C + \overline{A}\,\overline{B}C + \overline{A}BC$

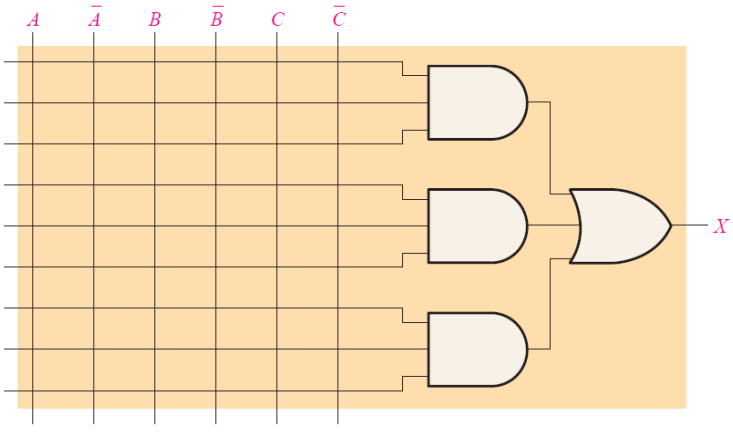

FIGURE 10–64

7.

Modify the array in Figure 10–67 to produce an output $X = \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + ABC + A\overline{B}C$

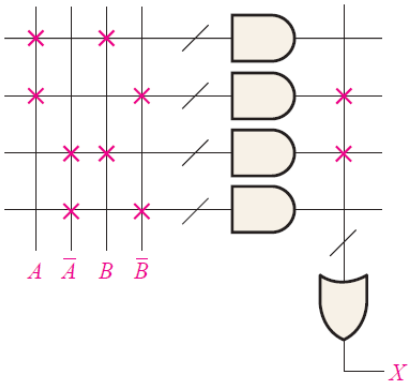

FIGURE 10–67

8.

Write a VHDL program for the logic described by the following Boolean expression.

$$X = \bar{A}B\bar{C} + ABC + \bar{B}\bar{C}$$

9.

Draw a basic logic diagram for a 512 × 4-bit static RAM, showing all the inputs and outputs.

10.

Using a block diagram, show how 64k × 1 dynamic RAMs can be expanded to build a 256k × 4 RAM.