EIE2050 Assignment 4

1.

For the ripple counter in Figure 9–66, show the complete timing diagram for sixteen clock pulses. Show the clock, Q_0, Q_1, and Q_2 waveforms.

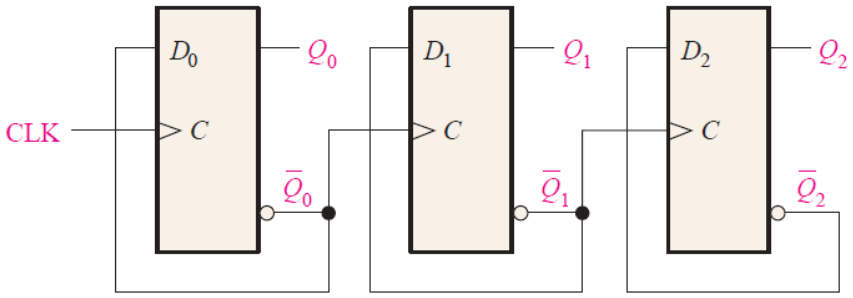


FIGURE 9–66

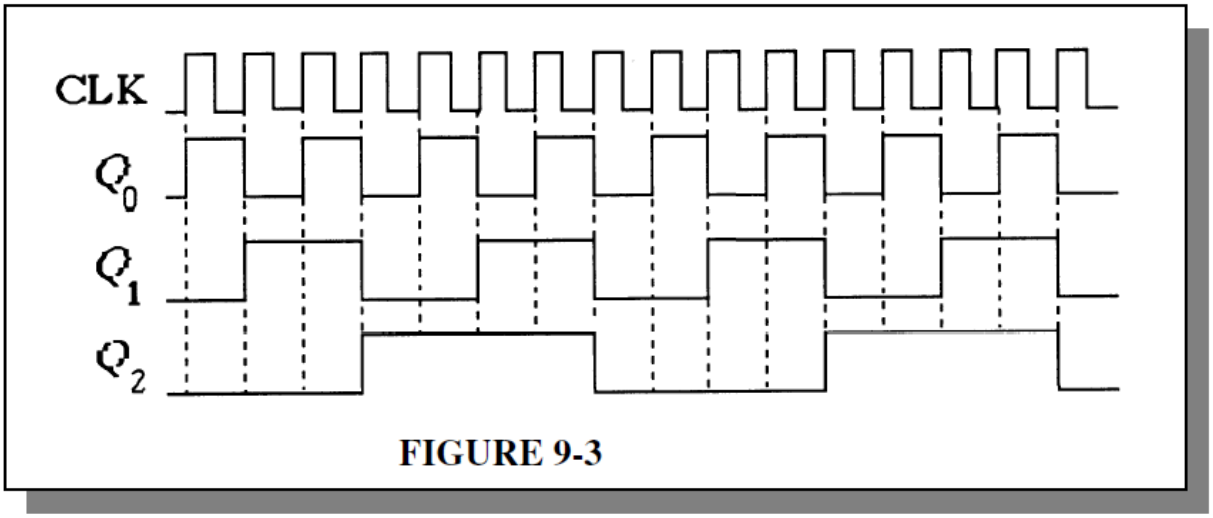


FIGURE 9-3

2.

Show the complete timing diagram for the 5-stage synchronous binary counter in Figure 9–67. Verify that the waveforms of the Q outputs represent the proper binary number after each clock pulse.

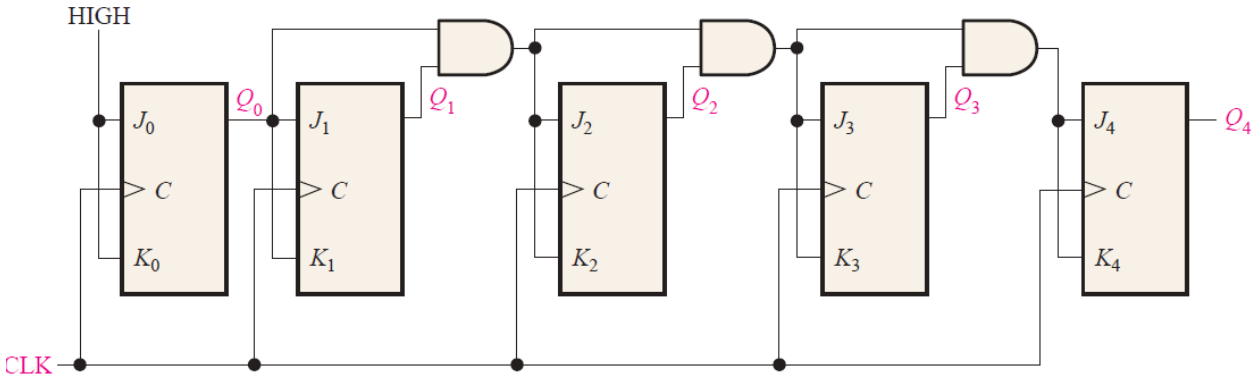


FIGURE 9–67

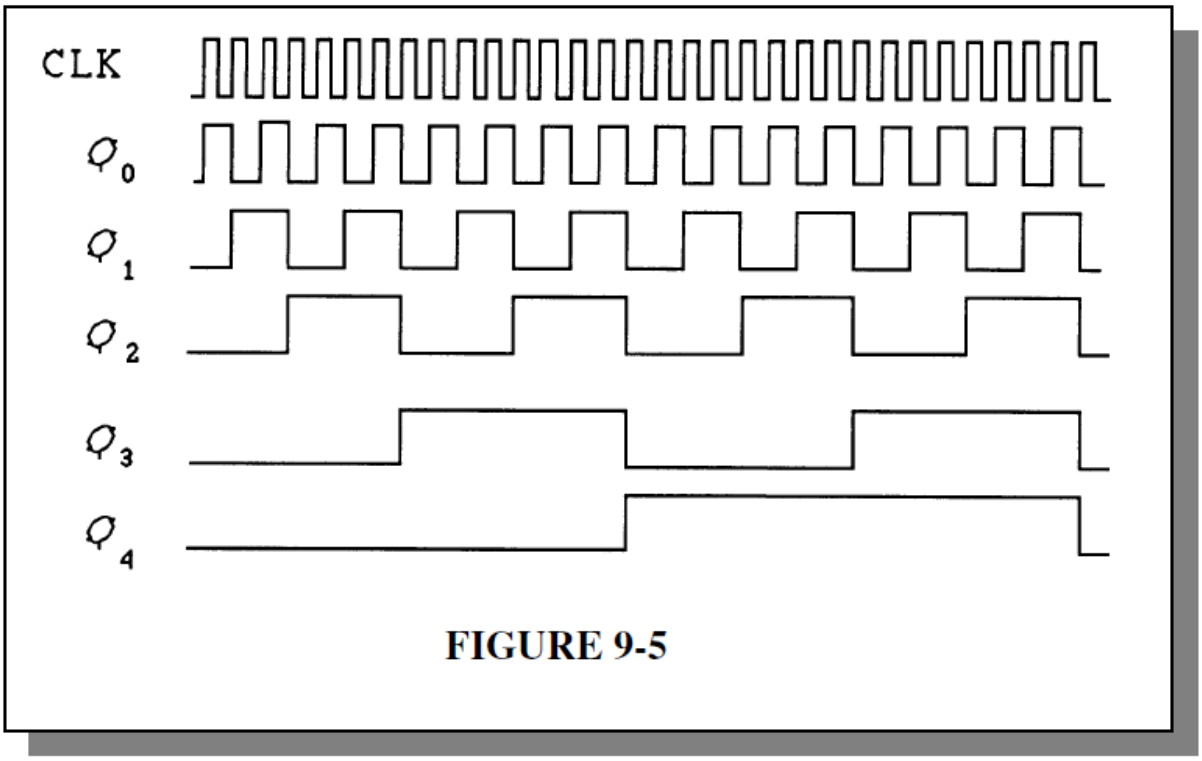


FIGURE 9-5

3.

Design a counter to produce the following sequence. Use J-K flip-flops.

00, 10, 01, 11, 00, . . .

NEXT-STATE TABLE

Present State		**Next State**	
Q_1	Q_0	Q_1	Q_0
0	0	1	0
1	0	0	1
0	1	1	1
1	1	0	0

TRANSITION TABLE

Output State Transitions (Present state to next state)		**Flip-Flop Inputs**			
Q_1	Q_0	J_1	K_1	J_0	K_0
0 to 1	0 to 0	1	X	0	X
1 to 0	0 to 1	X	1	1	X
0 to 1	1 to 1	1	X	X	0
1 to 0	1 to 0	X	1	X	1

See Figure 9-14.

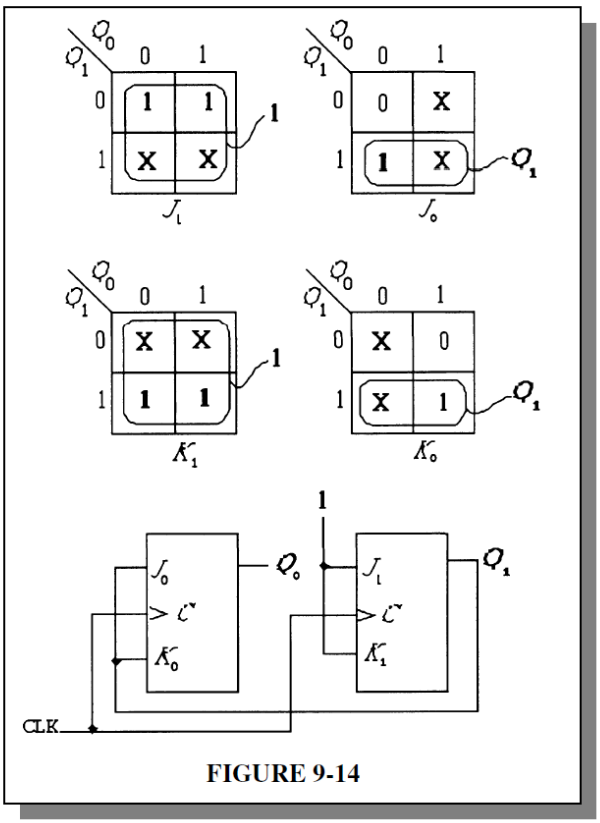


FIGURE 9-14

4.

Design a counter to produce the following binary sequence. Use J-K flip-flops.

0, 9, 1, 8, 2, 7, 3, 6, 4, 5, 0, . . .

NEXT-STATE TABLE

Present State				Next State			
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	1	0	0	1
1	0	0	1	0	0	0	1
0	0	0	1	1	0	0	0
1	0	0	0	0	0	1	0
0	0	1	0	0	1	1	1
0	1	1	1	0	0	1	1
0	0	1	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	0	0	0

TRANSITION TABLE

Output State Transition (Present State to next state)				Flip-flop Inputs							
Q_3	Q_2	Q_1	Q_0	J_3	K_3	J_2	K_2	J_1	K_1	J_0	K_0
0 to 1	0 to 0	0 to 0	0 to 1	1	X	0	X	0	X	1	X
1 to 0	0 to 0	0 to 0	0 to 1	X	1	0	X	0	X	X	0
0 to 1	0 to 0	0 to 0	1 to 0	1	X	0	X	0	X	X	1
1 to 0	0 to 0	0 to 1	0 to 0	X	1	0	X	1	X	0	X
0 to 0	0 to 1	1 to 1	0 to 1	0	X	1	X	X	0	1	X
0 to 0	1 to 0	1 to 1	1 to 1	0	X	X	1	X	0	X	0
0 to 0	0 to 1	1 to 1	1 to 0	0	X	1	X	X	0	X	1
0 to 0	1 to 1	1 to 0	0 to 0	0	X	X	0	X	1	0	X
0 to 0	1 to 1	0 to 0	0 to 1	0	X	X	0	0	X	1	X
0 to 0	1 to 0	0 to 0	1 to 0	0	X	X	1	0	X	X	1

Binary states for 10, 11, 12, 13, 14, and 15 are unallowed and can be represented by don't cares. See Figure 9-16. Counter implementation is straightforward from input expressions.

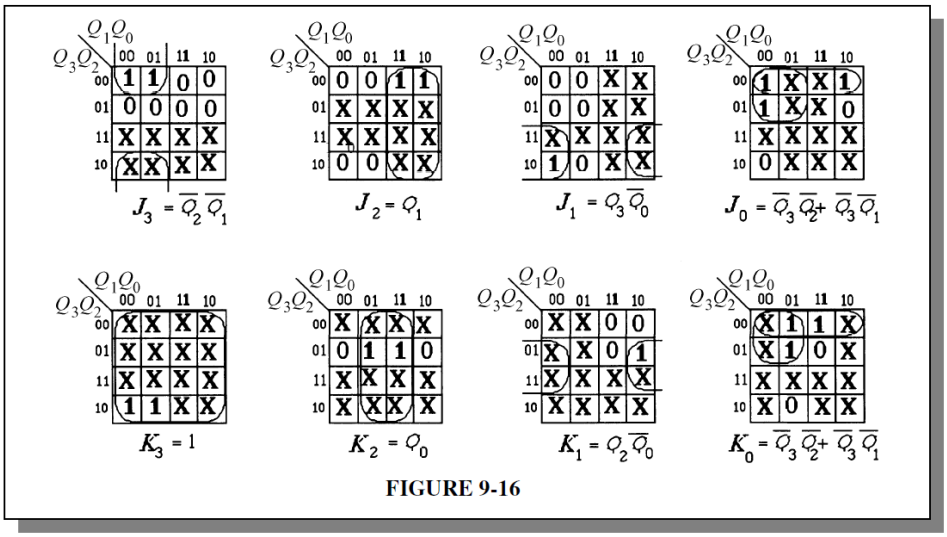


FIGURE 9-16

5.

For the 4-bit binary counter connected to the decoder in Figure 9–77, determine each of the decoder output waveforms in relation to the clock pulses.

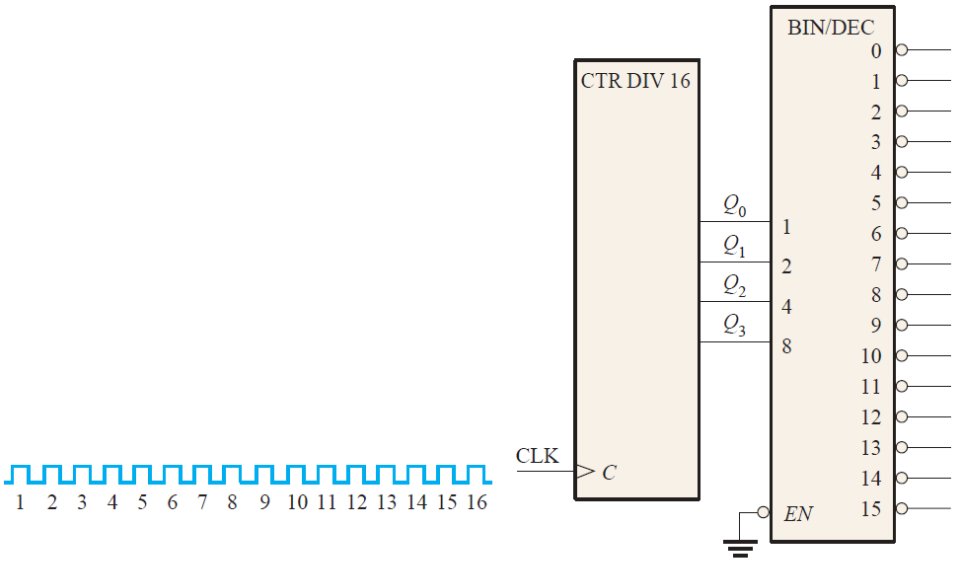


FIGURE 9–77

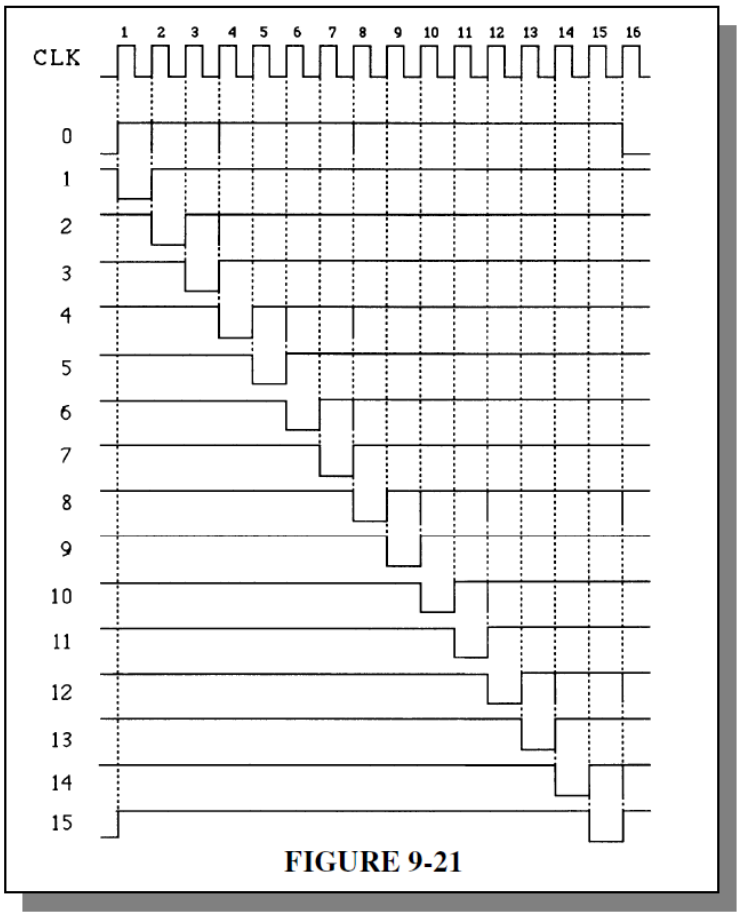


FIGURE 9-21

6.

Show how the PAL-type array in Figure 10–64 should be programmed to implement each of the following SOP expressions. Use an X to indicate a connected link.

(a) $Y = A\overline{B}C + \overline{A}B\overline{C} + ABC$

(b) $Y = A\overline{B}C + \overline{A}\,\overline{B}C + \overline{A}BC$

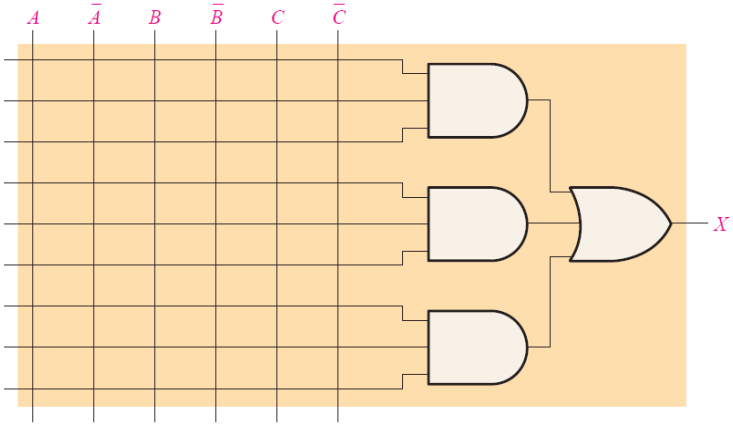
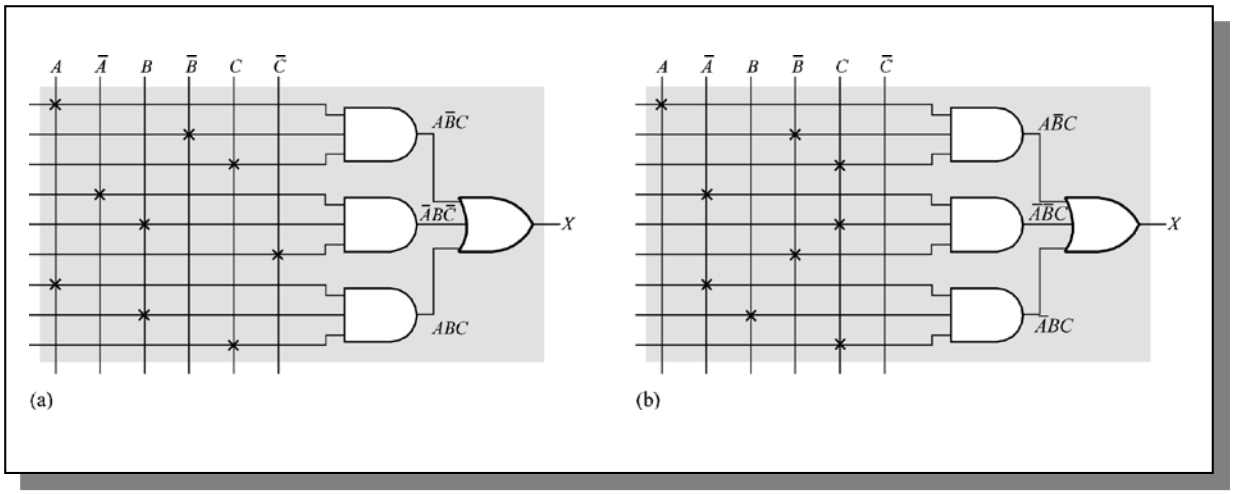


FIGURE 10–64



7.

Modify the array in Figure 10–67 to produce an output $X = \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + ABC + A\overline{B}C$

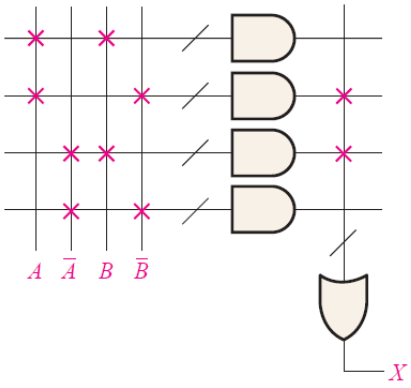


FIGURE 10–67

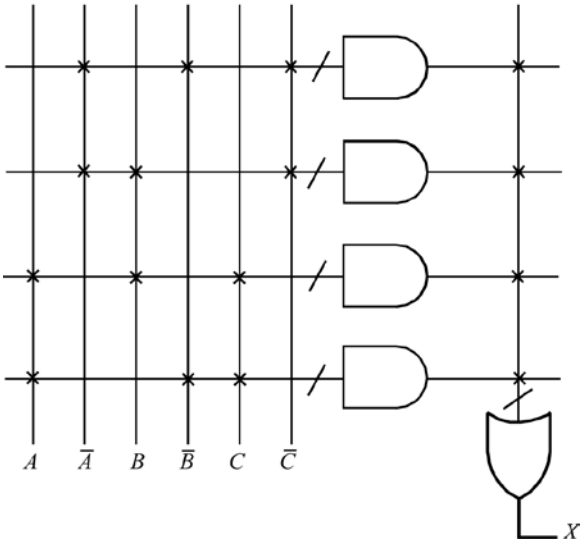


FIGURE 10-4

8.

Write a VHDL program for the logic described by the following Boolean expression.

$$X = \bar{A}B\bar{C} + ABC + \bar{B}\bar{C}$$

Omitted.

9.

Draw a basic logic diagram for a 512 × 4-bit static RAM, showing all the inputs and outputs.

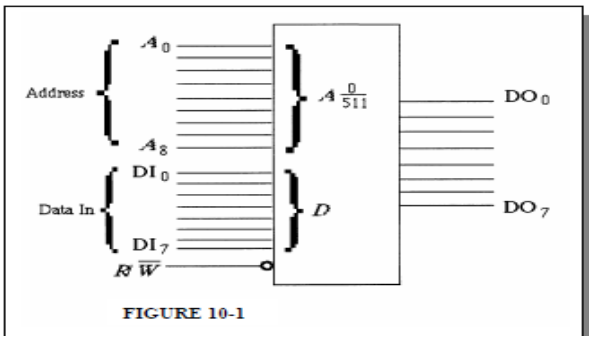


FIGURE 10-1

10.

Using a block diagram, show how 64k × 1 dynamic RAMs can be expanded to build a 256k × 4 RAM.

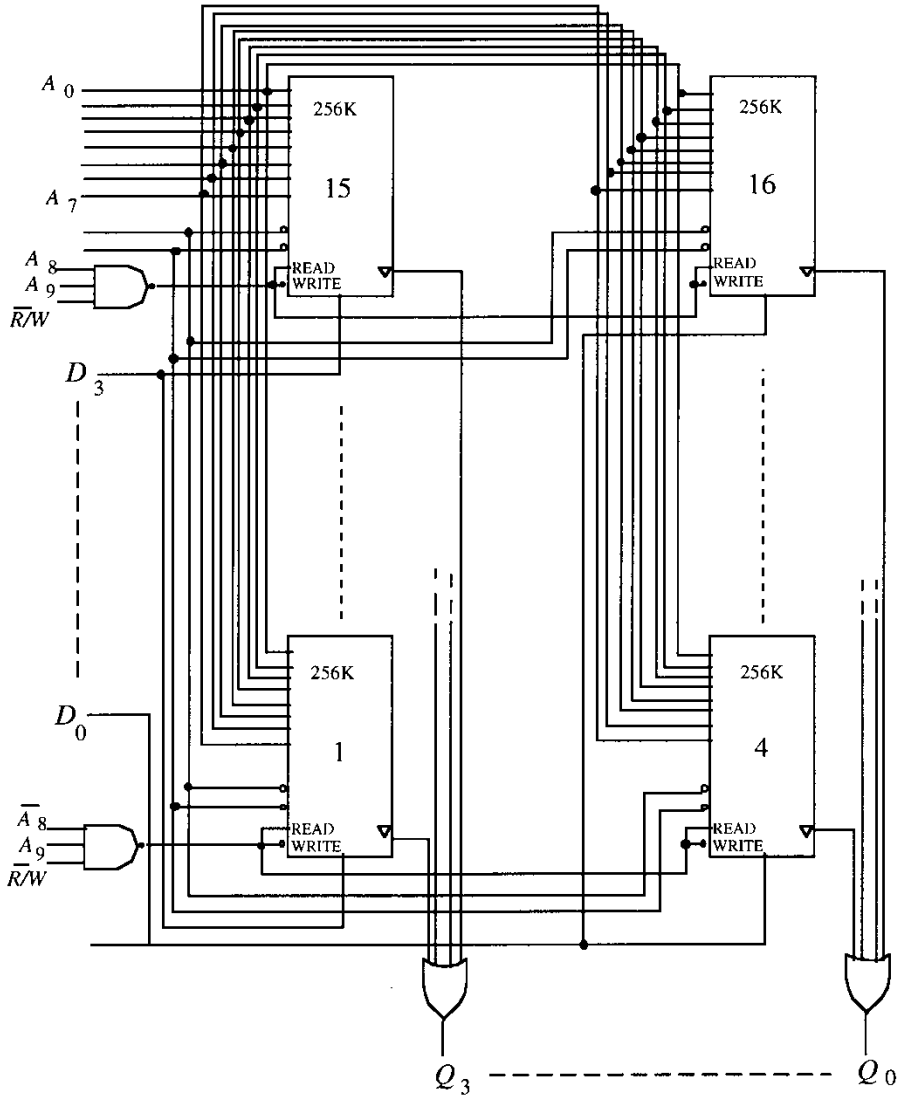


FIGURE 12-5