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From fundamentals to frontiers: a review of memristor mechanisms, modeling and emerging applications

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The escalating demand for artificial intelligence (AI), the internet of things (IoTs), and energy-efficient high-volume data processing has brought the need for innovative solutions to the forefront. The rapid automation surge, while transformative, has unveiled challenges due to processing capacity limitations in this digital age. A promising remedy lies in memristors, offering the potential to transcend the memory and power barriers inherent in the traditional von Neumann architecture, rooted in complementary metal oxide semiconductor (CMOS) devices. This review navigates the intricate landscape of memristors, elucidating their diverse mechanisms that diverge across materials and device architectures. In this review, we discuss all the fundamental processes, such as ion migration, charge trapping/de-trapping, and phase transition that underlies the switching behavior of memristor devices and analytical modelling. Unlocking a realm of possibilities, these mechanisms-based devices hold the promise of revolutionizing diverse sectors. From nociceptors to neural networks, photonic memristors to bio-voltage applications, the versatility of memristors is profound. Culminating the discourse, we survey the progress, anticipate challenges, and illuminate forthcoming prospects in the expansive domain of memristor-based applications.

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1. Introduction

The rapid development of complementary metal-oxide semiconductor (CMOS) technology over the past few decades has revolutionized electronics. Moore's law, which states that the number of transistors on a chip doubles every two years, has been a major driver of this advancement.¹ However, as CMOS scaling approaches fundamental physical constraints, it is becoming increasingly difficult to continue improving computing performance using this technology.² To address the memory bottleneck of the von Neumann architecture, much research has been done to create resistive switching devices for in-memory computing (IMC) applications. These designs share the fundamental idea of co-locating memory and processing with biological systems, where neurons integrate input signals and then create output signals that are sent to downstream neurons *via* comparable synaptic connections.^{3,4} Given the substantial demand for matrix–vector multiplications within artificial neural

network (ANN)-driven data processing for artificial intelligence (AI), IMC has garnered considerable attention as a pivotal technology for the advancement of AI accelerators. Such an architecture can support both conventional machine-learning algorithms and spiking neural networks (SNNs), where computation can be carried out in the same location as the data storage and online or offline learning can be implemented using the conductance modulation and non-volatility properties of memristive devices.

Memristors are passive two-terminal devices that exhibit reversible resistance modulation through changes in their internal material composition under external stimuli. Firstly, we briefly discuss the fundamentals of memristors and different types of resistive switching mechanisms which are classified as: ion migration, phase transition and charge migration. In addition to redox-based resistive switching memory, also known as resistive random-access memory (ReRAM), several other types of devices have been proposed to exhibit a “memristive” property. These include two-terminal devices (such as magnetic tunnel junctions and phase-change memory) and three-terminal devices (such as memtransistors, ferroelectric transistors, and ion-intercalation resistors). Memristors are emerging technologies that combine computational and memory operations in a single unit cell.^{5,6} This makes them a promising alternative to traditional CMOS-based computing architectures, which suffer from the high energy costs of data transfer between processing units and memory units. Among the various switching

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mechanisms that have gained prominence in the field of neuromorphic electronics, memristors stand out due to their compelling attributes of superior electrical performance and extensive scalability. A foundational characteristic of memristive devices lies in their capacity to serve as essential components of crossbar arrays for computational purposes.⁷

This is particularly noteworthy as crossbar arrays, as indicated by Kirchhoff's and Ohm's laws, inherently possess the capability for matrix–vector multiplication (MVM), also referred to as compute-in-memory (CIM) operations. The conventional von Neumann computing architecture has long grappled with energy-intensive data transfers between processing and memory units, whereas CIM holds the promise of revolutionizing computational efficiency through massively parallel processing. Beyond the device-level demonstrations, practical applications will necessitate a careful analysis of the nonidealities in the devices and circuits used such as stochastic switching behaviour, a limited on/off ratio, spike-dependant conductivity, threshold voltage and device variabilities.

In this review article, we explore potential and difficulties for future research while exhaustively highlighting current developments in diverse memristor's applications. Firstly, we briefly discuss fundamentals of memristors and different types of resistive switching mechanisms which are classified as: ion migration, phase transition and charge migration. Furthermore, current conduction mechanisms and analytic modelling of memristors are reviewed. We examine fundamentals of different forms of memristive devices such as nociceptors, artificial neurons, artificial synapses, neural networks, photonic memristors, data storage and bio-voltage memristor. Finally, ideas on the potential of memristive technology are provided for the future.

2. Memristor and underlying parameters

A memristor was initially defined by L. Chua as a memory device that is nonlinear, passive, two-terminal device that coupled electric charge and electrical flux.⁸ Generally, memristive systems can be defined as a nonlinear system with memory affected by one or more state variables denoted by x .⁹ These variables are necessary to determine the future behaviour of a system when the present state of system and inputs are known, and their physical interpretation can be widely broad, each type defining a different case of memristor as discussed in the classification later. Consider two complementary conjugate electrical variables U , Y (voltage, current, charge or flux).

$$Y = F(U, x) \quad (1)$$

$$\tau_k \frac{dx}{dt} = g(U, x) \quad (2)$$

The variable Y does not respond instantaneously to the change of stimulus. The changes of the 'slow' state variables are controlled by a driven adaptation function $g(U, x)$ with the characteristic time τ_k . The main properties of the memristive systems are (a) highly nonlinear characteristics in function F , (b) Significant memory effect which implies that the current value of Y depends on history of the sample by its need to integrate eqn (2).¹⁰

Because of the memory feature, there is a nonlinear relationship between current (I) and voltage (V) causing a pinched hysteresis loop.⁸ Memristive devices require an external voltage to function and current signals passing through the device determine its resistance state. The resistance is reversibly switched between high resistance state (HRS) and low resistance state (LRS) to regulate the current signal in device.⁷ The phrase "resistive switching" describes the phenomenon observed in dielectrics when a soft electric breakdown occurs due to a substantial change in an applied signal, leading to a non-volatile and reversible alteration in resistance. This phenomenon is categorized into two fundamental types: unipolar and bipolar switching. In unipolar switching, the memory state is altered by an electric signal of the same or opposite polarity. On the other hand, bipolar memory states can transition between their two conceivable configurations when an electrical signal with alternating polarity is applied.¹¹ In the realm of memristor dynamics, power consumption and switching speed are pivotal considerations. Power consumption $P = V_{\text{set}} \times I_{\text{set}}$ where V_{set} is set voltage and I_{set} is current at set voltage, underscores the efficiency of energy utilization. Swift and efficient switching across the entire resistance range is crucial for optimal memristor functionality. For instance, in neuromorphic computing, rapid resistance transitions akin to synaptic plasticity enable efficient learning processes. Lower power consumption not only enhances energy efficiency but also broadens the applicability of memristors in emerging technologies, such as edge computing and artificial intelligence, where efficient and high-speed information processing is paramount.

Current switching in memristor devices is classified as digital and analog switching as shown in Fig. 1. Digital switching refers to the ability of device to switch between two or more stable resistance states by applying substantial voltage or current pulse. Such stable resistance states represent the binary data like 0 and 1. Analog switching in memristor refers to the ability of the device to switch between a range of resistance states, rather than just two stable states. The digital switching memristor is a promising component for its use in both access devices and logic circuits. In order to develop neuromorphic computing, it is preferable to use memristors with analog switching behaviour in place of traditional digital logic gates.¹² Data endurance and retention are other two important parameters of memristor to consider. Endurance represents no. of read and write cycles while retention time shows the ability to withstand the ON and OFF states. In Fig. 1, starts from the centre of figure which represents different types of memristor's I - V characterizations to different types of resistive switching mechanisms and at the border of figure different applications.

3. RS mechanism in memristor

3.1 Ion migration

Ion migration type devices comprise of metal–insulator–metal (MIM) structure; a dielectric layer sandwiched between two electrically conducting metal electrodes. Here, the RS between

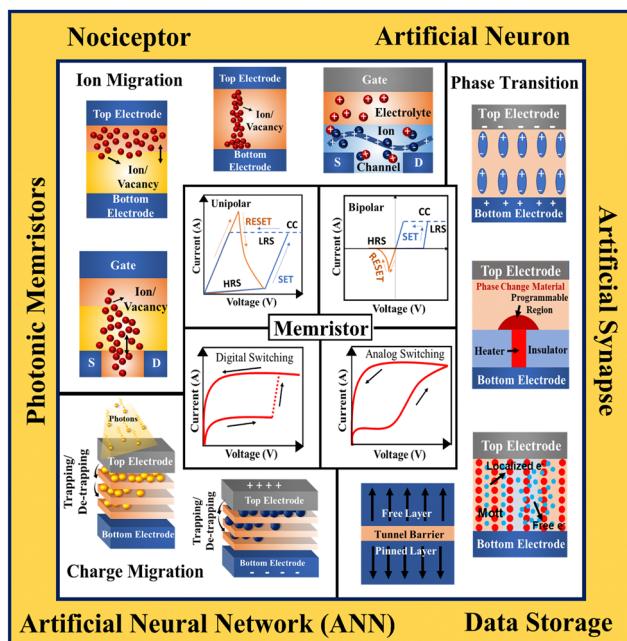


Fig. 1 Summary of the fundamentals, mechanisms and applications of memristor.

the LRS and HRS is the popular filament-type which can be explained by the formation and rupture of conductive filaments (CF) that connects the two electrodes *via* a metal-like percolation path. Various RS effects can be rudimentarily classified based on cation migration and anion migration, determined by migrating ions and redox reaction.¹³ As shown in Fig. 2(a) and (b), ion migration based memristors can be as electrochemical metallization memories (ECM) and valence change memories (VCM).

In ECM memristor, the RS mechanism is led by formation/rupture of the filament, attributed to generation and migration of cations in the dielectric material. ECM memory should have an electrochemically active metal electrode (Ag, Cu, *etc.*), an electrochemically inert metal as counter electrode (Pt, Au, Ir, Sn, *etc.*) and functional material or solid electrolyte (chalcogenide, *etc.*) sandwiched between two metal electrodes. Kim *et al.* reported ECM mechanism for device structure Ag/Cs₃Bi₂Br₉/ITO exhibiting bipolar switching behaviour with high endurance and retention of ~ 2000 cycles and 10^4 s respectively.¹⁷ A wide range of direct and indirect experimental attempts have been made to establish filament formation in the dielectric layer of the ECM memristors. Wang *et al.* carried out an *in situ* field-emission scanning electron microscopy as well as energy-dispersive X-ray spectroscopy analysis and demonstrated the formation of Ag filament as the mechanism of resistive switching in a quantum dot-based CsPbBr₃ all inorganic memristor (see Fig. 2(e) and (f)).¹⁵

VCM-based devices comprise a structure wherein an oxide material is sandwiched between electrochemically inert top and bottom electrodes. These devices rely on the migration and redistribution of oxygen vacancies to induce a filament-type resistive switching (RS) effect, classifying them as VCM or anion migration-based devices.¹⁸ The different mechanisms by which

the conductance state is generated can be classified into three types: filamentary, interfacial, and redox transistor type. Recently, Huang *et al.* reported the change in resistance in their device (Au/ α -CsPbI₃/ITO) due to VCM mechanism, validated by conducting atomic force microscopy which showed high ON/OFF ratio (10^4) with low operating voltage (0.5 V) with multistate operating capability.¹⁶ To investigate the switching mechanism, the Pt tip of the conducting AFM was scanned over the bare CsPbI₃ film and the flow of current could be observed preferably at some locations which are marked by white spots in the current image of Fig. 2(i). When this current profile of the film was mapped with topography as shown in Fig. 2(j), it shows that the current proliferates along the grain boundaries, confirming that the switching mechanism in this device is mainly due to the valence change mechanism.

Electrolyte-controlled RS devices also termed as electrochemical RAM (ECRAM) by IBM are mainly dominated by two mechanisms: electrochemical doping and ion intercalation. Generally, the gate electrode transfers ions from the electrolyte to current conductive film, leads to change in conductance. Thin film transistors like organic electrochemical transistors (OECT) are based on electrochemical doping. It has an organic semiconductor thin film as electronic conductive channel, an electrolyte for ion supply, and a gate electrode. Electrons or holes are responsible for the current generated between the source and the drain. In the other type of ion intercalation, ions injected from the electrolyte can change the band structure, altering the conductivity of the active area. A Li-ion-based transistor with linear and analog switching was described by Fuller *et al.* using Li-ion intercalation into Li_{1-x}CoO₂. Li_{1-x}CoO₂ experiences an insulator-to-metal transition (IMT) as x varies from 0 to 0.5, and this results in an increase in electronic conductivity of six orders of magnitude. Due to the low activation energy of Li diffusion in Li_{1-x}CoO₂, the switching voltage is relatively low (100 mV).¹⁹

3.2 Phase transition

Phase transition-based memory (PCM) is a type of non-volatile memory that utilizes the reversible phase change between two states in a material to store information. PCM comprises an active volume of phase-change material sandwiched between two electrodes and undergoes the transformation from a highly conductive state (crystalline phase) to a low conductive state (amorphous phase) and *vice versa*. Subject to the applied current pulses, the temperature of material increases as an effect of Joule heating and thermoelectric effect. *Via* the Joule heating effect, the device can be either SET by crystallization of amorphous phase, or the device can be RESET by amorphization of the crystalline phase.²⁰ Fig. 3(a) and (b) show the cross-section schematic of the conventional PCM cell and its typical I - V characteristics respectively.²¹ The resistance contrast between the set and reset states is substantially below the threshold voltage (V_{th}). This is reversible on the withdrawal of voltage pulse and also switch to the LRS for an applied voltage greater than V_{th} . However, memory switching is observed for a voltage pulse width longer than the crystallization time.²¹ To set the PCM cell into the crystalline phase, a medium current

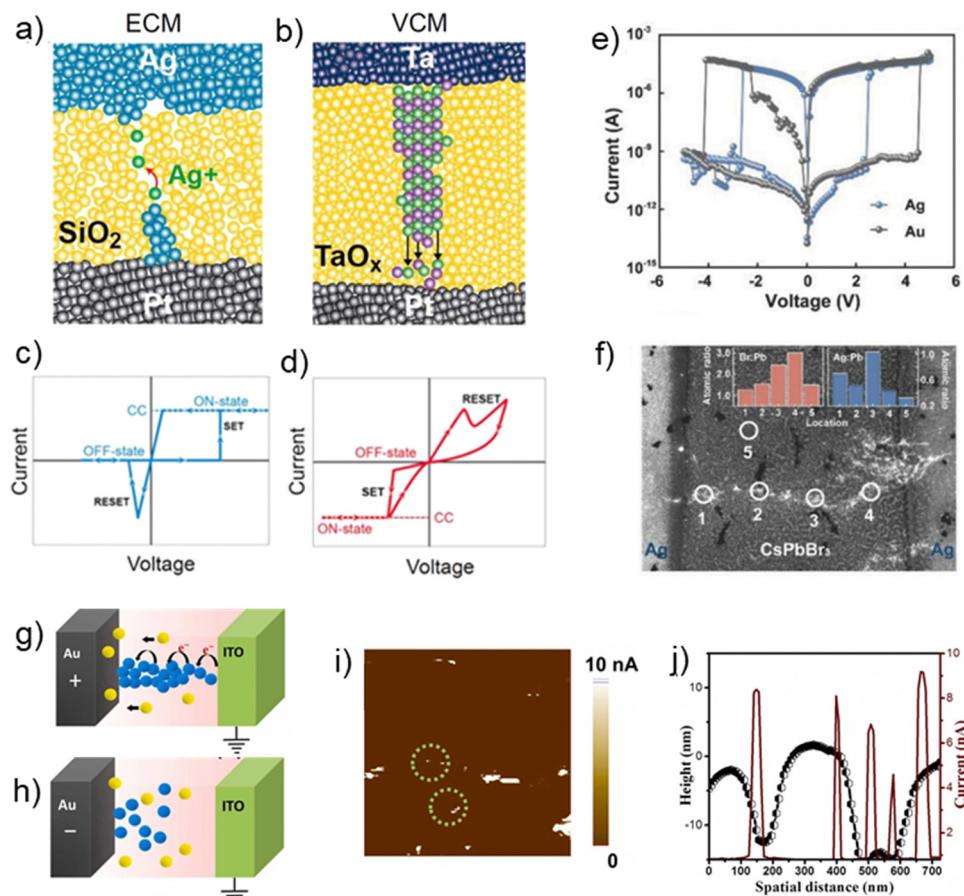


Fig. 2 Schematic of the switching mechanism in (a) Pt/SiO₂/Ag and (b) Pt/TaO_x/Ta memory cell structure and corresponding *I*–*V* characteristics for (c) ECM cells, and (d) VCM cells. Reproduced from ref. 14 with permission from IOP Publishing Ltd, copyright 2017; (e) *I*–*V* characteristic of the ITO/PMMA/CsPbBr₃/PMMA/metal structured ECM memory cell with Ag and Au metal anode, (f) *in situ* SEM images of Ag/CsPbBr₃/Ag device showing the formation of Ag filament. Schematic view of the (g) SET and (h) RESET processes in a VCM cell. Reproduced from ref. 15 with permission from John Wiley and Sons, copyright 2018. Yellow balls represent iodide ion and blue balls represent iodide vacancy, (i) *in situ* current image of the $\alpha\text{-CsPbI}_3$ film acquired by conducting AFM (c-AFM), and (j) corresponding distribution of the current profile according to the morphology of the film. Reproduced from ref. 16 with permission from Elsevier, copyright 2023.

pulse is applied for comparatively longer period to anneal the programming region at a temperature between the crystallization temperature and the melting temperature (blue pulse in Fig. 3(c)). To reset the cell into an amorphous state, a very short pulse is applied to anneal it at a temperature higher than the melting temperature (red pulse in Fig. 3(c)).

In metal-to-insulator transition memory (Mott), the metal-insulator transition (MIT) characteristic of Mott material is utilized in Mott transition-based memory. The competition between localization and delocalization of electrons is the main underlying mechanism supporting MIT phase transition and conductance-switching behaviour. A wide range of factors can trigger phase transition including temperature, electrical, doping, optical, and magnetic stimulation. It is noteworthy, unlike physical and structural changes that occur at a temperature between the crystallization temperature and the melting temperature as well as greater temperature than melting temperature in PCM. Mott transition is driven by electron correlation and band structure changes, therefore more resilient to

repeat stress than PCM. Recently, a lot of interest has been shown in electrically/thermoelectrically triggered MIT devices as potential bidirectional devices are selected for ReRAM applications due to their simple structure metal/metal-insulator stack, high ON/OFF ratio, and quick transition speed. The physical mechanisms are precisely discussed by extensive investigation in many research papers.^{22,24} H. S. Lee *et al.* published several research papers on voltage-driven transition of Pr_{0.7}Ca_{0.3}MnO₃ (PCMO) based ReRAM. In such devices, the transition occurs between the initial p-conductor PCMO and partially oxygen-deficient Mott insulator PCMO as shown in Fig. 3(d) along with the change in band structure.²²

Ferroelectric random-access memory (FeRAM) is also a non-volatile memory, in which data are stored using hysteretic *P*–*E* (polarization *vs.* electric field) characteristics in a ferroelectric film. FeRAMs are being mass-produced at present and widely used in IC (integrated circuits) cards and RF (radio frequency) tags. Their benefits include non-volatile data storage, the lowest power consumption and, fast operating speed as DRAM. As

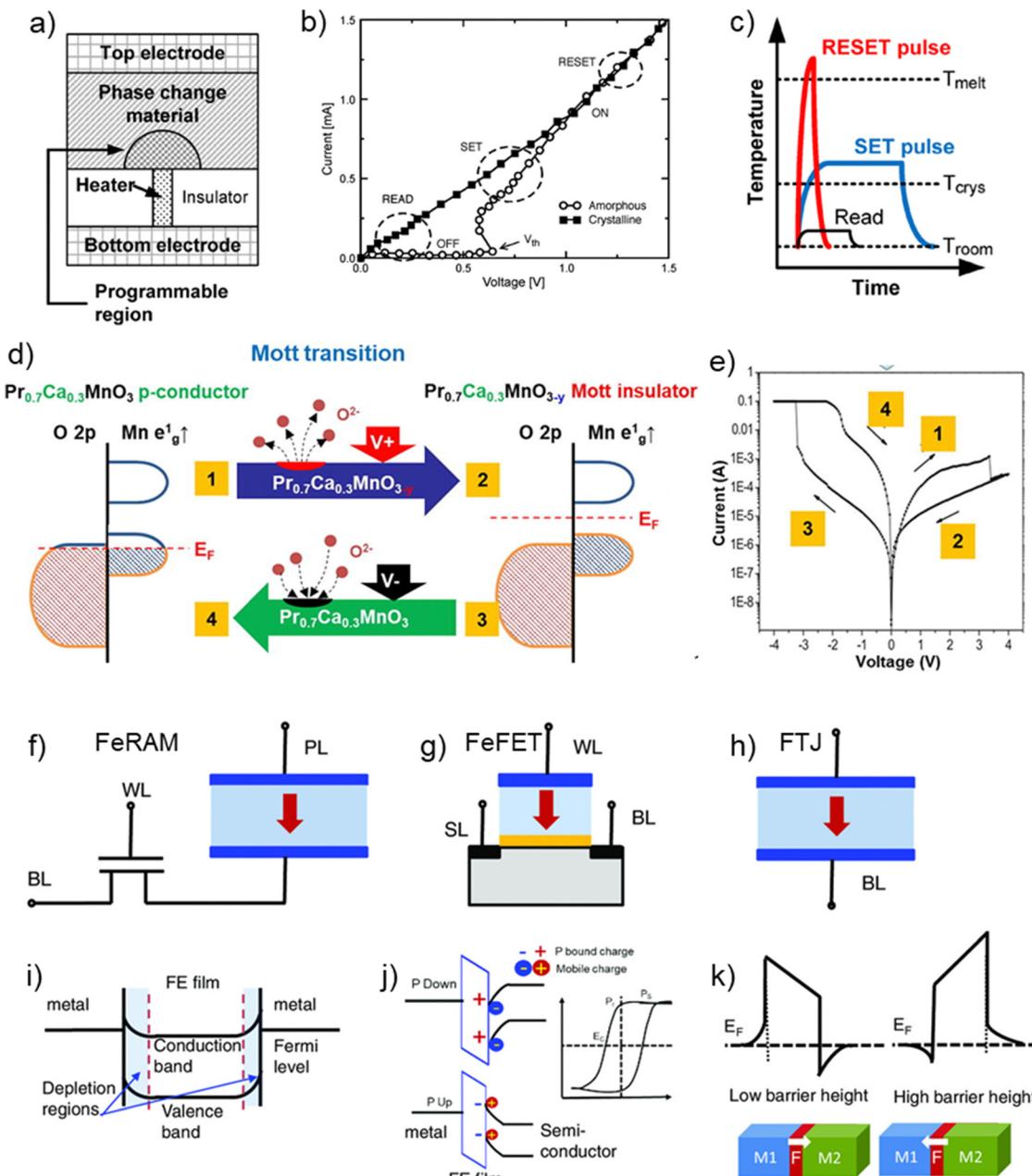


Fig. 3 (a) The cross-section schematic of the conventional PCM cell. (b) I – V characteristics of set and reset state, the white circles and the black squares represents the amorphous and crystalline states respectively, and (c) applied SET, RESET, and read pulses which change temperature accordingly reproduced from ref. 21 with permission from IEEE, copyright 2010; (d) a schematic of the transition between p-conductor PCMO ($\text{Pr}_{0.7}\text{Ca}_{0.3}\text{MnO}_3$) and partially oxygen deficient Mott insulator PCMO and (e) the corresponding I – V characteristics measured by a DC voltage sweep of ± 4 V and a compliance current of 100 mA Reproduced from ref. 22 with permission from Elsevier, copyright 2019; (f) 1T–1C FeRAM cell, (g) one-transistor FeFET cell, (h) an FTJ, and (i)–(k) the schematics of their corresponding device band diagrams respectively reproduced from ref. 23 with permission from John Wiley and Sons, copyright 2022.

known, this ferroelectric material exhibits polarization even in the absence of external electric stimulation and by applying electrical stimulation the direction of polarization can be reversed. FeRAMs are generally classified into two types: capacitor-type and field effect transistor (FET) type.²⁵ The schematic of the device architectures of these two types are shown in Fig. 3(f) and (g) and the corresponding working principles are illustrated in Fig. 3(i) and (j) using the respective

band diagram. A traditional FeRAM has one transistor-one capacitor (1T-1C) configuration, where the data storage is done in the FE capacitor while a MOS transistor acts like a switch. Although such FeRAM gives robust device performance, it comes with a price of high operating voltage and large footprint. In a FeFET cell, a ferroelectric layer is embedded in the FET gate stack which acts as the charge storage medium (Fig. 3(g)). The non-volatile analog switching behaviour of

FeRAM makes it eligible for application in neuromorphic computing and deep neural networks (DNN). Another type of ferroelectric material based memristor is ferroelectric tunnel junction (FTJ). As shown in Fig. 3(h), in FTJ, an ultrathin layer (1–5 nm) of FE barrier is sandwiched between two different metal or semiconducting electrodes. The orientation of polarization in the tunnel barrier can be switched between two perpendicular directions (up or down) by applying a varying electric field and charge carriers either accumulate or deplete from the interface layers of the electrodes (Fig. 3(k)).²³

Magneto-resistive random-access memory (MRAM) is a class of solid-state storage circuits that store data as stable magnetic states of magneto-resistive devices and read data by measuring the resistance of devices to determine their magnetic states. MRAM makes use of a pair of ferromagnetic metal plate differentiated by thin insulating or dielectric spacer layer. A metal is defined as magneto-resistive when it shows the change in electrical resistance if placed in magnetic field. These two metal plates and the insulating layer together is termed as magnetic tunnel junction (MJT). One of the metal plates is

known as fixed or reference layer as its magnetic direction never changes while another plate is known as free layer as its magnetic direction changes, on the application of external bias. Unlike other resistive switching devices where electrical charge determines whether bit binary is 0 or 1, here the magnetic field determines the binary bits. These MJT based circuits are all resistive memories in terms of read operation. It is the writing method of magnetic states that differentiates them and forms different types of MRAM technologies. The most commonly studied writing methods include thermally assisted switching, spin torque switching and Savchenko switching.²⁶

3.3 Charge migration

Charge migration (trapping/de-trapping) is another mechanism involved in ReRAM or RS memory. When a voltage is applied to the ReRAM device, charges are injected into the active material and can become trapped in defects within the layer. The trapped charges can change the local electric field within the oxide and affect the resistance of the material. The trapped charges can be released or de-trapped by applying a voltage of

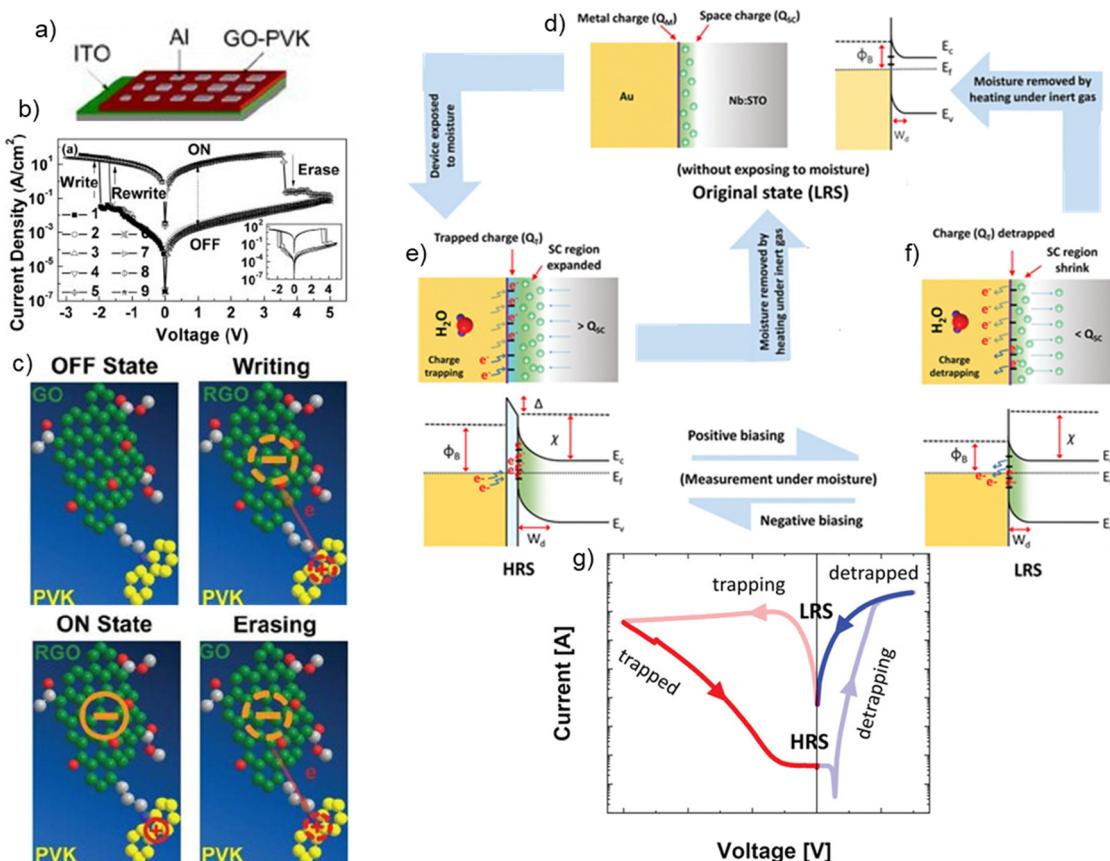


Fig. 4 (a) A schematic diagram of the charge transfer-based Al/GO–PVK/ITO memristive device, (b) the corresponding J – V characteristics, and (c) plausible switching mechanism of GO–PVK complex. GO and RGO stand for graphene oxide and reduced graphene oxide respectively reproduced from ref. 28 with permission from AIP Publishing, copyright 2009; (d)–(f) moisture induced charge trapping and de-trapping mechanism at Au/Nb:STO interface, (d) initially without exposure to moisture a clean interface and an intrinsic Schottky barrier profile exists, (e) the device goes to the HRS upon building an interfacial charge layer with the negative bias charges (e.g., electrons) trap at the interface via moisture interaction, (f) the device goes to the LRS with the positive bias and subsequent electrons de-trapping from the interface, corresponding to a increase and decrease in Φ_B and W_d are also shown, and (g) the corresponding I – V characteristics reproduced from ref. 29 with permission from John Wiley and Sons, copyright 2023.

opposite polarity. This changes the electric field within the oxide, causing the trapped charges to be released and the resistance of the material to return to its original state. The ability to trap and de-trap charges is dependent on the material properties of the oxide and the electrodes, as well as the voltage and time applied. The exact mechanisms can vary depending on the specific ReRAM device and the materials used.²⁷ Liu *et al.* reported a poly(*N*-vinylcarbazole)-functionalized graphene oxide (GO-PVK) based memristor which had a device structure of Al/GO-PVK/ITO and exhibited resistive switching *via* intramolecular charge transfer (Fig. 4(a)–(c)). The as-fabricated device is in the low conductivity state due to the presence of a tunneling barrier for charge transport. At the switching voltage, electrons transit from the PVK moieties into the GO resulting in reduced graphene oxide (RGO) nanosheet and enhanced conductivity.²⁸

Recently in 2022, Kunwar *et al.* discussed the modulation of Schottky barrier by charge trapping/detrapping mechanism for their device (Au/Nb:STO). In this work, they further claimed moisture trapped at the interface of device is major source for electron trapping and interface Schottky modulation. Devices exhibited wide *I*–*V* hysteresis area in moist atmosphere leading to electron trapping process while the *I*–*V* hysteresis diminished in the absence of moisture leading to electron detrapping process.²⁹ The schematic of the moisture induced charge trapping and de-trapping mechanism and the corresponding *I*–*V* characteristics are shown in Fig. 4(d)–(g). A summary Table 1 is given to compare some of the devices with the different resistive switching mechanisms and performance parameters.

3.4 Redox mechanism

The exploration of redox mechanisms within memristors represents a pivotal area of research, with numerous reports delving into the intricate details that govern the operation of these nanoscale devices.^{30–32} The exploration of redox mechanisms within memristors represents a pivotal area of research, with numerous reports delving into the intricate details that govern the operation of these nanoscale devices. These mechanisms, often involving the manipulation of ionic concentrations and the migration of ions within the memristor, play a decisive role in shaping its resistance states. Understanding these redox processes at the nanoscale is of paramount importance as they are fundamental in influencing a memristor's capacity to retain and modulate resistance levels—a crucial aspect for both information storage and processing. In a significant breakthrough, S. Goswami *et al.* uncovered a charge-disproportionate molecular redox mechanism, offering a deterministic condensed matter pathway to achieve three discrete conductance plateaus. These plateaus, characterized by their functional non-volatility and robustness, represent a notable advancement in the landscape of memristor technology.³¹ Building upon this groundbreaking finding, Goswami and collaborators introduced a novel approach by employing voltage-driven conditional logic interconnectivity between different molecular redox states of a metal-organic complex. This innovative strategy allowed them to embed a complex network of decision trees, comprising an

impressive 71 nodes, within a single memristor.³⁰ Grasping the nuances of these redox mechanisms emerges as a cornerstone in advancing the efficacy and scalability of memristor-based technologies. As researchers continue to unravel the intricacies of redox mechanisms, they open up new horizons for the integration of memristors in cutting-edge technological applications, promising a future where these devices play a transformative role in the evolution of electronic systems.

4. Current conduction mechanisms in memristors

The current conduction in the memristor primarily depends on the material of the dielectric layer, electrodes and the properties of the interfaces formed. Based on these properties, possible conduction mechanisms can be broadly divided as injection-limited and bulk limited. Multiple mechanisms may be exhibited in the same device depending on the resistance state of the memristor (*i.e.* filamentary or non-filamentary), as well as operating conditions, such as range of applied fields, operating temperature, *etc.* In the following section, we discuss these mechanisms, and their corresponding analytical model is summarized in Table 2.

4.1 Injection limited conduction mechanism

In these mechanisms, electron conduction depends on the properties of the electrode–dielectric interface such as barrier height and width. Schottky emission, Fowler–Nordheim (F–N) tunneling, and direct tunneling are some examples of injection-limited mechanisms. In case of Schottky emission, also known as thermionic emission, electrons are thermally activated and injected into the conduction band of the dielectric over a Schottky barrier (Fig. 5(a)). This is most common in oxide based memristors such as Al/ZnO/Al,⁶¹ Al/Al₂O₃/Nb_xO_y/Au,⁶² *etc.* In a simplified model, the emitted electron current density (J) can be described by the Richardson–Dushman by equation (eqn (3)), where A is Richardson constant, T is absolute temperature, q is elementary charge, Φ_B is the junction barrier, and k is Boltzmann constant.

$$J = A \times T^2 \times \exp\left(\frac{-q\Phi_B}{kT}\right) \quad (3)$$

when a higher field is applied, the electrons may tunnel through the dielectric layer. If the layer is thinner than 3 nm, direct tunneling is more dominant, whereas, in the case of a thicker oxide, the conduction can be dominated by F–N tunneling (Fig. 5(b) and (c) respectively).

4.2 Bulk limited conduction mechanism

When there are sufficient carriers present in the bulk material, the current conduction mechanism is governed by the characteristics of the dielectric such as carrier mobility, dielectric properties, trap properties, *etc.* Ohmic conduction, Poole–Frenkel (P–F) emission, space charge limited current (SCLC), ionic conduction, hopping conduction, trap-assisted tunneling (TAT)

Table 1 Comparison of RS performance and applications based on different switching mechanisms

Mechanism		Device structure	On/ff ratio	Endurance (cycles)	Retention (s)	Applications	Ref.
Ion migration	ECM	Pt/(γ -AlOOH/ITO/PET) Ag/PCPX-Ag/ITO Au/Ag/PVdf-HFP/Au Ag/BIO/Pt	$>10^3$ 10^4 10^7 10^5 10^4 10^4	$\geq 10^4$ — $\geq 10^2$ 50 3×10^3 10^2	$>2 \times 10^4$ $>10^4$ $>10^4$ 10^4 6×10^3 $\sim 10^4$	Artificial nociceptor SNN, neuromorphic applications Data storage Neuromorphic computing and retinalike sensors Flexible artificial synapse Synaptic applications, neuromorphic analogue circuits High density storage and neuromorphic computing	33 34 35 36 37 38
	VCM	Au/Pt/Ag/ITO Ti/Au/InO _x /Ti/Au Au/Mo ₂ C/MoS ₂ /Au Au/Cr/CuSe/Cr/Au	$>10^3$ $>10^2$ 3×10^2 $>10^8$	$>10^2$ $>10^2$ 3×10^2 $>10^8$	6×10^3 $\sim 10^4$ 10^4 $>10^8$		39
	ECRAM	(Ti ₃ C ₂ T _x) MXene Pt/WO ₃ Nb:SrTiO ₃ W/Si/LPO/WO ₃ /W	— — 8	$>10^2$ 10^4 10^5	$>10^3$ 10^4 10^3	Data storage Artificial synapse Memory applications	40 41
	PCM	C ₃₄ (Sb ₂ Te) ₆₆ -based device C-based/SiGeAsSe/C-based Ge ₂ Sb ₂ Te ₅ (GST-225) based device Ge ₁₁ Te ₆₀ Sn ₄ Al ₂₅ based device Au/LNO/Cr/Pt/Cr	$>10^3$ — — — —	$>10^8$ — — — —	$>10^6$ — — — —	OTS memory applications Optical disk memory Optical disk memory Analog-neuromorphic computing Spike-based intelligence machines	42 43 44 45
	Mott	Pt/VO ₂ /Pt SrCoO _x (SCO) based device	— 4	5×10^5 $>10^4$ 10^8	10^5 — 3×10^3	— — —	46 47 48
	FERAM	Ti/GaN/ScAlN/IMMO TiIN/HZO/WO _x /TiIN Au/CuInP ₂ S ₆ (CIPS)/Ti	40 10 10^2	10^5 10^8 10^2	10^5 5.4×10^5 2×10^3	Neuromorphic computing In-memory computing for neuromorphic hardware Spike-based intelligence machines,	49 50 51
MRAM		Ti/Oxide/ScAlN/GaN Oxad MTI-CoFeB/MgO based device	10^5 —	$>10^5$ 10^{11}	10^4 10^8	Analog in-memory computing Large scale integrated circuit	52 53
		Ia _{0.7} Sr _{0.3} MnO ₃ /BaTiO ₃ /La _{0.7} Sr _{0.3} MnO ₃ Au/Pt/Au	— —	— 10^2	$>10^3$ 10^3	Artificial synapse Neuromorphic vision sensors	54 55 56
Charge migration	Photonic	ITO/ZnO/ZSO/ITO	750	$>10^3$	10^2	Opto-electronic neural system	57 58
	Electronic	Pt/Ta ₂ O ₅ /Nb _x O _{5-x} /Al ₂ O _{3-y} /Ti Al/CdSe-PVP/Al	10^3 6.1×10^4	$>10^5$ $>10^2$	$>2 \times 10^4$ $>10^4$	Neuromorphic applications Data storage	59 60

Table 2 Analytical expression of current density and the field/temperature dependency of the conduction mechanism discussed above. Here, the usual meaning symbols and variables used can be found in the relevant literature.⁶⁷

Conduction mechanism	Current density	Electric field/temperature dependency
Schottky emission	$J_{SE} = \frac{4\pi q m^*(kT)^2}{h^3} \exp\left(\frac{-q(\phi_B - \sqrt{qE/\pi e})}{kT}\right)$	$J_{SE} \propto T^2 \exp\left(A\frac{\sqrt{E}}{T} - B\right)$
Fowler Nordheim tunneling	$J_{FN} = \frac{q^2}{8\pi h\Phi_B} E^2 \exp\left(\frac{-8\pi\sqrt{2qm^*}}{3hE} \Phi_B^{3/2}\right)$	$J_{FN} \propto E^2 \exp\left(\frac{-A}{E}\right)$
Direct tunneling	$J_{DT} \approx \exp\left\{\frac{-8\pi\sqrt{2q}}{3h} (m^*\Phi_B)^{1/2} \cdot t_{ox,eq}\right\}$	$J_{DT} \propto \exp(-Ak \cdot t_{ox,eq})$
Ohmic	$J_{ohmic} = q\mu N_C E \exp\left[\frac{-(E_C - E_F)}{kT}\right]$	$J_{ohmic} \propto E \cdot \exp\left(\frac{-A}{T}\right)$
Poole Frenkel emission	$J_{PFE} = q\mu N_C E \exp\left[\frac{-q(\phi_T - \sqrt{qE/\pi e})}{kT}\right]$	$J_{PFE} \propto E \cdot \exp\left(A\frac{\sqrt{E}}{T} - B\right)$
Space charge limited conduction	$J_{SCLC} = \frac{9}{8} \epsilon_i \mu \theta \frac{V^2}{d^3}$	$J_{SCLC} \propto E^2$
Ionic conduction	$J_{ionic} \propto \frac{E}{T} \exp\left(\frac{-\Delta G^\#}{kT}\right)$	$J_{ionic} \propto \frac{E}{T} \exp\left(\frac{-A}{T}\right)$
Nearest neighbour hopping	$J_{NNH} = \sigma_0 \exp\left(\frac{-T_0}{T}\right) \cdot E$	$J_{NNH} \propto E \cdot \exp\left(\frac{-A}{T}\right)^{\frac{1}{4}}$
Variable range hopping	$J_{VRH} = \sigma_0 \exp\left(\frac{-T_0}{T}\right)^{\frac{1}{4}} \cdot E$	$J_{VRH} \propto E \cdot \exp\left(\frac{-A}{T}\right)^{\frac{1}{4}}$
Trap assisted tunneling	$J_{TAT} = A \exp\left(\frac{-8\pi(\sqrt{2qm^*})}{3hE} \Phi_T^{3/2}\right)$	$J_{TAT} \propto \exp\left(\frac{-A}{E}\right)$

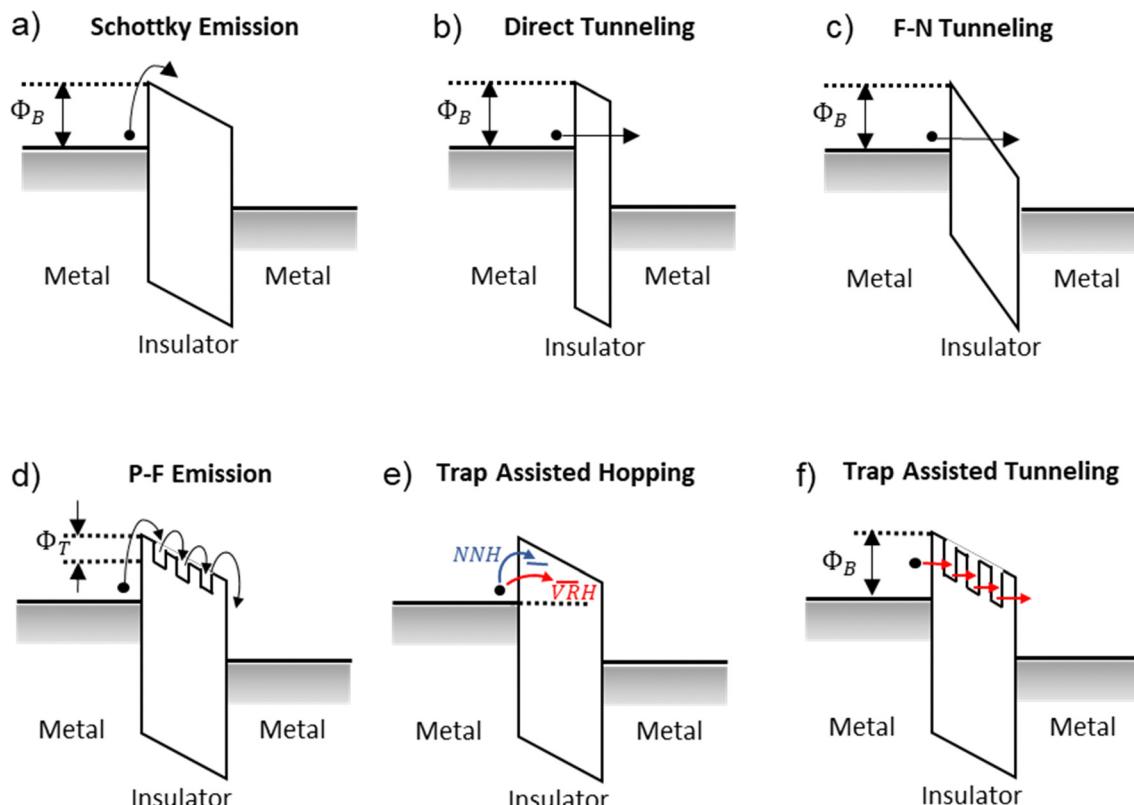


Fig. 5 Schematic energy band diagram of different current conduction mechanisms in memristor; (a) Schottky emission; (b) direct tunneling, (c) Fowler Nordhiem tunneling, (d) Poole Frenkel emission, (e) trap assisted hopping (blue arrow nearest neighbour hopping, red arrow variable range hopping), and (f) trap assisted tunneling.

are some of the commonly encountered bulk-limited mechanisms in memristive devices. When the applied field is low, there are a smaller number of thermally generated mobile carriers in the bulk and the electron transport occurs through ohmic conduction in which current density is directly proportional to the electric field. When sufficient carriers can get injected from the contact and accumulate in the bulk to create a space charge region, the overall conductivity of the material decreases, and the device current is limited by the rate of movement of the accumulated carriers. This conduction mechanism is known as space charge limited current. The space charge can be caused by factors such as trapping of charge carriers at defects or impurities or the slow recombination of carriers at certain interface. The SCLC mechanism can be easily identified from the power law dependence of the current-voltage characteristics ($I \propto V^n$). The trap-filled or trap free SCLC conduction is represented by $I \propto V^2$ ($n = 2$), also known as child's square law region, while trap filling SCLC region may have much higher value of n .⁶³ In P-F emission, the trapped carriers attain sufficient energy from the applied electric field to get excited to conduction band of the insulator and thereby participate in the current conduction (Fig. 5(d)). Analytically, it is quite similar to Schottky emission model, except for the exponential dependence of Φ_B which is replaced by the trap potential barrier. I. A. Petrenyov *et al.* demonstrated a memristor based on nanotubular arrays of zirconium oxide

where P-F emission is the dominant conduction mechanism.⁶⁴ All types of materials used as dielectric layers for memristors often contain many defects and impurities that can act as traps and contribute to current conduction in different ways. In such disordered materials, one commonly encountered mechanism is hopping conduction. When a trapped electron hops into the nearest trap site by tunneling the potential barrier, it is known as nearest neighbour hopping (Fig. 5(e), blue arrow). In the case of highly disordered systems, such trapped electrons may hop into trap sites further away with a lower trap energy barrier, instead of the nearest one (Fig. 5(e), red arrow). Such hopping mechanism is called Mott variable range hopping. Z. Zhou proposed a TiN/SiO_x/p-Si tunneling junction based memristor device that exhibited artificial synapse characteristics and proposed that the variable-range hopping and F-N tunneling theories are responsible for gradual conduction change.⁶⁵ Trap assisted tunneling (TAT) is another type of conduction mechanism, in which, electrons from the cathode are first captured by traps temporarily before tunneling through the barrier (Fig. 5(f)). This process allows carriers to tunnel through energy barriers that would otherwise be too high for direct tunneling. Recently, P. Mainali *et al.* demonstrated light operated synaptic potentiation in an $\alpha\text{-Fe}_2\text{O}_3$ /p-Si memristive device. From the fitting results of the $I-V$ characteristics, it was concluded that the conduction is dominated by TAT when voltage is lesser than 0.7 V and P-F emission when it is higher than 0.7 V.⁶⁶

Table 3 Current–voltage relationships and state variable expressions of different memristor models discussed here. Here, the usual meaning symbols and variables used can be found in the relevant literature

Memristor model	Current–voltage relationship	State variable expression
Dopant drift model ⁶⁸	$v(t) = \left(R_{\text{ON}} \frac{w(t)}{D} + R_{\text{OFF}} \left(1 - \frac{w(t)}{D} \right) \right) i(t)$ $i(t) = w^n(t) \beta \sinh(\alpha v(t)) + \gamma \exp(\lambda v(t) - 1)$	$\frac{dw(t)}{dt} = \mu_v \frac{R_{\text{ON}}}{D} i(t)$ $\frac{dw(t)}{dt} = \mu_v \frac{R_{\text{ON}}}{D} i(t)$
Yang model ⁷⁵	$i(t) = w\gamma \sinh(\delta v(t)) + (1-w)\alpha[1 - \exp(-\beta v(t))]$	$\frac{dw(t)}{dt} = \lambda \sinh(\eta v(t))$
Chang model ⁷⁶	$i(t) = I_0 \left[\exp \left\{ \frac{q}{\eta k T} [v(t) - i(t) R(t)] \right\} - 1 \right], \quad \text{for } v > 0$ $I_0, \quad \text{for } v < 0$	$\frac{dw(t)}{dt} = \mu_v \frac{R_{\text{ON}}}{L^3} i(t) w(t) [L - w(t)]$
Hur <i>et al.</i> ⁷⁷		
Tunnel barrier model ⁷⁹	$i = \frac{I_0}{\Delta w^2} \left\{ \phi_1 e^{-B\sqrt{\phi_1}} - (\phi_1 + e v_g) e^{-B\sqrt{\phi_1 + e v_g }} \right\}$	$\frac{dw(t)}{dt} = \begin{cases} c_{\text{off}} \sinh \left(\frac{i}{i_{\text{off}}} \right) \exp \left[-\exp \left(\frac{x - a_{\text{off}} - i }{w_c} - \frac{x}{b} \right) \right] - \frac{x}{w_c}, & i > 0 \\ c_{\text{on}} \sinh \left(\frac{i}{i_{\text{on}}} \right) \exp \left[-\exp \left(\frac{x - a_{\text{on}} - i }{w_c} - \frac{x}{b} \right) \right] - \frac{x}{w_c}, & i < 0 \end{cases}$
TEAM model ⁸⁰	$v(t) = \left(R_{\text{ON}} + \frac{R_{\text{OFF}} - R_{\text{ON}}}{x_{\text{off}} - x_{\text{on}}} (x - x_{\text{on}}) \right) i(t)$	$\frac{dw(t)}{dt} = k_{\text{off}} \left(\frac{i(t)}{i_{\text{off}}} - 1 \right)^{a_{\text{off}}} f_{\text{off}}(x), \quad 0 < i < i_{\text{off}}$ $\frac{dw(t)}{dt} = 0, \quad i_{\text{off}} < i < i_{\text{on}}$
Yakopcic model ⁸¹	$I(t) = \begin{cases} a_1 \sinh(bv(t)) x(t) \\ a_2 \sinh(bv(t)) x(t) \end{cases}$	$\frac{dx}{dt} = \eta g(v(t)) f(x(t))$ $g(v(t)) = \begin{cases} A_p (e^{v(t)} - e^{v_p}), & v(t) > v_p \\ A_n (e^{-v(t)} - e^{v_n}), & v(t) < -v_n \end{cases}$ $f(x(t)) = \begin{cases} 0, & -v_n \leq v(t) \leq v_p \\ e^{-(x(t)-x_p)} w_p(x(t), x_p), & x(t) \geq x_p \\ e^{(x(t)+x_n-1)} w_n(x(t), x_n), & x(t) \leq 1 - x_n \\ 1, & 1 - x_n \leq x(t) \leq x_p \end{cases}$

5. Analytical modelling of memristors

To cater to this wide range of memristor materials and a variety of working mechanisms different analytical models have been proposed in the literature starting from material-level atomistic modelling, semiconductor physics-based device modelling, and compact modelling for large-scale circuit implementation. Here, we briefly review the progress in memristor modelling approaches. We restrict our discussion to the modelling attempts which can be described by simple analytical expressions or can be represented by some equivalent circuits. Table 3 lists the current–voltage relationships and state variable expressions of the memristor analytical models discussed here.

5.1 Dopant-drift model

Linear ion drift model⁶⁸ is the first and simplest model based on the TiO₂ memristor from HP labs. The model considers the dopant occurring from the oxygen-deficient titanium dioxide layer (TiO_{2-x}) drift linearly in a uniform field. The device resistance is dependent on the ratio between the value of the dynamic state variable $w(t)$, representing the thickness of the non-stoichiometric TiO_{2-x} layer and the device thickness D (Fig. 6(a) and (b)). Although this model was the breakthrough in the field of memristor research and several works have been based upon this model,^{69–71} this model is highly inaccurate considering the highly non-linear nature of the motion of the ions in practical devices, with a significant reduction of their drift velocity at the boundary regions. To address the

nonlinearity at the boundary, various window functions have been introduced.^{72–74} A window function $g(i)$, when multiplied with the state variable derivative equation makes the change of state variable nonlinear. Table 3 shows some of the window functions found in the literature, their mathematical representation, symmetry in the opposite polarity of field, capability of resolving boundary issues, capability of addressing nonlinear drift, scalability, and graphical representation as a function of w/D ratio.

5.2 Circuit-based memristor model

Several attempts were made to model the memristor using certain circuit equivalents. Yang *et al.* proposed a combination of a memristor and a rectifier in parallel to realize the hysteretic I – V characteristics (Fig. 6(c)).⁷⁵ It assumes asymmetric switching in the sense that during ON state, I – V curve follows a tunneling process and during OFF state I – V curve follows the behaviour of a PN junction. The first of the two terms of the model is an approximated representation of a flux-controlled memristor taken from tunneling barrier model, which we use for the ON state of the memristor. The second term represents the rectifier when the memristor is switched OFF. The authors demonstrated that the potential barrier height modifications at the Pt/TiO₂ interfaces due to the drift of positively charged oxygen vacancies lead to ohmic or rectifying-type characteristics and subsequently device resistance switches. Chang *et al.* proposed a modified memristor-rectifier model, based on WO_x memristors, which introduced nonlinearity in the state variable

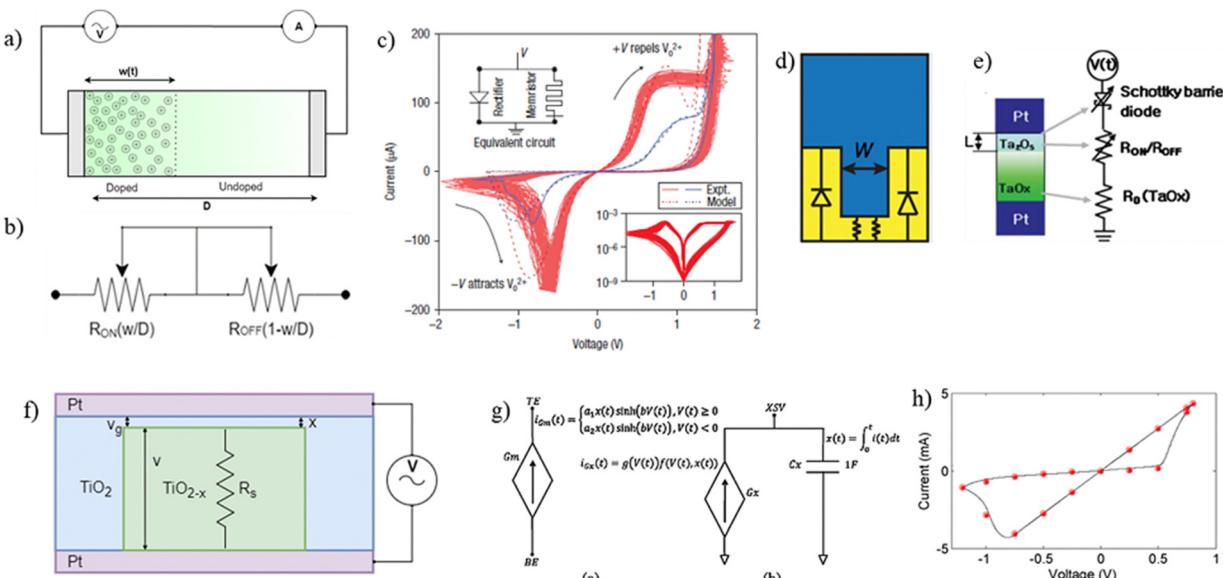


Fig. 6 (a) Schematic of the first TiO₂ memristor where $w(t)$ is the state variable that represents the length of the doped region, (b) the linear ion drift model represented as a series of two resistors reproduced from ref. 68 with permission from Springer Nature, copyright 2008, (c) I – V characteristics of a TiO₂ memristor, the inset shows the model which is a combination of a memristor and a rectifier in parallel reproduced from ref. 75 with permission from Springer Nature, copyright 2008. (d) Schematic of a Pd/WO₃/W memristor where the filament area in the conductive region acts as the state variable reproduced from ref. 76 with permission from Springer Nature, copyright 2011. (e) Schematic of Pt/Ta₂O₅/TaO_x/Pt memristor and the corresponding circuit model, with variable Schottky barrier, variable resistor, and base layer resistance reproduced from ref. 77 with permission from American Physical Society, copyright 2010. (f) Schematic of a Pt/TiO₂/Pt memristor, where the tunnel barrier acts as the state variable reproduced from ref. 79 with permission from AIP Publishing, copyright 2009. (g) The SPICE subcircuit for Yakopcic model, (h) experimental I – V characteristics of a TaO_x memristor with reference to the one simulated using Yakopcic model reproduced from ref. 83 with permission from IEEE, copyright 2013.

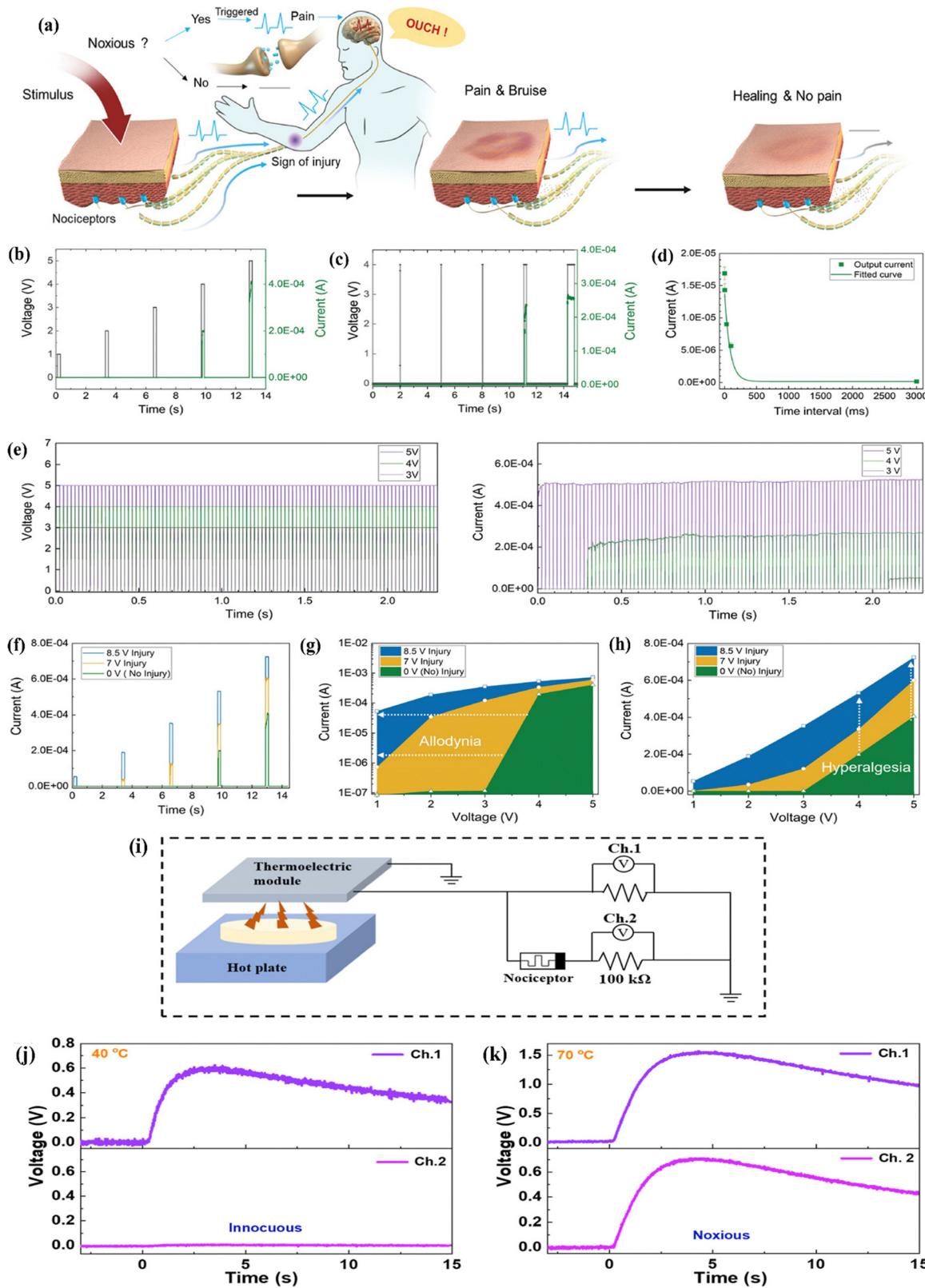


Fig. 7 Demonstration of the first bioinspired artificial injury response system with advanced functions, including a sense of pain, sign of injury, and healing, under different scenarios. (a) Schematic illustration of the physiological protection modality of human bodies under noxious stimuli, including a sense of pain, sign of injury, and healing. (b)–(e) An artificial nociceptor with four signature nociceptive characteristics: threshold, no adaptation, relaxation, and sensitization. (b) Pulse level measurement: a train of 200 ms wide voltage pulses (black) with different amplitudes (1, 2, 3, 4, and 5 V) and the corresponding output currents (green). The interval time between pulses was with 3 s. (c) Pulse width measurement: a train pulse of 4 V (black) with different pulse width (0.5, 1, 10, 200, and 500 ms) and the corresponding output currents (green). The interval time between pulses was with 3 s. (d) Relaxation: the current response at 2 V (200 ms) after a train pulse of 4 V (200 ms) with different interval time: 0.1, 1, 30, 100, and 3000 ms. (e) Current response of the device to 100 voltage pulses (pulse width of 20 ms and pulse interval of 2 ms) with different amplitude (3, 4, and 5 V). The higher the pulse level, the shorter the incubation time. (f)–(h) Demonstration of the allodynia and hyperalgesia features. (f) The output currents at 200 ms voltage pulses with different amplitudes (1, 2, 3, 4, and 5 V) 3 min after different injury pulses (8.5 V – blue, 7 V – yellow, 0 V – green/no injury). The corresponding maximum output currents at different pulse amplitudes in (g) log scale and (h) linear scale. Reproduced from ref. 89 with permission from John Wiley and Sons, copyright 2022. (i) Illustration of electric circuit with thermoelectric module and a nociceptor device. The generated output of nociceptor device and thermoelectric module was observed by oscilloscope channels ch. 1 and ch. 2 at different hot plate temperature of (j) 40 °C and (k) 70 °C. Reproduced from ref. 90 with permission from American Chemical Society, copyright 2023.

function of Yang's model.⁷⁶ The model considered the conductive region area as the state variable (Fig. 6(d)) and a sin hyperbolic function was used to represent the state variable equation that reflects the exponential dependence of the velocity of the vacancy front with the applied field. Hur *et al.* proposed an equivalent circuit model based on bipolar Ta₂O₅/TaO_x stack.⁷⁷ According to the model, due to the forming step certain conductive paths are formed inside the material stack and therefore subsequent switching is focused locally near the Ta₂O₅/TaO_x interface. The state variable is the length of the oxygen-vacancy-doped region near the interface. The memristor can be represented by an equivalent circuit with a variable Schottky barrier and variable resistance in series with a constant resistance (R_o) due to the TaO_x layer (Fig. 6(e)). During the LRS ($w = L$), the device current is ohmic, with its resistance dependent on R_{ON} and R_o .

5.3 Tunneling barrier model

Borghetti *et al.*⁷⁸ investigated the electrical transport characteristics of a TiO₂-based memristor as a function of the temperature and reported the device conduction to transit from area-distributed current flow to localized conduction after electro-forming. The model was further developed by Matthew D. Pickett *et al.* considering Simmons tunnel barrier for a rectangular potential barrier with image force effect in the MIM junction.⁷⁹ A conducting channel is formed as a result of the electroforming step, along with a remnant tunnel gap between the conducting channel and the opposite electrode, which can be modulated by applying a voltage and inducing the motion of ionized defects. It assumes that the memristor is a series connection of a resistor (R_s), with an electron tunnel barrier and the width of the tunnel barrier is considered as the state variable (Fig. 6(f)). These tunneling-based models are limited between two limiting values of currents, which makes it suitable for digital applications and also discards the requirement of window functions. The mathematical expressions in these models are considerably complex with no implicit relation between voltage and current. In addition to that, they are not generic in nature.

To address these issues and have a simplified model for circuit simulation Kvatinsky *et al.*⁸⁰ proposed threshold adaptive memristor (TEAM) model, which is a simplified version of

Simmons tunnel barrier model. Here, the relation between current and state variable derivative is polynomial instead of exponential, Yakopcic *et al.* proposed another simplified tunneling-based model, that assumes voltage threshold, and an implicit memristance.⁸¹ It considers two types of electronic conduction represented by two different sin hyperbolic function and controlled by the state variable. In their subsequent work on the same model, these two electronic conductances are developed as an exponential conduction (through a tunnel barrier) during HRS and a linear conduction LRS (Fig. 6(g) and (h)).⁸²

6. Applications and implementation of RS-based memristor

6.1 Nociceptor

A nociceptor is a critical and special receptor of a sensory neuron that can detect noxious stimuli and provide a rapid warning to the central nervous system to start the motor response in the human body and humanoid robotics. It differs from other common sensory receptors with its key features and functions, including the “no adaptation” and “sensitization” phenomena. Nociceptors are present in all the nerve endings of sensory neuron's axon. Whenever any noxious stimuli are received, it alerts the nervous system and the necessary action is taken.

The memristor and nociceptor are analogous as the memristor changes the current rapidly upon surpassing a certain voltage, mimicking the biological nociceptor working while experiencing a pain stimulus. Nociceptor has certain key features, namely “threshold,” “relaxation,” “no adaptation,” and “sensitization”. These features depend on the intensity, duration, and repetition of the external stimuli's rate, respectively.

The nociceptor exhibits a discernible pain recognition threshold, below which it remains unresponsive, while it exhibits a pronounced and swift response beyond this threshold. The threshold for activation is evident at 4 V as illustrated in Fig. 7(b), coupled with a pulse width of 200 ms as demonstrated in Fig. 7(c). Below this specified pulse amplitude and width, the nociceptor remains unreactive.

Following an initiating pulse of 4 V, when subjected to a read voltage of 2 V and a pulse width of 200 ms (Fig. 7(d)), a relaxation time interval is observable. Demonstrating the

presence of “no adaptation” phenomenon involves assessing the current response after a series of 100 pulses at different voltages (3 V, 4 V and 5 V). When employing a pulse width of 20 ms and a pulse interval of 2 ms, the output current displays no plasticity over time. This substantiates the presence of an adaptation response. When a nociceptor, a sensory receptor for pain, is subjected to a strong stimulus, it can become damaged. As a result, it becomes sensitive to stimuli that are either below or above its usual threshold. This sensitivity alteration is referred to as allodynia, where the threshold is lowered, and hyperalgesia, where the response is heightened. This condition transforms the nociceptor into a state of hypersensitivity or damage, rendering it without a clear threshold value. In cases where the nociceptor reacts to stimuli that are normally considered below the threshold, it's termed allodynia, and when it reacts more strongly to stimuli above the threshold, it's termed hyperalgesia (as shown in Fig. 7, panels f–k). Both allodynia and hyperalgesia serve as mechanisms to safeguard the body against harmful stimuli. This phenomenon is illustrated in Fig. 7(i) as the behaviour of a thermal nociceptor. At a lower temperature, such as 40 °C, the nociceptor remains unresponsive (Fig. 7(j)), while at a higher temperature, like 70 °C, the nociceptor responds as if it is encountering a noxious stimulus (Fig. 7(k)).

Humanoid robots, which are well-infested with artificial intelligence algorithms are not only useful in daily mundane tasks but also could be easily deployed to places where humans cannot reach to collect the respective data samples, some examples could be battlegrounds, human unreachable provinces, space exploration missions, *etc.*^{84,85} The tactile sensors in robotics are the sensory organs interacting with the outer environment physically to detect any potential damage. This sensing system consists of two different units, namely the sensor and processing unit of the signals. These units are separate nanodevices that, when combined, create a high density and low energy output. Though the sensors are being scaled down, the processing unit is still a bulky part due to the functions it performs. The memristors can work as a replacement in this system to perform both sensing as well processing functions. These characteristics can be achieved by using a single unit of memristor. Traditional CMOS has reached the limit of improvement in the scaling sector as well as the size.^{86–88} The memristors can be a better alternative to overcome this bottleneck of traditional systems.

6.2 Artificial neuron

Biological neurons send information to the post-neuron through axons after receiving it from the pre-neuron through a vast number of dendrites. Integration and firing are two of a neuron's primary electrical processes.⁹¹ The biological neurons transmit spiking electrical signals that are composed of action potentials. The fundamental mechanism of the action potential was discovered by Hodgkin and Huxley (HH).⁹² It corresponds to a transient response of the transmembrane potential by the concerted action of voltage-gated ion channels. The neurons enter a nonequilibrium state by a Hopf bifurcation⁹³ in which it produces sustained oscillations that form the basis for

computation and transmission of information in the brain. The HH model can be considered as an extension of eqn (1) and (2) for the generic memristor with three internal state variables.^{10,94} A number of simplified models have been discussed in the recent decades.^{95–100}

There are different approaches to build the neurons needed for neuromorphic computation. One is to use a simple “integrated-and-fire” scheme in which an RC element is changed until a threshold is reached. The other, more complex one is to build devices that mimic closely the biological bifurcation mechanisms and produce self-sustained spiking properties. The benefits of each approach for brain-like computation have been analysed.^{101,102} The preferred kind of neuron may depend on the requirements of data and type of computation.¹⁰³ There is great interest in building biology-like neurons by using different materials platforms, such as nano fluidics¹⁰⁴ and organic and inorganic semiconductors.^{105,106}

6.3 Artificial synapse

In the current scenario of data processing systems, the human brain is now thought to be the smartest and fast-thinking operating system. As a result, neuromorphic computing which mimics the functioning of the human brain has been hailed as a promising new type of computer. The human brain is small and uses less than 20 W of power, which is less than what is needed to run an ordinary light bulb. It has 10^{11} neurons and 10^{15} synapses.¹⁰⁷ A neuron is divided into three main parts: cell body, single axon and a dendrite. At the junction between an axon and a dendrite, there exists a specialized micro-level structure called a synapse or synaptic cleft (Fig. 8(a)). In biological synapse, a neuron transmits an electrical signal to the post-neuron by producing an electrical spike known as an action potential. The brain utilizes action potentials as the signals to gather, process, and transmit information. These action potentials carry crucial information within neurons. When an action potential occurs, the neuron responds by producing and storing transmitters within vesicles. These transmitters play a vital role in transmitting information between neurons, contributing to various brain functions and processes. The Ca^{2+} channel is opened when the presynaptic terminal depolarizes, and the vesicles are subsequently released into the synaptic cleft. Synapses are 20–40 nm contact sites between pre-neuron and post-neuron. They attach to the receptor molecules of the Na^+ channel in the postsynaptic membrane after passing through the synaptic cleft. The pre-neuron's spike may be communicated to the post-neuron during this procedure. The ability of synapse to strengthen or weaken over time in response to increase or decrease of activity is termed as synaptic plasticity (Fig. 8(a)). Similarly, in memristor device synaptic plasticity refers to the ability of memristor to change resistance state in response to applied voltage or current that further allows the device to store and retrieve information (Fig. 8(a) – potentiation and depression).^{108–111}

Other synaptic properties of memristors include temporal dynamics, which describes how the memristors resistance changes over time. The magnitude, duration, and frequency

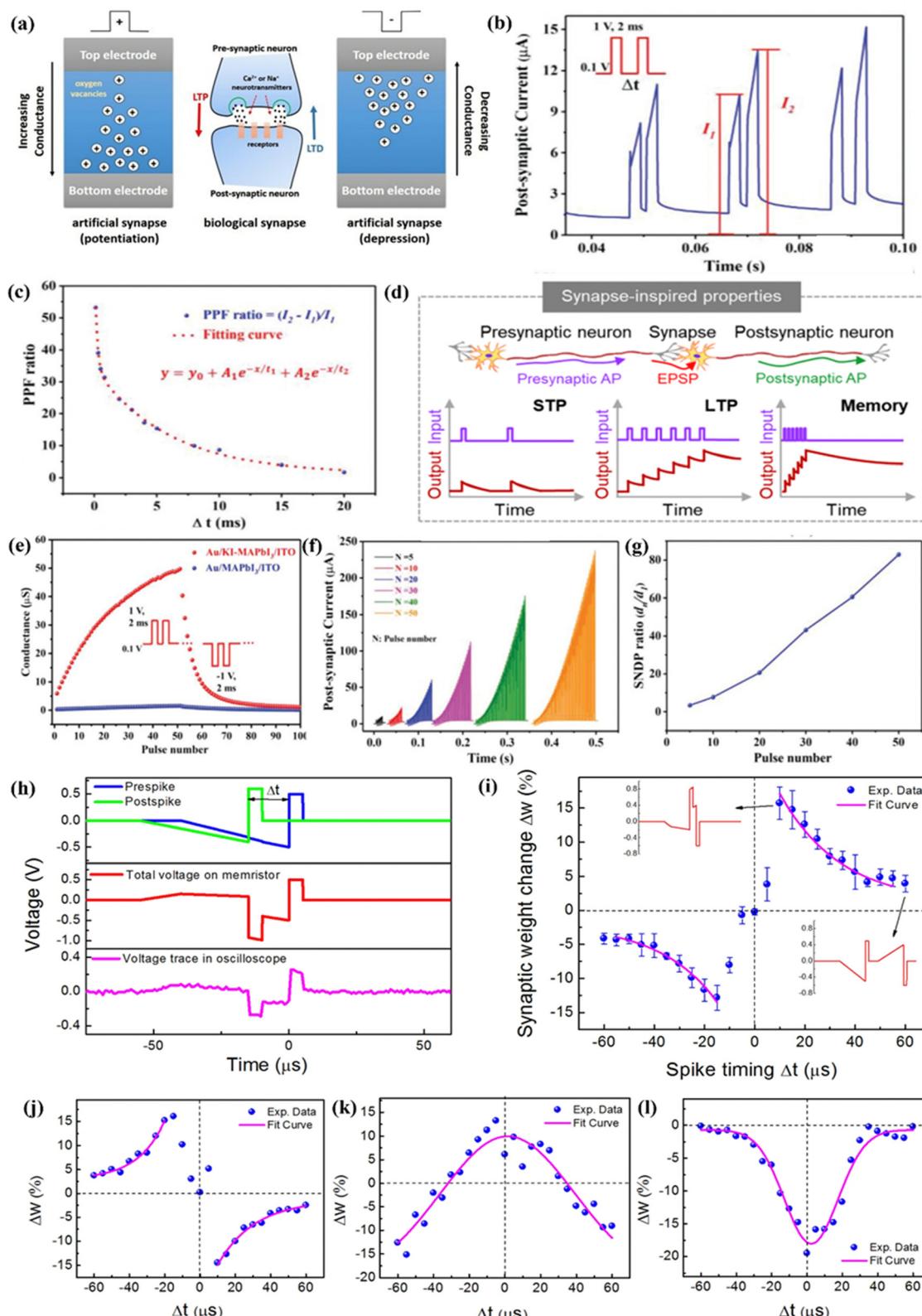


Fig. 8 (a) Shows a schematic of a biological synapse between a presynaptic neuron and a post-synaptic neuron (at centre), left and right a potentiation and depression of artificial synapse based on memristor (b) shows the currents of the memristor in response to an applied voltage pulse (c) figure indicates that the PPF decreases with increasing pulse interval (also named as PPF index). Reproduced from ref. 113 with permission from AIP Publishing, copyright 2013 (d) transition of STP (short term plasticity) to LTP (long term plasticity) with respect to time and pulse interval (e) potentiation and depression (f) SNDP (spike number dependent plasticity): by increasing number of pulse increase observed in postsynaptic current (g) weight ratio vs. number of pulse in SNDP (h) input spikes of STDP (spike time dependent plasticity), (i)-(l) output of STDP curve named as asymmetric Hebbian, asymmetric anti-Hebbian, symmetric Hebbian, and symmetric anti-Hebbian. variation of conductance (%) with respect to the time interval between pre- and post-synaptic neurons reproduced from ref. 121 with permission from PLOS computational Biology, copyright 2013.

of the voltage or current, applied to the memristor can influence its temporal dynamics. In addition, the switching speed, durability, variability, and noise characteristics of memristor can affect its performance. The strength between the pre-synaptic neuron and post-synaptic neuron is modulated by increasing the applied pulse width or by decreasing the pulse interval.¹¹² With a pair of pulses (stimuli) the second post-synaptic current is several times larger than the magnitude of the first. This effect is called paired-pulse facilitation (PPF).¹¹³

The PPF of memristor is defined by the equation:

$$\text{PPF index} = \frac{I - I_0}{I_0} \times 100\% \quad (4)$$

where I_0 and I are the currents of the first and second pulse, respectively. Fig. 8(b) and (c) shows the PPF as a function of the time interval between the paired pulses.

Synapses show two types of plasticity: long-term plasticity (LTP) and short-term plasticity (STP), distinguished by how long the synaptic modifications last. While LTP can last for several hours, months, or even years, STP fades after few minutes.¹¹⁴ Furthermore, STP and LTP are subdivided into short term facilitation (STF), short-term depression (STD) and long-term facilitation (LTf) and long-term depression (LTD), respectively. While short-term plasticity is expected to have a crucial computational role in the processing of spatiotemporal information in biological brain systems, long-term plasticity is thought to be associated to learning and memory processes.¹¹⁵ The short-term plasticity can be accomplished in different memristive devices by taking advantage of the volatility of memristive electronics. According to Chang *et al.*, the WO_3 -based VCM memristors displayed in Fig. 8(d) exhibit short-term plasticity.¹¹⁶ The low stability of the conducting filaments, which tend to dissolve, in such devices ensures short-term plasticity and allows the device to relax towards the insulating state. With relaxation associated with the oxidation-reduction counter process, TiO_2 based VCM devices have been observed to exhibit both potentiation and depression behaviour.

Spike number-dependent plasticity (SNDP) is a type of synaptic plasticity that is dependent on the number of spikes that are received by a postsynaptic neuron. In other words, the strength of the synaptic connection between two neurons can be strengthened or weakened depending on how many spikes the postsynaptic neuron receives. SNDP play an important role in learning and memory.

Spike rate-dependent plasticity (SRDP) refers to the synaptic weight between neurons by firing frequency. The presynaptic spikes with high frequency led to increased synaptic weight resulting in potentiation. While the postsynaptic spikes with low frequency led to a decrease in synaptic weight leading to depression. In between potentiation and depression lies threshold frequency which can be modulated and such tunable SRDP is related to synaptic meta plasticity.¹¹⁷ Wei *et al.* demonstrated SRDP for MXene-based synaptic device.¹¹⁸ The external stimulus of 10 spikes was applied to Ti_3C_2 – MXene synapse which produced a dynamic high pass filter of the signals.¹¹⁹

Spike time-dependent plasticity (STDP) is also one of the key learning mechanisms in biological synapses. In STDP process, the strength of a synapse changes based on the relative timing of the spikes (or action potentials) occurring at two neurons connected by synapse. STDP is widely used in the gradual development of learning and controls the conductivity based on the time interval between pre and post-synaptic neurons.¹²⁰ As shown in Fig. 8(h), the variation of conductance (%) with respect to the time interval between pre- and post-synaptic neurons is caused by varying the spike order and spike interval (Δt) between the two neurons. For the presynaptic spike before the postsynaptic spike, *i.e.*, $\Delta t > 0$. $\Delta w\%$ conductance is positive, indicating the potentiation of synaptic weight while strike of the presynaptic spike after the postsynaptic spike, *i.e.*, $\Delta t < 0$ indicates depression. In 1949, Hebbian suggested this as the basis for learning and memory modelling by mentioning that if an axon is enough to excite another axon and participates in firing it continuously, growth processes or metabolic changes occur in one or both cells. It states the relation of the shifts in synaptic weights ($W(\Delta t)$) upon excitation of synapse with the time intervals ($\Delta t = t_{\text{post}} - t_{\text{pre}}$) of the presynaptic and postsynaptic nerve fires (t_{pre} and t_{post}).¹²¹

$$W(\Delta t) = \left\{ A_+ e^{-\Delta t/\tau_+}, \Delta t \geq 0 - A_- e^{-\Delta t/\tau_-}, \Delta t < 0 \right\} \quad (5)$$

where A^+ and A^- are constants that scale the potentiation and depression strengths, respectively, and τ^+ and τ^- are temporal constants that scale the width of the positive and negative learning windows, respectively.¹²¹ STDP can be achieved using memristive devices by dedicatedly design the pulse width, the number of pulses, or the pulse voltage amplitude.^{122,123} Table 4 summarize the different switching mechanism and synaptic performance based on various device configuration.

6.4 Photonic-based memristor

A photonic-based memristor uses light to control its resistance. It consists of a photonic material, such as a light-sensitive organic polymer or a photosensitive semiconductor, sandwiched between two electrodes. When light is shone on the material, it triggers a photoconductive effect that changes the resistance of the memristor. The use of photonics in memristors has several potential advantages over traditional electronic-based memristors. For example, photonic-based memristors can operate at much higher speeds and with lower energy consumption, making them attractive for use in high-speed computing and communication applications. Additionally, they can be integrated with other photonic components, such as photodetectors and lasers, to create more complex photonic circuits.

Memristors, as photodetectors in the field of photonics, are used to simulate the retina in the human eye for capturing, transmitting, and processing visual information.^{133,134} The formation of visual memory is illustrated by the image sensor and memory unit connected in series with a neighbouring electrode as shown in Fig. 9(a) and (b). The use of ultraviolet light converts HRS of memristors to LRS by increasing the

Table 4 Comparison table of switching mechanisms and synaptic performance for different device structures

Device structure	Conduction mechanism	Type of switching	Operating voltage (V)	Switching time	Retention (s)	P&D (no. of pulses)	Synaptic functions	Ref.
Pt/HfO ₂ , NRs/TiN	VCM	Analog (bipolar)	±4	<100 ns	10 ²	25	STDP, LTP, LTD	124
Au/Mo ₂ C/MoS ₂ /Au	VCM	Analog (bipolar & unipolar)	-3/2.9	>10 ⁴	20	PPF, LTP, LTD	39	
Ag/GeSe/Pt/Ti/SiO ₂	CBRAM	Digital (bipolar & unipolar)	+0.195/-0.36	10 ⁵	50	LTP, LTD, PPF, SRDP, STDP	125	
Au/CuInP ₂ S ₆ (CIPS)/Ti	FeRAM	Analog (unipolar)	±3	>10 ³	70	PPF, PPD, STDP EPSC	53	
Ge ₂ Si ₂ Te ₅	PCM	Analog (bipolar)	±1	500 ns	20	P&D, STDP	126	
Pt/GDC/CeO ₂ /Pt	PCM	Analog (bipolar)	±4	>10 ³	100	STP, LTP	127	
SrCoO _x	PCM	—	—	10 ³	—	LTP, LTD	50	
Pt/NbO _x /Pt	Mott	—	—	10 ³	—	STDP	128	
VO ₂	ECRAM	Analog (bipolar)	±1	—	—	SRDP, LTP, LTD, STDP	129	
ITO/ZnO/ZSO/ITO	ECRAM	Analog (bipolar)	+1.22/-1.3 V	—	—	LTP, LTD, STDP	58	
Pt/HfSiO _x TaN	ECM	Analog (bipolar)	+1.5/-1	—	—	PPF, SRDP, LTP	130	
Ni/PZT/LSMO	ECM	Analog (bipolar)	±4	100 ns	>8 × 10 ⁴	—	—	
Cu/Ti/MoS ₂ /Al ₂ O ₃ /Au	ECM	Analog (bipolar)	0.33 V/-0.22 V	<100 µs	>600	—	—	
					50	—	—	131
						—	—	132

partial current due to the decreased resistance of the image sensor (photodetector). Identifying the recorded image after the light has been turned off can take up to a week, and the data can be reset by applying a negative voltage.¹³⁵

In-memory computing of the future will use electrical and optical signals as inputs and device current as output in logic gates, so novel memory that integrates with other functions, such as arithmetic and demodulation, is a crucial building block.¹³⁶ On top of the fact that photonic memristors can have their memory characteristics tweaked, this is a significant advantage. Two light sources (blue and green) along with wavelength and light intensity could reach four memory states in ITO/CeO_{2x}/AlO_y/Al devices with the physical mechanism, allowing for the storage and transmission of information in 8-bit codes.¹³⁷ The linear relationship between photocurrent and mathematical operations such as adding machines and counters. Simple integration of memory and logic operations is a helpful method for reducing system complexity in integrated circuits. When 'X' and 'Y' patterns are input into a 5 × 5 device pattern, as shown in Fig. 9(c), the output patterns of the same region (AND gate) illustrated in Fig. 9(d), and the output pattern with all parts (OR gate) exhibit in Fig. 9(e).¹³⁸

However, the development of photonic-based memristors is still in the early stages, and many technical challenges must be overcome before they can be widely used. Some of the challenges include improving the reliability and stability of the devices and developing practical methods for integrating them into existing electronic and photonic systems.

Optogenetics is a novel technique that has been developed in recent years and has found widespread use in neuroscience due to its high temporal resolution. Optogenetics is the study of how light can be used to control the activity of individual neurons. In Fig. 9(f), we see the corresponding muscle response of natural and artificial synapses to the external stimulus of light.^{139,140}

6.5 ANN implementations for AI

In this section, a brief description is given of the implementation of these memristors to perform neuromorphic computing tasks in ANN. ANN are a network of nodes that are known as artificial neurons. Several models of these neurons were proposed^{142–144} historically. These neurons are basically connected and thus form an ANN. The operation of this neural network is governed by neuronal dynamics. Neuronal dynamics can be categorized into two parts, one related to the dynamics of activation state and the other related to the dynamics of synaptic weights. Based on this, different learning rules were formulated that govern the working of neural networks. These learning laws, come into play when weights at each node in the neural network are updated with the input data, output data, or both simultaneously. If the learning is supervised,^{145,146} the neural network is fed with the known data based on which weights of each node are updated, and the trained neural network with this data is used to get output for unencountered situations. The learning can also be unsupervised,¹⁴⁷ which utilizes concepts from statistics like correlation among

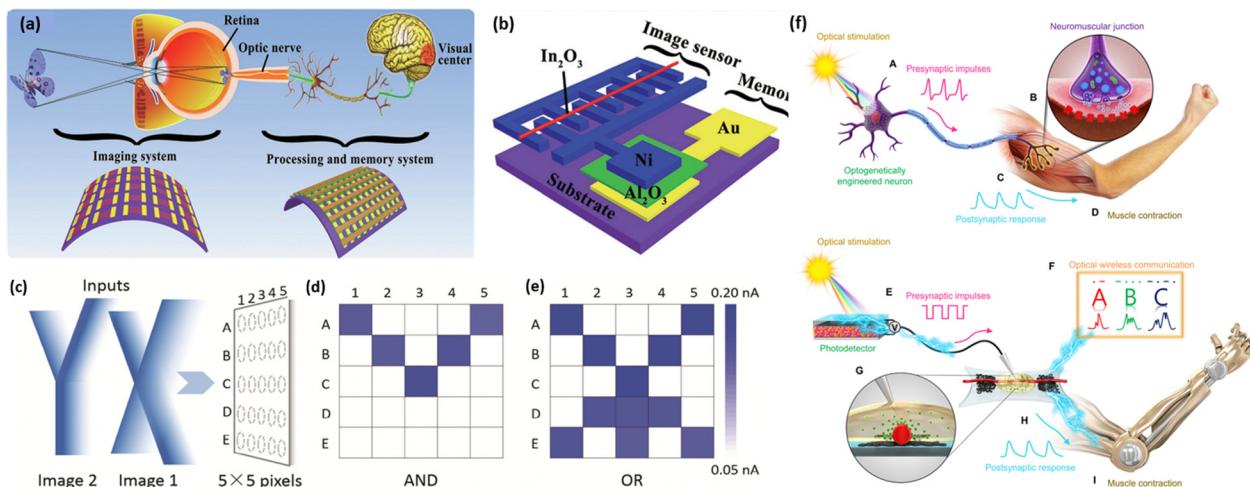


Fig. 9 Photonic-based applications of memristor devices: (a) schematic illustrations of imaging and memory system corresponding to human visual memory (b) schematic illustration of the bioinspired visual memory unit integrated by image sensor and resistive switching memory device reproduced from ref. 135 with permission from John Wiley and Sons, copyright 2018. (c) Patterns "X" and "Y" fed into the memlogic devices; output sketch of (d) the same regions (AND gate) and (e) all the parts of both input patterns (OR gate). Reproduced from ref. 138 with permission from American Chemical Society, copyright 2017. (f) Biological and artificial synapse under optical simulation and the corresponding muscle response. Reproduced from ref. 141 with permission from Elsevier, copyright 2018.

different columns of data or update weights by the output of the neural network with a given activation function. Because most real-world situations modelling is nonlinear in nature, the neural networks used these days for a variety of use cases comprise the number of hidden layers sandwiched between an input layer and an output layer. Also, most of these neural networks are feedforward in nature which means the weights at each node in hidden layers are updated by the input. However, one can train their model by the output through back-propagation, which allows one to calculate the error attributed to each of the nodes in the hidden layer, allowing us to fit the parameters that define the predicted model accordingly. These neural networks are utilized in nearly every area, ranging from ship traffic on waterways,¹⁴⁸ which utilizes a more advanced graph neural network to most recent use of them in tasks like natural language processing, *etc.* With this, it becomes of paramount importance to find a solution to overcome the bottleneck of memory and inefficiency in the real-time data processing.

6.6 Data storage

Memristor devices specifically non-volatile in nature can be employed for data storage applications. Owing to their extraordinary qualities such as low power consumption (\sim femtojoule/bit), simple and cost-effective device fabrication techniques, quick switching response (\sim picosecond time scale), high scalability (\sim nanometre scale) memristor devices hold potential to meet the future demands of high density as well as long term data storage.¹⁴⁹

Among all the possible applications of memristor devices one of them is it can be used as a replacement of traditional hard disk drives as it can comparatively store data at higher density, also reads and writes faster. Memristor retains data for

longer period of time without power and can read it whenever required therefore it can also be used in archival storage such as tape storage. In solid-state drives (SSDs) memristor can be used instead of NAND flash memory to significantly increase the storage density and reduce the power consumption. In 2011, Kim *et al.* demonstrated a high-density, fully operational, vertically integrated hybrid memristor system with the device structure consisting of W/SiGe stack, an amorphous Si layer and Ag layer acting as the bottom electrode, a dielectric layer and top electrode respectively.¹⁵⁰ Fig. 10(a) and (b) show the SEM image of this 40×40 crossbar array and the corresponding $I-V$ switching characteristics from 10 different cells in the crossbar array, respectively. Binary bitmap images were successfully stored and retrieved with considerable read margin with the help of this device (Fig. 10(c)).¹⁵⁰

Hybrid perovskites are widely explored for optoelectronic applications due to their unique properties, including high carrier mobility, and tunable bandgap.^{152–155} The presence of ion migration and high dielectric constant enable hybrid perovskites for next-generation memory devices.¹⁵⁶ Several types of memory devices have been developed using hybrid perovskites, including ReRAM and ferroelectric memory. In ReRAM, hybrid perovskite materials are used as the switching medium to control the resistance state of the device.^{153,157–160} The resistance state is determined by the formation and rupture of conductive filaments within the hybrid perovskite material. Hybrid perovskite ReRAM devices have demonstrated high on/off ratios, low power consumption, and fast switching speeds, making them a promising candidate for future memory applications. Recently, Poddar *et al.* demonstrated a highly dense and ultra-fast memristor in the form of a flexible 8×8 crossbar array. The schematic and the photograph of the fabricated crossbar, the schematic of alphabetic data storage

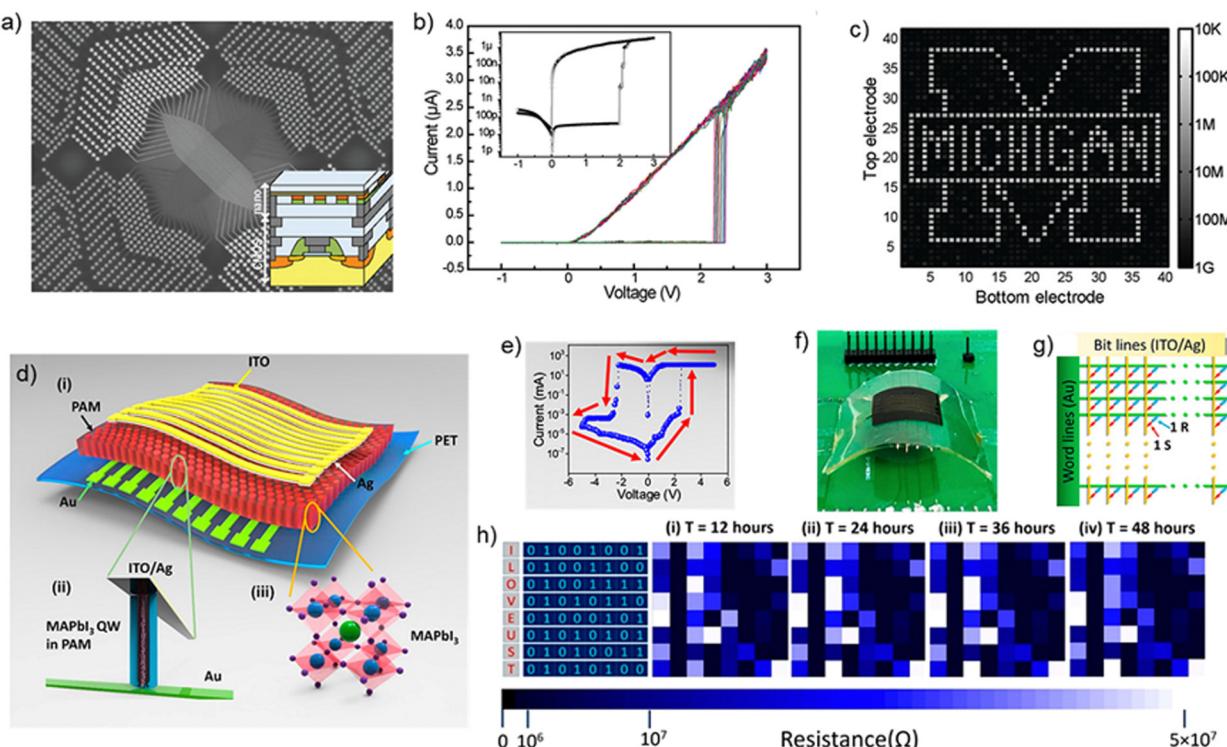


Fig. 10 (a) SEM image of a crossbar array based on two-terminal resistive switches (W/SiGe/a-Si/Ag), insets: the schematic of the vertical integration of the crossbar array with the on-chip CMOS circuitry, (b) I – V switching characteristics from 10 different cells in the crossbar array. Insets: I – V characteristics in log scale, (c) storage of 40×40 bitmap image representing the University of Michigan logo. Reproduced from ref. 150 with permission from American Chemical Society, copyright 2012. Device structure, photograph, and equivalent circuit of the QW memory device. (d) (i) Schematic showing the MAPbI_3 QWs/NWs in the PAM stacked between the crisscrossing Ag/ITO and Au finger electrodes on PET substrate. (ii) An individual QW comprising the Ag filament, (iii) crystal structure of MAPbI_3 , (e) I – V characteristics of a long QW Re-RAM device, (f) photograph of the flexible QW memory device, (g) equivalent bitline–wordline circuit of the ITO/Ag/QW/Au and the selector, shown in red (MIM formed by Ag/ Al_2O_3 /Au), connected in series with the perovskite QWs in LR and (h) schematic of alphabetic data storage and corresponding temporal retention of data. Reproduced from ref. 151 with permission from American Chemical Society, copyright 2021.

in the 8×8 array and the corresponding temporal retention of data are shown in Fig. 10(d)–(h). The devices exhibited a high ON/OFF ratio of $\sim 10^7$, ultra-fast switching speed of ~ 100 ps, long retention time of over 2 years and high endurance of $\sim 6 \times 10^6$ cycles.¹⁵¹ While hybrid perovskite-based memory devices have shown promising results, challenges remain in terms of device stability and reliability, scalability, and integration with existing semiconductor technology. Nevertheless, ongoing research in this area is expected to advance the development of hybrid perovskite-based memory devices, and further improve their performance and commercial viability.

6.7 Bio-voltage memristor

Bio-voltage memristors are a type of memristor that operates at the same voltage levels as biological systems. This makes them well-suited for applications in bioelectronics, such as brain–computer interfaces and drug delivery. The voltage levels at which bio-voltage memristors operate are similar to the action potentials of neurons. This makes them well-suited for use in brain–computer interfaces, which use electrical stimulation to communicate with the brain. Electronic devices that record very small signals (sub-100 mV range), such as wearable sensors and intracellular biological probes, must be linked to communication

amplifier circuits for amplification before signal processing. This pre-processing procedure will result in higher power requirements for closed-loop bioelectronic devices.^{161,162} Bio-voltage memristors might immediately offer the possibility of processing bio-signals, in contrast to technical methods that capture physiological data with high precision, answering the needs of bio-energy-saving systems and requiring less integration. Additionally, by combining sensors with memristor-based artificial neurons to create a front-end afferent circuit and a back-end execution system, wearable neuromorphic interfaces are provided that are capable of processing bio-stimulation effectively and intelligently to produce intelligent responses.^{163,164} Fu *et al.* reported a fully sensor-driven, integrated neuromorphic system by achieving signal match at the biological level, which is composed of a protein nanowire memristors, an electric energy harvester, and an electronic sensor. The flexible memristor can be driven by sub-100 mV signals, enabling bio-amplitude neuromorphic circuits and signal processing. The device schematic, the multilevel switching characteristics, and device yield and forming voltage with various bending times are shown in Fig. 11(a)–(c). Notably, the typical sensing signal's intrinsic amplitude mismatch with the computation signal makes wearable integrated interfaces at the biological level inappropriate.¹⁶⁵ In order to integrate sensing and computation

processes in biological systems, bio-voltage signal processing is essential. The experimental results for dynamic response in the neuromorphic interface are consistent with the simulation predictions, as can be seen from the published literature, demonstrating the enormous potential of bio-voltage memristors in upcoming self-sustaining wearable neuromorphic interface applications. A resistive memory based on exfoliated 2D perovskite single crystals was reported by Tian *et al.* that exhibited a program current as low as 10 pA. Owing to this extremely low operating current, the energy consumption is only 400 fJ per spike during the synaptic characterization, which is very close to that of biological synapses of 1–100 fJ per spike. The switching mechanism in this artificial synapse is Br⁻ ion movement in 2D perovskite, which mimics the Ca²⁺ ion movement in a bio-synapse (Fig. 11(h)).¹⁶⁶

6.8 Organic protonic memristor

The exploration of protonic modulation in the realm of organic protonic memristors signifies a significant breakthrough in neuromorphic computing.^{167,168} The study's emphasis on utilizing

protons as the primary modulating ions presents a compelling advantage over other ions, particularly in their ability to operate within the approaching zero-power limit. This distinguishing feature holds great promise for advancing artificial synapses and neuromorphic systems, addressing critical energy efficiency concerns. The incorporation of a proton-reservoir organic molecule, 4,4',4'',4'''-(porphine-5,10,15,20-tetrayl) tetrakis(benzene-sulfonic acid) (TPPS), in memristor construction showcases innovative thinking in material design.¹⁶⁹ The synthesized molecules, with proton-donating sulfonic acid and proton-accepting amino groups, contribute to the unique characteristics of the resulting memristors. The demonstrated sequential proton migration and interfacial self-coordinated doping highlight the intricate processes enabling effective and non-volatile modulation of device conductance over a wide range of states. A standout aspect of protonic modulation is its achievement of ultra-low power consumption, ranging from 16.25 pW to 2.06 nW for modulating device conductance and 6.5 fW to 0.83 pW for reading. This near-zero-power operation is a key factor for practical implementation,

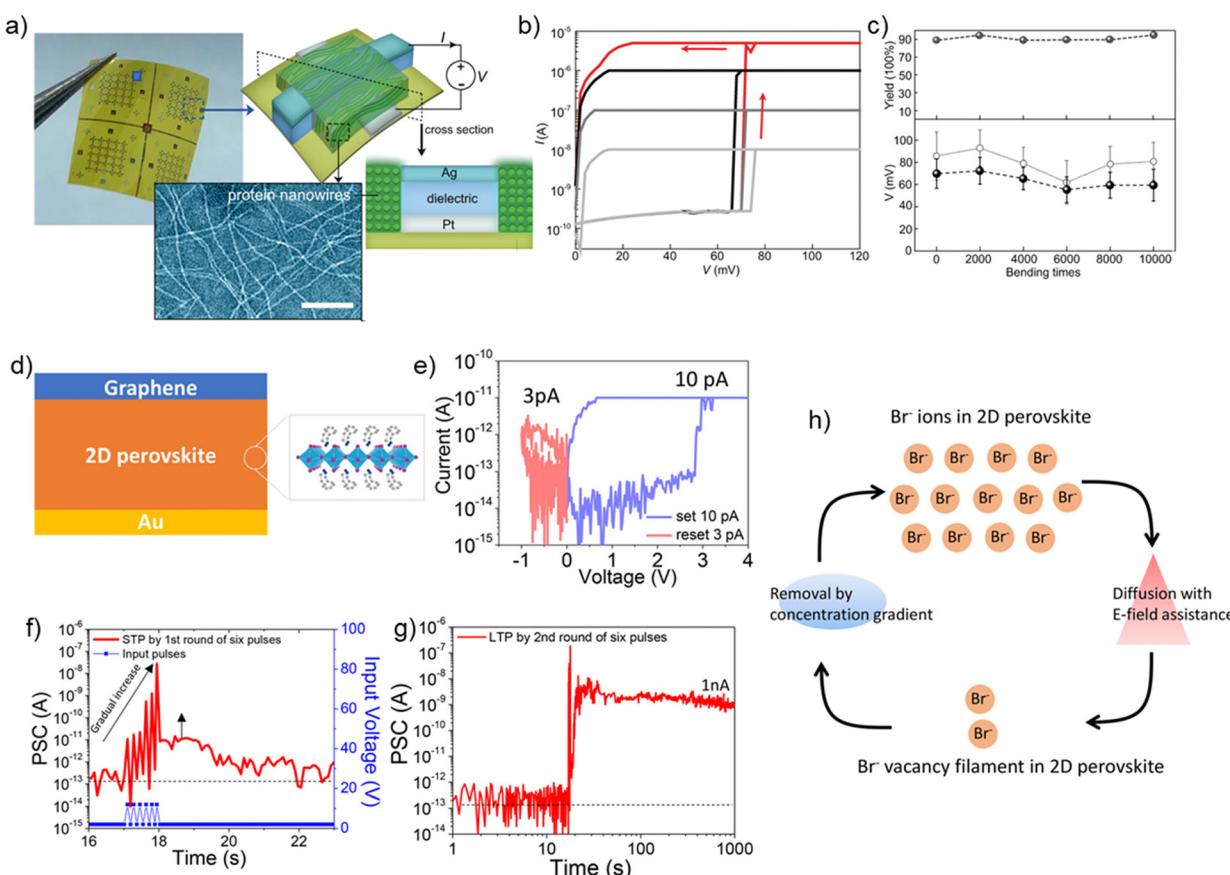


Fig. 11 (a) (left) Image of a protein nanowire memristor array on a polyimide (PI) substrate and (right) the schematics of the device structure. (bottom) TEM image of protein nanowires, (b) multilevel switching I – V characteristics of the memristor with different current compliance, (c) device yield (top), threshold switching voltage (black, bottom), and forming voltage (gray, bottom) in protein nanowire memristors subjected to various bending times. Reproduced from ref. 165 with permission from Springer Nature, copyright 2021. (d) Schematic diagram of a graphene/2D perovskite/Au structure and the 2D layered structure of (PEA)₂PbBr₄ perovskite, (e) corresponding I – V characteristics indicating extremely low operating currents, (f) and (g) synaptic characteristics obtained from the 2D perovskite memristor, (f) STP by a first round of six pulses, (g) LTP by a second round of six pulses, and (h) working mechanism schematic of the artificial synapse showing the Br⁻ ion movement in 2D perovskite which mimics the Ca²⁺ ion movement in a bio-synapse. Reproduced from ref. 166 with permission from American Chemical Society, copyright 2017.

especially in energy-sensitive applications. Overall, the research signifies a crucial step forward in the development of energy-efficient and high-performance molecular neuromorphic systems, leveraging the unique properties of protons for enhanced artificial intelligence applications.

7. Current state of art

In recent years, the memristor technology is expected to replace CMOS for realizing neuromorphic computing to obtain high-volume data processing ability. This review summarizes the progress of representative memristors from three aspects: working mechanisms, artificial synapse and neuron functions, as well as novel applications. We focused on the detailed analysis of physical mechanisms of various types of RS including ion migration, phase transition, and charge trapping/detrapping which provides an understanding of the origin of the memristive behaviour for advanced applications. In addition, memristors successfully emulate typical artificial synaptic functions with STP, LTP, and the transition from STM to LTM, which are the foundations for building efficient ANN for novel neuromorphic computing systems. Last, the applications of bio-voltage memristors in computing and bioelectronic neuromorphic interface application prospects are introduced. Despite research on biological voltage memristors having made phased progress, there are still some obstacles to overcome to realize long-term stable and effective bioelectronic interactions.

In terms of device mechanism, more thorough research is needed to fully understand how the actual workings of memristor devices relate to their performances and, consequently, to their most practical uses. Additionally, memristors have highly non-ideal properties like fluctuation, noise, and drift between devices and operation cycles, which restricts the overall ANN's ability to operate at a lower standard of efficiency. As a result, it's important to boost each device's performance from cycle to cycle and from one to another.

Future connections between electronic devices and biological neural networks will depend on the use of artificial synapses and neurons. To achieve low-power artificial synapses (STDP and SRDP), large-scale bio-compatible ANN must take all pertinent factors into account. In terms of modulating synaptic conductance, the actual memristors are typically nonlinear and asymmetric.^{170,171} There are now a few studies on the sensing properties of memristor, which need more research.

Applications are built on the integration of memristors on a large scale. The key element limiting the scale of integration in the cross-bar array is crosstalk. The sneak route issue of the cross-bar array may be effectively suppressed and the integration can be improved by integrating the transistor with memristor. However, it appears that memristor applications are harmed by relatively low set and reset voltages. Therefore, the key to future study will be how to implement the integration of bio-voltage memristor and bio-voltage transistor to fulfil the voltage matching.

8. Summary and outlook

In this comprehensive review, we have meticulously examined a spectrum of categorized resistive switching mechanisms, shedding light on the intricate dynamics inherent to these devices. Although resistive switching devices feature a straightforward two-terminal design, they exhibit intricate internal dynamics influenced by a combination of physical and chemical mechanisms. Based on the resistive switching mechanisms, diverse applications of such devices have been reviewed. Regardless of all the encouraging outcomes to date, there are still several obstacles to actual commercial application. For applications relying on online learning, the reliability and efficiency of machine learning applications can be greatly impacted at the device level by differences across device to device and cycle to cycle as well as non-linear and uneven conductance changes. Consequently, it becomes imperative for researchers and engineers delving into the realm of devices and materials to cultivate a profound understanding of the underlying physical processes, thereby enabling more precise fine-tuning strategies for the realization of scalable devices with enhanced performance.

Conflicts of interest

The authors have no conflicts to disclose.

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