PCB Reverse Engineering Using Nondestructive X-ray Tomography and Advanced Image Processing

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***Abstract*— Reverse engineering (RE) of electronic systems is performed for many different reasons, including, but not limited to, failure analysis and fault isolation, obsolescence management, proof of IP rights infringement, security assessment, development of attacks, and counterfeiting. Regardless of the goal, it is imperative that the community understands the requirements, complexities, and limitations of RE. Traditional RE is based on a destructive process of serial sectioning followed by imaging, which is time-consuming, expensive, and error-prone. However, with the advent of advanced characterization tools and imaging software, this is starting to change. In this paper, we introduce a nondestructive approach for printed circuit board (PCB) RE based on X-ray tomography. The imaging parameters for a successful tomography are explained in detail and combined with advanced 3-D image processing and analysis to automate RE, thereby lowering the associated time and cost. We demonstrate our proposed process on two PCBs, a four-layer custom designed board, and a more complex commercial board. Lessons learned from this effort can be used to both develop advanced countermeasures and establish a more efficient workflow for instances where RE is unavoidable.**

***Index Terms*— Nondestructive imaging, reverse engineering (RE), X-ray tomography.**

I. Introduction

REVERSE engineering (RE) of electronics provides both a reassurance and concern for industry, government, and modern society. Electronics are the driving force of today's critical systems in transportation, energy, communication, health, defense, and more applications. A failure could have catastrophic and, in some cases, even life threatening consequences. Globalization of integrated circuit (IC) and printed circuit board (PCB) industries has resulted in well-documented concerns such as counterfeiting, piracy, and hardware Trojan insertion [1]–[5]. For such instances, RE represents an important tool for validating the performance, quality, authenticity, and integrity of electronics. Similarly, many of the critical systems and infrastructures (planes, trains, defense systems, etc.) in use today are decades old. Maintaining them requires electronic components that are no longer available. For example, the original component manufacturer may no longer exist, the original design files may be lost. Replacing or redesigning the entire system may be too time-consuming or expensive. Once again, RE is the answer. Through it, one can study the particular component in order to reproduce it and replace it in the legacy system.

On the other hand, RE can be responsible for as many threats as solutions. While it is perfectly legal to use RE to analyze the features of a competitor's product, some do not stop there. RE can be used to generate unauthorized clones of an IC or PCB. If sold under the same name, there is no telling what environment the clones are manufactured and tested in, which could ultimately result in failures that harm the original IP owner's reputation. If such clones are sold under another name, this can seriously undercut the profit of the original IP owner who invested the time, money, and effort in developing the design. As another example, there can be serious repercussions on national security if military systems are captured and reverse engineered. RE can be used to not only copy such systems, but find weaknesses and develop attacks to cripple them [6], [7]. These arguments for and against the benefits of RE can go on forever. However, regardless of the goal, it is more important to understand how RE is performed and its challenges. Such knowledge could be used to lower the time, cost, etc., when RE is used with positive intentions. Alternatively, it could be used to prevent RE altogether.

In this paper, we focus on PCB RE. A PCB is a laminated, nonconductive material that connects electronic components via conductive copper traces. Electronic components and chips are mounted on the board and are electrically interconnected with these traces. The board might be single or multilayered, depending on the complexity of the system. If there are multiple layers, then vertical interconnects called vias are also part of the PCB. To perform RE, one begins by analyzing the outer layers of the PCB to find the components mounted on it, its traces, and its ports. Many systems are now composed of commercial-off-the-shelf components and the information recovered through this step can be enough to build a clone (albeit some additional steps may be needed to re-engineer any on-chip firmware).

Once the outer information is known, one needs to determine the traces internal of the PCB to recover its overall netlist. The internal structure can be obtained destructively or nondestructively. Destructive methods are more common, and consist of inexpensive, off-the-shelf and state-of-the-art technologies to expose each layer separately for optical imaging. The delayering process is mostly manual and requires careful monitoring. Different polishing techniques using chemicals or mechanical tools expose each layer [8]. Although many labs and companies are pursuing destructive RE, there is much less effort devoted to nondestructive PCB RE. Nondestructive RE

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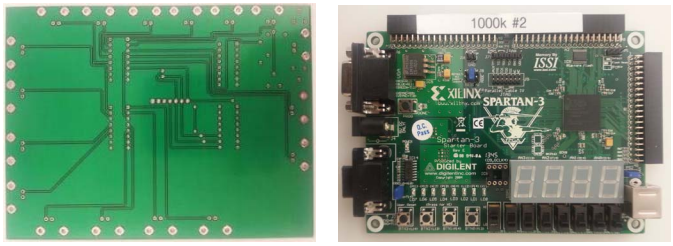


(a) (b)

Fig. 1. (a) Four-layer custom board. (b) Commercial Xilinx Spartan-6 starter board.

would come in handy for a variety of reasons. Aside from saving considerable time and labor, the PCB itself would be unharmed. For legacy systems where there are few samples to begin with, a nondestructive approach is ideally desired. In addition, if one wants to detect a counterfeit PCB or Trojan inserted in the PCB, one would need a nondestructive approach so that it could be still used once it is verified. This would be impossible to achieve with a destructive RE approach [9]–[11].

In this paper, we use a 510 Versa X-ray tomography machine to demonstrate an automated workflow for PCB RE. Our description includes in-depth details of how to tune the X-ray tomography parameters, perform image processing, and segment the data to extract trace information. Tuning the tomography parameters is an important process since it is related to the total speed of tomography and the quality of the results [12]–[14]. Partially destructive refers to the fact that components must be removed from the board in order to reduce the noise level in the tomography images. The process itself is both fast (1.5 h/tomography) and partially nondestructive. Compared to traditional destructive methods, where serial sectioning is required, this method is also repeatable and more amenable to automation. We illustrate our technique on a small custom PCB first [see Fig. 1(a)] as a proof of concept. Then, the same scanning process is applied to a six-layer commercial Xilinx Spartan-6 starter board [shown in Fig. 1(b)]. Note that while the Versa 510 machine source is used to demonstrate our approach, other systems such as GE Vtom and Skyscan 2211 have also been tested and can generate similar results (not shown).

The remainder of the paper is as follows. We present the X-ray imaging details in Section II. In Section III, we discuss the image stitching process required to recover the entire PCB. Section IV describes postprocessing operations such as image segmentation and filtering. We summarize the lessons learned in Section V and present the conclusion in Section VI.

II. Nondestructive 3-D Imaging

Tomography and laminography are noninvasive imaging techniques to visualize the internal structure of an object without interference from occluding structures. Laminography has more flexibility to acquire images of large flat samples, when the risk of collision is much higher in tomography. It also helps to zoom in and directly acquire high resolution images from a specific area on such samples, without any interference or attenuation of X-rays through other particles. This is due to the fact that source and detector are not located in a straight line in laminography. While laminography has some advantages as described above, researchers are still trying to improve the 3-D image reconstruction algorithms for laminography and results are not yet comparable to tomography [15]. Hence, in this paper we choose micro X-ray computed tomography primarily due to its advantages in reconstruction algorithms. X-ray tomography offers the ability to extract the geometrical information of traces, via holes and connections on PCB layers. This is not possible using traditional 2-D X-ray systems that do not possess the imaging, stage stability, computation for reconstruction, etc., to extract 3-D images. Note that all PCB layers (front, back, and internal) can be captured in a *single imaging session* using tomography.

A. Optimizing Image Acquisition Parameters

In tomography, a stack of 2-D images is acquired as the sample rotates. Mathematical algorithms such as direct Fourier transform and center slice theory [16] are applied in the next step to reconstruct a 3-D image. The 2-D projections are collected from many different angles depending on the feature size and required image quality. The object properties, such as its dimension and material density, are important to consider in selection of the tomography process parameters. The parameters include the following.

1) *Source Power:* This is correlated to the X-ray energy and amount of penetration.
2) *Detector Objective:* This determines the field of view and the resolution range.
3) *Filtering:* This controls the dose that blocks low energy X-rays and transmits only high energy X-rays to penetrate into the object, which is also called physical beam hardening.
4) *Distance of Source and Detector From Sample:* This is inversely proportional to the number of transmitted X-rays.
5) *Number of X-Ray Projections:* This identifies the angular steps as the sample rotates.
6) *Exposure Time:* This is linearly related to counts and determines the total time and, consequently, the cost of scanning.

These parameters can affect the pixel size and signal-to-noise ratio, which must be optimized based on the region-of-interest. Internal and external structure can be analyzed when the 3-D image is reconstructed, which needs center shift correction (to align source, stage and detector in one perfect straight line to make sure there is minimal movement) and beam hardening tuning (to remove low energy X-rays from the spectrum and reduce noise using only high energy X-rays for imaging) [12], [17].

B. Tradeoff Between Pixel Size and X-Ray Counts

The most critical parameter for defining the quality of 3-D reconstructed images is the pixel size. Many other parameters such as distance to the sample (geometric magnification) and detector objective (similar to optical magnification) can be tuned based on the pixel size. To use both magnifications effectively, one has to optimize all the parameters simultaneously. Thanks to a near-ideal point source technology for X-ray

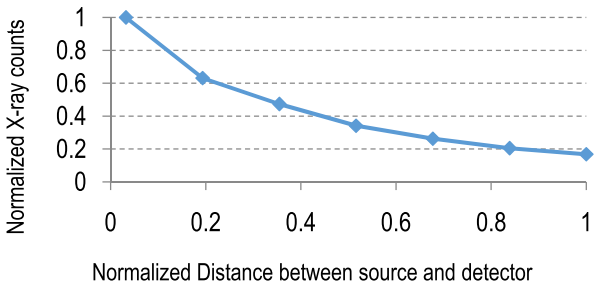


Fig. 2. X-ray counts relation with respect to the distance between source and detector.

systems, the detector and source can be moved toward or away from one another to change the pixel size while keeping the same image resolution. Geometrical magnification can help to decrease pixel size by a factor of 10 in addition to the magnification offered by the detector, which is yet another parameter to tune.

Using the combination of both magnifications, one can choose any value between 0.3 and 62 μm for pixel size. Each detector has a specific number of pixels (an array of about 1000 $\times$ 1000), which defines the field of view for imaging. However, there is a tradeoff between pixel size and image quality. Smaller pixel size demands the detector to be positioned relatively far from the source, thus reducing the number of X-ray counts (number of X-ray photons that can pass through the sample and reach the detector). Based on the principles of wave propagation, wave power is inversely proportional to square of distance from the wave source. In order to get a clear image, one has to obtain 2-D projections with more than 5000 X-ray counts. Therefore, to maintain such X-ray count values, the exposure time and total scanning time must be increased. In addition, the window size decreases with a smaller pixel size.

More details for effecting parameters on X-ray tomography are out of the focus of this paper and are explained elsewhere [12]. Fig. 2 shows the relation between the measured detector distance and X-ray counts as it moves back. The values for distance and X-ray counts are normalized based on the maximum value for each to better show the behavior of these two parameters. Our X-ray system is equipped with the technology of resolution at a distance, which enables high-resolution X-ray tomography on large samples. As shown in this figure, more than 30% of X-ray counts reach the detector when the distance between source and detector is about 70% of the max distance (110 cm). This value is enough to collect a good 2-D projection.

A four-layer custom board is first used as a proof of concept for our tomography on PCBs and to tune process parameters. Then, the same process is reapplied for RE on a commercial Xilinx Spartan-6 starter board. Both PCBs are shown in Fig. 1(a) and (b), respectively. To make sure that we can see features on the board, we have selected a fine pixel size which gives us enough image quality. The values presented in Table I are selected after several rounds of optimization for tomography. This optimization is a nontrivial process, where each of the six tomography parameters (source power, detector objective, filtering, distance of source and detector

TABLE I
X-RAY TOMOGRAPHY PARAMETERS FOR PCB

Tomography parameters	Scan
Pixel size (μm)	49.2
Window size (μm)	49520
Detector	4X
Source distance (mm)	204.2
Detector distance (mm)	80.1
Exposure time (s)	1.2-7.2
Number of projections	1201
Total tomography time (hr)	1.5

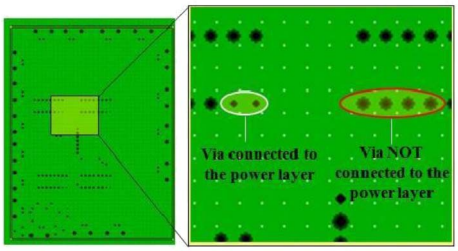


Fig. 3. Layout of an internal layer.

from sample, number of X-ray projections, exposure time) will be tuned to make sure the X-ray transmission value is between 20% and 35% and X-ray counts must stay between 5000 and 60 000 to perform a successful tomography [13], [17].

As discussed above, the tomography window size has a direct relation with the pixel size. The detectors on the X-ray machine have an array of 1000 $\times$ 1000 pixels. This will give us an area of about 5 $\times$ 5 cm for each 2-D image, with the parameters in Table I. In order to do a complete tomography on the custom board (size: 10 $\times$ 15 cm) in one session, a raster scan is performed on six different areas to cover the entire board. Similarly, 12 raster scans performed to scan the Xilinx PCB. Once the parameters are set for the tomography, scanning will be started to acquire all the projections. Later, each of the raster scans will be stitched together. Note that the same process and a very similar set of parameters should be widely applicable to most PCBs.

C. Custom Board Tomography

For the four-layer custom board [Fig. 1(a)], all traces, connections, and via holes can be captured as seen in Figs. 4 and 5. In order to check the effectiveness of the tomography the results are compared to the board design files previously used to print it. The board includes a front side, a backside, and two internal layers. The internal layers correspond to power and ground. Vias go through the entire board and act as vertical interconnects to connect different layers of the board. Vias may connect traces on the top layer to the bottom layer, or external layers to power and ground. The power layer with vias connected and not connected is shown in Fig. 3.

The 3-D image of the board is reconstructed by combining thousands of virtual 2-D slices. These slices can be viewed and analyzed separately. The thickness of each of them is the same as the pixel size (approximately 50 μm). In Fig. 4, one slice is demonstrated, which shows the information about the

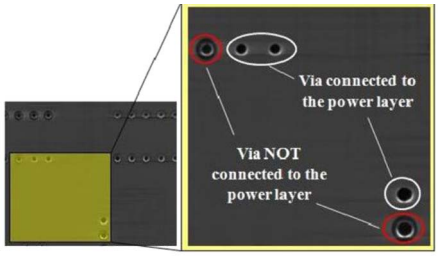


Fig. 4. Virtual slicing of internal layer.

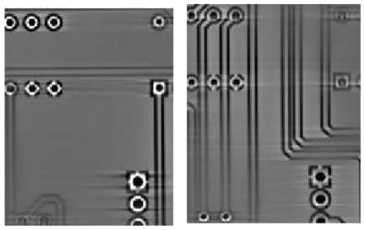


Fig. 5. Reconstructed (a) top and (b) bottom layers.

internal power layer. Obviously, a better resolution or smaller pixel size will give us better image quality, which can result in an easier image processing effort. However, one also has to consider that a better image will increase the costly X-ray scanning time and data size.

Comparing the design layout of the board and the imaging results (in Figs. 3 and 4), one can see a clear difference between the via holes that are connected and those that are not connected to the internal layer. The soldering material, which provides connection of the via holes to the layer has high density and results in white contrast for the pixels. On the other hand, when there is no soldering material and no connection, the isolating material between the via hole and the layer has lower density and results in dark contrast for the pixels. The same principle will let us detect the traces on the side layers of the board due to the attendance of copper on the traces as shown in Fig. 5.

D. Xilinx Spartan-6 Board Tomography

The tomography process as described in Section III-C reveals the internal structural information about a PCB. In the next step, a more complex commercial PCB, Xilinx Spartan 6, is scanned and reverse engineered.

This is a six-layer PCB with considerably more traces and more connections between layers. Note that the same tomography parameters as in Section III-C are used for this PCB. Twelve areas were scanned based on the PCB and scanning window size, which resulted in 18 h of tomography for whole PCB. In our first imaging attempt, the board was scanned with all the components mounted on it. Most of the components such as resistors, plastic switches, and ports are low Z material in the periodic table, which do not cause any effect during the scanning process. However, there were also some of elements such as soldering material and metal ports, which created artifacts in the reconstructed images as seen in Fig. 8(a). These artifacts appear as noise in the image and can make it difficult to set up an automated reconstruction process. In order to solve this problem, we detached the components from the board using a hot air gun. The soldering material was melted down during this process and imaging was repeated with better results.

III. Image Stitching and Reconstruction

The area of the PCB is much larger than the field of view of a single tomography. Yet, multiple imaging sessions increases the time and cost associated with imaging and also creates errors associated with mounting and alignment. In our approach, X-ray imaging was done in one session as follows. Coordinates of each scanning region were preprogrammed and scanning was then performed at each region of the board in order. At the end, the data from each region were stitched together using linear correlation algorithm to match the geometry and form the complete PCB.

First, to ensure enough information is available for alignment, scanning was performed with a 15%–20% overlap between neighboring areas. This portion was then used to align the surfaces together. The alignment process is based on the iterative closest point algorithm [18]. This algorithm operates in the following iterative fashion.

1) Corresponding points in the neighboring scans are associated together based on linear correlation.
2) A transformation (combination of translation and rotation) is estimated to minimize the mean square distance between the reference point cloud and the target one. This transformation function will be iteratively revised to best match the target cloud to the reference.
3) A scaling process is then applied on all the areas by imposing a global minimum and maximum intensity value for the entire data set. These values are obtained by choosing the smallest minimum and the largest maximum value among all the stitched scans.

IV. Image Filtering and Segmentation

Although reconstructed 3-D images contain valuable information, they cannot be used directly for fabrication or elaborate quantified inspection. A series of image processing steps are necessary to transform the *image* to a *computer-aided design (CAD) system* file, which is a prerequisite for fabrication. In particular, to print circuits on the board, Gerber files are generated for each layer, which are 2-D binary CAD files containing geometric information.

The most critical step for the transition from a 3-D X-ray image to a Gerber file is *image segmentation*, that is, assigning material to each pixel (or in the case of 3-D, each voxel) to extract point cloud (x, y, z) information. Efforts have been made in the past to perform image processing on images of PCBs for the purpose of inspection or RE of PCBs [19]–[21]. In [19], defect characterization in PCBs has been achieved using a subtraction and elimination process. The technique is limited to simple defects and physical fixtures are used for alignment purposes. In [20], series of morphological operations, such as erosion and dilation, are utilized for segmentation but lack automation and after the proposed process the images are not converted into CAD files for recreation. Koutsougeras *et al*. [21] applied an automatic

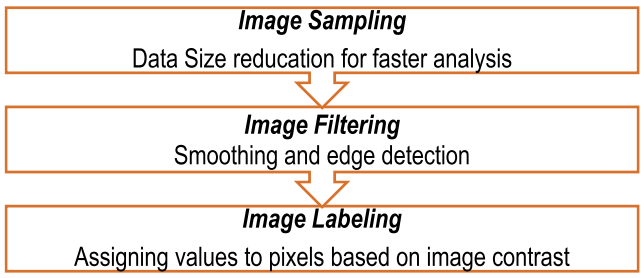
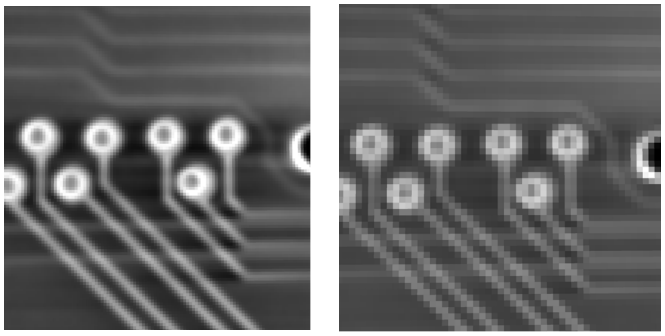


Fig. 6. Image processing algorithm.



(a) (b)

Fig. 7. Image binning (a) 2 and (b) 4.

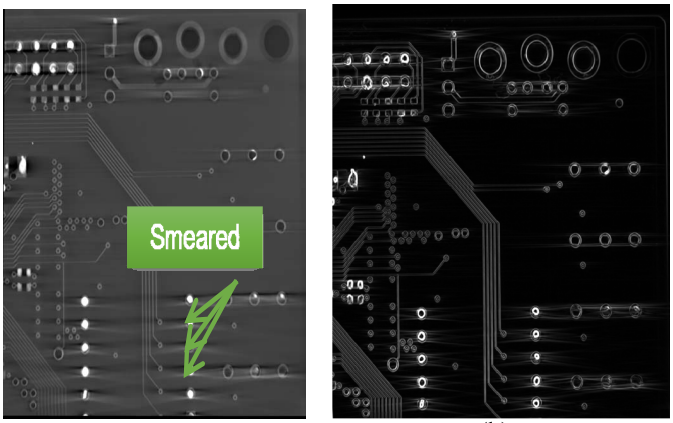
Verilog HDL Model Generator, which includes 2-D image processing technique used to identify the components and their connections at much lower resolution but lacks information about the internal layers.

Here, we propose an automated step-by-step algorithm (shown in Fig. 6) that can be utilized for any 3-D data of the boards regardless of the imaging modality, board feature complexity, and number of layers.

The first step, *image sampling*, is deemed critical when the data size is relatively large as is this case with X-ray tomography data. For instance, the complete data set of the Xilinx board has a file size exceeding 60 GB. Sampling shrinks the dimensions of the original image grid by merging neighboring pixels. Although images may lose sharpness, using a binning of 2 can reduce the file size by a factor $2^3 = 8$, which make the data more manageable for further processing.

Fig. 7 shows the effect of binning on the quality of data for extraction information on vias and traces. Fig. 7(a) is image with binning 2 where traces and vias are still kept at very high quality for feature extraction. On the other binning (1), shown in Fig. 7(b), there is a loss of clear edges and pixilation in the resulting image.

The next step is *filtering the images* to remove different inevitable artifacts in the 3-D data. For example, due to the presence of materials with radically different X-ray absorption coefficients, there are several locations with saturated illumination [as illustrated in Fig. 8(a)]. Also, as the X-ray penetrates through the sample, it loses some of its energy. This phenomenon is known as beam hardening. Beam hardening can cause false image contrast for the same material making the process of labeling difficult. In order to have a clean and accurate CAD file for the imaged PCB traces, there is need



(a) (b)

Fig. 8. X-ray images (a) before and (b) after application of smoothing and 3-D Sobel operator.

to apply different image filtering algorithms and reduce the artifacts so that the image features can be easily extracted. Among all the different type of tools available for feature extraction or feature detection, edge detection is a fundamental and basic set of mathematical methods. The goal of edge detection is identifying regions in a digital image where there is a sharp change of image brightness. It is also a basic step in image processing, image analysis, image pattern recognition, and computer vision techniques. For instance, an ideal edge detector may lead to a set of connected curves that indicates the boundaries of an object. This is a very beneficial tool for the purpose of this paper since detecting the boundaries of PCB traces can hugely help to reconstruct the netlist and reverse engineer the PCB.

There are two main edge type features in the tomographic image: edges resulting from the beam hardening effect, as can be seen in Fig. 8(a), and edges corresponding to PCB traces (which are comparably sharper). Since only the PCB traces are of interest for the RE process, we blur the image before applying the edge detection algorithm. The blurring is performed by convolving the image with a Gaussian filter kernel. The size of the convolution kernel can be selected along each of the three axes. This will increase the smoothness of the image and remove the previously mentioned soft edges (i.e., noise corresponding to beam hardening). Once the image is smoothed, the edge detection filter can be applied to detect only those edges from the PCB traces. There are two major algorithms to detect edges in an image: Laplacian zero-crossing and Sobel algorithm.

The *Laplacian filter* is a rotation invariant edge detection filter. This operator calculates the second spatial derivative of an image. In 1-D, if we take the gradient of a signal with a steep ramp in it, which can be translated as an edge, there will be a large peak centered on the edge. By comparing the peak to a threshold value, one can find the edge, but the thickness of the edge will be directly related to the threshold value. Edges are correlated with peaks in the signal; to overcome this problem, the Laplacian can be computed and the zero crossings in the resulted output will present the edge locations. However, there might be other zeros found in the

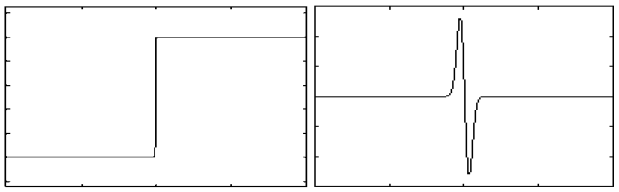


Fig. 9. Response of 1-D Laplacian to step function.

Laplacian due to the texture and noise. These can be removed by comparing the local variance of image intensity. If the value is low then the zero crossing must have been caused by a noise and not a real edge [22]–[24]

$$L(x, y) = \frac{\partial^2 I}{\partial x} + \frac{\partial^2 I}{\partial y} \tag{1}$$

where I represents the image intensity and x, y represent the original coordinates. In order to better demonstrate the concept, a 1-D example is shown in Fig. 9. As mentioned earlier, an edge can be defined as the line where image intensity changes rapidly before and after in one direction. The left image is a step function, which can be assumed as the edge in a 2-D image, and the signal amplitude is similar to the image intensity. The right image shows the result of applying the Laplacian filter on the step function. According to the Laplacian mathematical equation (1), the Laplacian will be zero where the image intensity is constant, positive in the vicinity of the intensity-change on the darker side, negative on the lighter side, and zero at some point in between.

The Sobel algorithm can highlight the edges corresponding to traces and vias while smoothing the rest of the image. The Sobel filter is an edge detection filter that estimates the gradient of an image using central differences. It convolves the image with a $3 \times 3 \times 3$ kernel (2a) and (2b) in all proper directions [15] [25], [26]

$$\underset{X-1}{\begin{bmatrix} -1 & -3 & -1 \\ -3 & -6 & -3 \\ -1 & -3 & -1 \end{bmatrix}}, \quad \underset{X}{\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}}, \quad \underset{X+1}{\begin{bmatrix} 1 & 3 & 1 \\ 3 & 6 & 3 \\ 1 & 3 & 1 \end{bmatrix}} \tag{2a}$$

$$\frac{\partial f}{\partial x} = \frac{f(x+1) - f(x-1)}{2}. \tag{2b}$$

Note that the kernel in the X-direction has been provided above as an example. The Y and Z kernels can be simply obtained by rotating the kernel in the appropriate direction. Although both Laplacian and Sobel filters are good in edge detection, the Laplacian responds only to some of the edges and is very sensitive to noise. Sobel filter is computationally less costly and less sensitive to noise. Therefore, we have used a Sobel filter to detect edges in the image.

Finally, the filtered images are ready to be *labeled*. There are different techniques that can be used to segment/label including Top-hat [27], watershed, thresholding [28], [29], and several others such as binary thresholding [30]. In the following a brief overview of these methods will be discussed.

Top-hat transform is a tool to separate features from each other in an image. It can detect features based on a combination of the image input and its dilation and erosion. This makes the top-hat transform capable of performing different image processing procedures such as feature extraction, background equalization, and image enhancement. Top-hat transform can be configured in two different formats that are called white and black top-hat transforms. The mathematical form of the mentioned filters are presented in (3a) and (3b). If f is a grayscale image and b is a grayscale structuring element then the white and black top-hat transforms are

$$T_w(f) = f - f \circ b \tag{3a}$$

$$T_b(f) = f \bullet b - f \tag{3b}$$

where "$\circ$" denotes opening operation and "$\bullet$" denotes closing operation. The details of these operators are out of the scope of this paper. We refer the interested reader to [31] for more details. It is important to notice the difference between these two forms of top-hat transform. White top-hat detects objects or features in an input image that are smaller than the structuring element are brighter in contrast compared to their neighboring pixels. Dark top-hat returns the smaller but darker objects or features under the same conditions mentioned above. This makes top-hat a good candidate to detect the PCB traces in a fast and accurate manner, but it needs these traces to be the brightest pixel in a region. This is challenging since it is not easy to fully avoid noise from high Z material in the reconstructed images from PCB tomography.

Watershed is another method for image segmentation, which can be classified as a region-based segmentation tool. The basic idea behind this method is from geography, where the watershed is the ridge that divides areas drained by different water flow systems [31]. These areas are called basins and refer to the features or objects in an image. The ridge also refers to the edge of such features. There are different ways to formulate and simulate a watershed transform. However, the main concept behind most of them is to first compute a complete partition of the input image into basins, and then watersheds for the ridges. Although watershed transform can detect the features well, in a noisy image one object will be detected as multiple features and will be labeled with different materials.

Simple *binary thresholding* merely replaces each pixel on an image with a 0 or 1 (black or white) depending on the logical operation on the intensity of the image (i.e., if intensity $(I_{i,j})$ $<$ predefined threshold (T) replaces with 0, else replace with 1) as

$$I_{i,j} = \begin{cases} 1, & \text{for } I_{i,j} > T \\ 0, & \text{for } I_{i,j} < T. \end{cases} \tag{4}$$

However, this simple method cannot be used for the 3-D data of the boards as locations belonging to traces and vias have different image intensities at different locations within the image. This issue is further compounded by stitching, which adds more segments to the image with different intensity values of the same material. Therefore, we have used *localized thresholding* in this paper, where an image is broken into different sections which are not overlapped. In each section, a specific bandwidth of the histogram correlated to the pixel intensity of traces or vias will be segmented. This will select

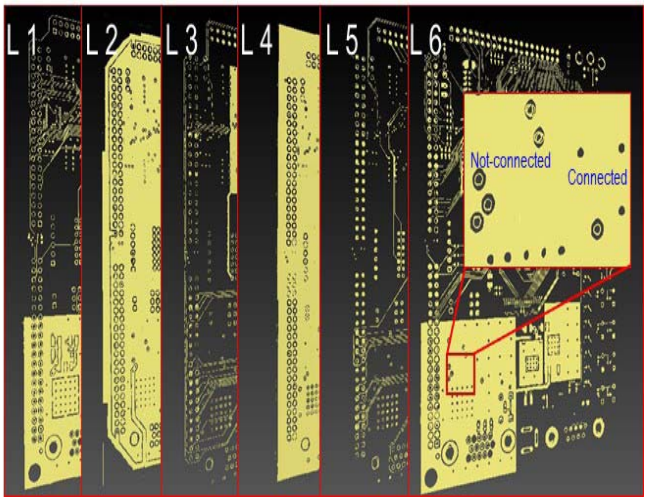


Fig. 10. Segmented layout of PCB layers 1–6, with example of connected and not-connected vias.

the via or traces locally without selecting other features with the same pixel contrast and in another section. Once the bandwidth on the histogram is selected, a brushing tool will be used to only select those trace and via and this process will be repeated all over the image to scan all sections.

Note that we have decided to use a thresholding method in this paper, but any of the three methods introduced in this section can be used for feature extraction. The thresholding method was selected after many rounds of trials among different image segmentation techniques from the literature [32] to find the most suitable algorithms for this purpose since they are based on the image gradient. The final decision on which method to use for segmentation depends mostly on the amount of noise on images; if images have less noise and clear features, watershed or top-hat method can be used, but for images with more noise, thresholding was found to be a more reliable technique.

Fig. 10 shows the outcome of applying localized thresholding method on all layers of the board. Some of the details are not clear in the presented figures, which is due to the image size limitation. The original CAD files indeed present all the details as one zooms in. Fig. 10 also shows a zoomed-in region from layer 1 of this PCB where both connected and not-connected vias are present. As seen in the figure, these connections are accurately segmented in the CAD file.

Performing a layer-by-layer segmentation provides interconnection information between layers. Once it is done for all the PCB layers, the information is then available. In Fig. 11, PCB vias are presented from both the side and top views. In order to reverse engineer this connection one has to know the connectivity conditions of vias to each layer. Each top view segmented layer will provide the information on whether or not a via is connected to any traces in that specific layer. The via itself provides a constant connection between all the layers for our test samples. If a no-connection case is present between via and traces on one layer, that via is not communicating with the layer.

In test samples, all vias were through holes and we had a continuous connection between all the layers. The beauty

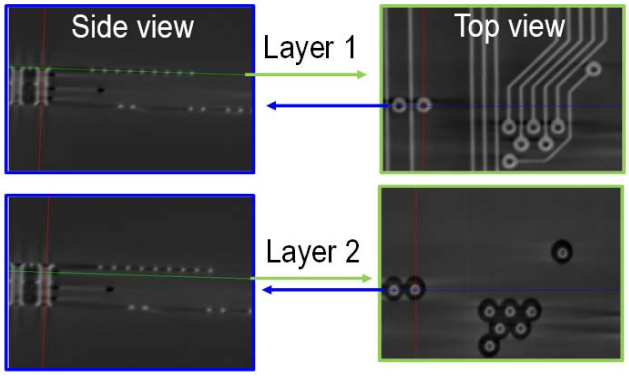


Fig. 11. Side and top views of vias in PCB.

of this method is that for nonthrough hole connections or blind holes, no extra analysis is required. When a PCB has a blind hole, the via information for those layers sharing the via will be extracted as described in this paper. For those layers without that via, the same algorithm is still valid but during segmentation no via is segmented which results in a blind via case. Once all layers' information is presented together it will be clear that the via stops in a certain layer and there is a blind hole.

V. Lessons Learned to Develop Countermeasures

The proposed approach can significantly reduce the time, cost, and manual effort associated with RE. Here are the lessons learned from this research: 1) nondestructive imaging of PCB systems is possible using X-ray tomography; 2) there is always a challenge in feature recognition once a low-density material is located next to high density material; and 3) long X-ray exposure might cause damage or ionization on some of the chips. If the goal is to prevent RE, this can be used as an external source to harvest energy for countermeasures.

We introduce concepts from the last two lessons learned above to prevent RE in critical applications in two ways.

1) *Indirect:* Materials such as zinc sulfide are sensitive to X-ray and emit light upon exposure to X-ray. Using the combination of zinc sulfide and a photodiode, one can implement an X-ray sensor in the system to store the history of the devices exposure to high energy X-ray photons and/or react destructively when the exposure exceeds a certain limit.
2) *Direct:* X-ray photons are directly converted into electrical charge, which can be used to alter information in the device. These types of sensors are fabricated from solid-state material such as silicon [22]. The amount of exposure and the X-ray power defines the output of the sensor. Depending on the amount of energy harvested from the sensor, one can use it to store exposure information in the device or use it as an anti-RE sensor as stated above.

VI. Conclusion and Future Work

In this study, we have presented a nondestructive RE method using X-ray tomography on a custom PCB and another, more complex commercial Xilinx Spartan-6 starter board. The netlist of components and connections were extracted as a

CAD file from the images using advanced image processing techniques. These types of files can be directly converted into DXF or GERBER files that are compatible with circuit printing machines. We will continue the study to develop a software where the X-ray images are imported and the final netlist is generated as output in a completely automated fashion. Image noise is the main challenge in automating the process. Image artifacts and noises are unpredictable to some extent and can be compensated either by removing the noise source before imaging or using other postprocessing techniques to solve it. This will be further investigated and addressed in the future work by the authors.

Since RE could lead to IP theft, piracy, cloning, and so on of PCB products, we will be developing countermeasures for both destructive and nondestructive methods using either high density material or advanced packages that detect an attack and destroy the proprietary information before it can be captured by the adversary [33]. We hope that this paper raises awareness of the current-state-of-the-art techniques and provides motivation for the development of additional low-cost and robust anti-RE techniques.

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