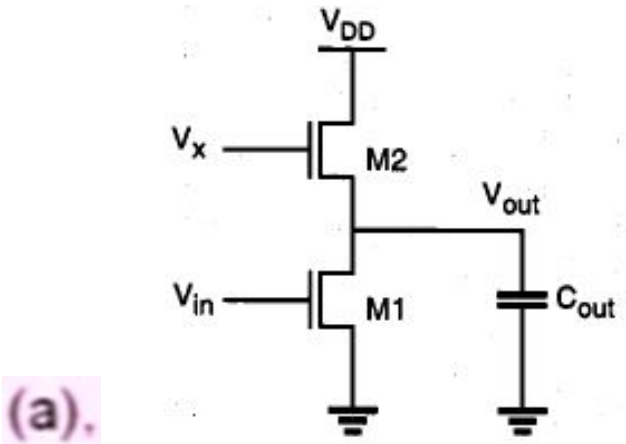
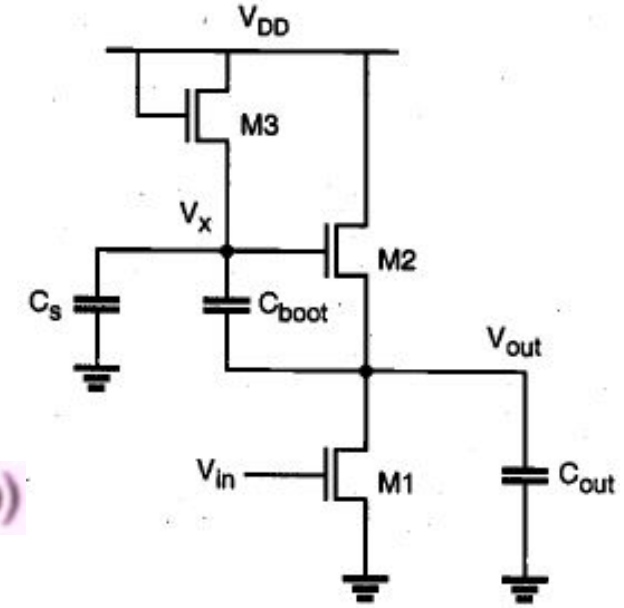
Unit 5: Dynamic Logic Circuits

Voltage Bootstrapping

- Voltage bootstrapping is a technique used for overcoming threshold voltage drops in digital circuits.
- Consider the circuit shown in (a), where voltage $V_x \leq V_{DD}$. M2 will operate in saturation.
- When $V_{in} = 0$, then $V_{out}(max) = V_x - V_{T2}(V_{out})$
- To overcome threshold voltage drop and to obtain V_{DD} at output node, V_x must be increased.
- In (b) third transistor M3 is added.



(a).



(b)

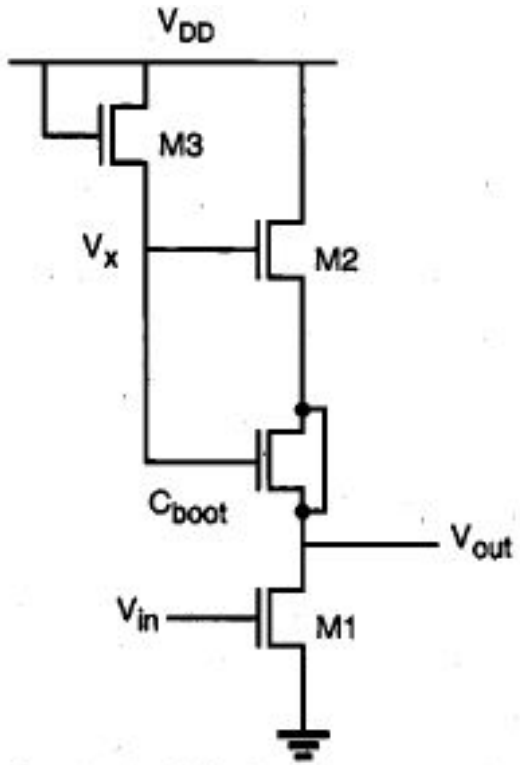
Cont…

- The two capacitor C_s and C_{boot} represent capacitances which dynamically couple the voltage V_x to the ground and to the output.
- The circuit will produce a high V_x during switching, so threshold voltage can be overcome at the output node. $V_x \geq V_{DD} + V_{T2}(V_{out})$
- Initially Vin = 1, M1 is in linear region & M2 in saturation and output voltage is low.
- Since ID3 = 0, $V_x = V_{DD} - V_{T3}(V_x)$
- If input switches from 1 to 0 at t = 0, M1 turns off and V_{out} will start to rise.
- The change in output voltage level will now be coupled to V_x through bootstrap capacitor C_{boot}.
- The transient current flowing through C_s and C_{boot} is

$$i_{Cs} \approx i_{Cboot} \Leftrightarrow C_S \frac{dV_x}{dt} \approx C_{boot} \frac{d(V_{out} - V_x)}{dt}$$

Cont…

- C_s is the sum of parasitic source-to-substrate capacitance of M3 and gate-to-substrate capacitance of M2.
- To obtain large C_{boot} in comparison to C_s, an extra dummy transistor is added to the circuit as shown.
- The dummy transistors drain and source terminals are connected together, it acts as an MOS capacitor between V_x and V_{out}.

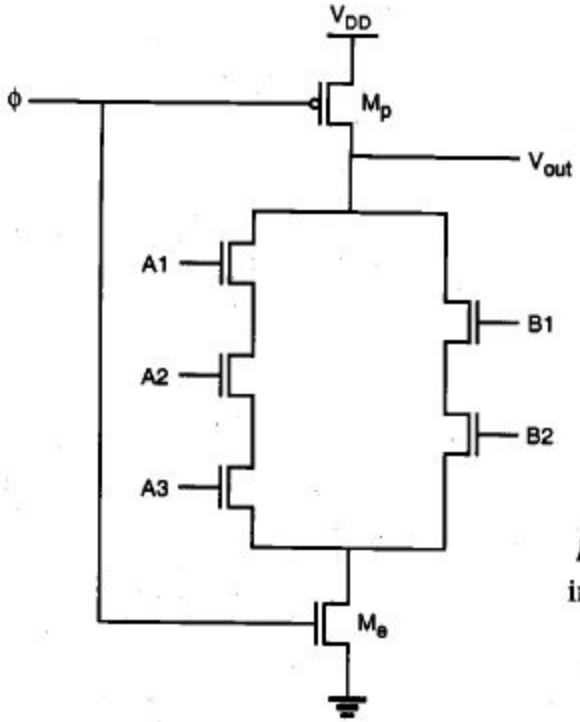


Realization of the bootstrapping capacitor with a dummy MOS device.

Dynamic CMOS Logic (Precharge-Evaluate Logic)

In the following, we will introduce a dynamic CMOS circuit technique which allows us to significantly reduce the number of transistors used to implement any logic function.

The circuit operation is based on first *precharging* the output node capacitance and subsequently, *evaluating* the output level according to the applied inputs.



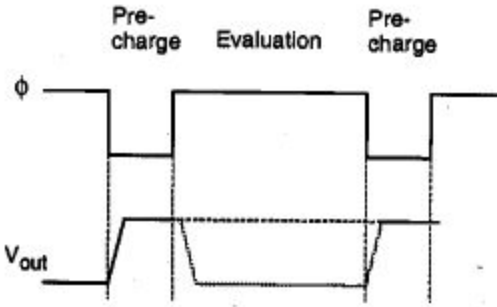


Figure 9.26. Dynamic CMOS logic gate implementing a complex Boolean function.

Both of these operations are scheduled by a single clock signal, which drives one nMOS and one pMOS transistor in each dynamic stage. A dynamic CMOS logic gate which implements the function $F = \overline{(A_1A_2A_3 + B_1B_2)}$ is shown in Fig. 9.26.

Cont…

When the clock signal is low (precharge phase), the pMOS precharge transistor M_p is conducting, while the complementary nMOS transistor M_e is off. The parasitic output capacitance of the circuit is charged up through the conducting pMOS transistor to a logic-high level of $V_{out} = V_{DD}$. The input voltages are also applied during this phase, but they have no influence yet upon the output level since M_e is turned off.

When the clock signal becomes high (evaluate phase), the precharge transistor M_p turns off and M_e turns on. The output node voltage may now remain at the logic- high level or drop to a logic low, depending on the input voltage levels. If the input signals create a conducting path between the output node and the ground, the output capacitance will discharge toward $V_{OL} = 0$ V. The final discharged output level depends on the time span of the evaluation phase. Otherwise, V_{out} remains at V_{DD}.

The operation of the single-stage dynamic CMOS logic gate is quite straightforward. For practical multi-stage applications, however, the dynamic CMOS gate presents a significant problem. To examine this fundamental limitation, consider the two-stage cascaded structure shown in Fig. 9.27. Here, the output of the first dynamic CMOS stage drives one of the inputs of the second dynamic CMOS stage, which is assumed to be a two-input NAND gate for simplicity.

Cont…

During the precharge phase, both output voltages Vout1, and *Vout2* are pulled up by the respective pMOS precharge devices. Also, the external inputs are applied during this phase. The input variables of the first stage are assumed to be such that the output Vout1 will drop to logic "0" during the evaluation phase. On the other hand, the external input of the second-stage NAND2 gate is assumed to be a logic " 1," as shown in Fig. 9.27.

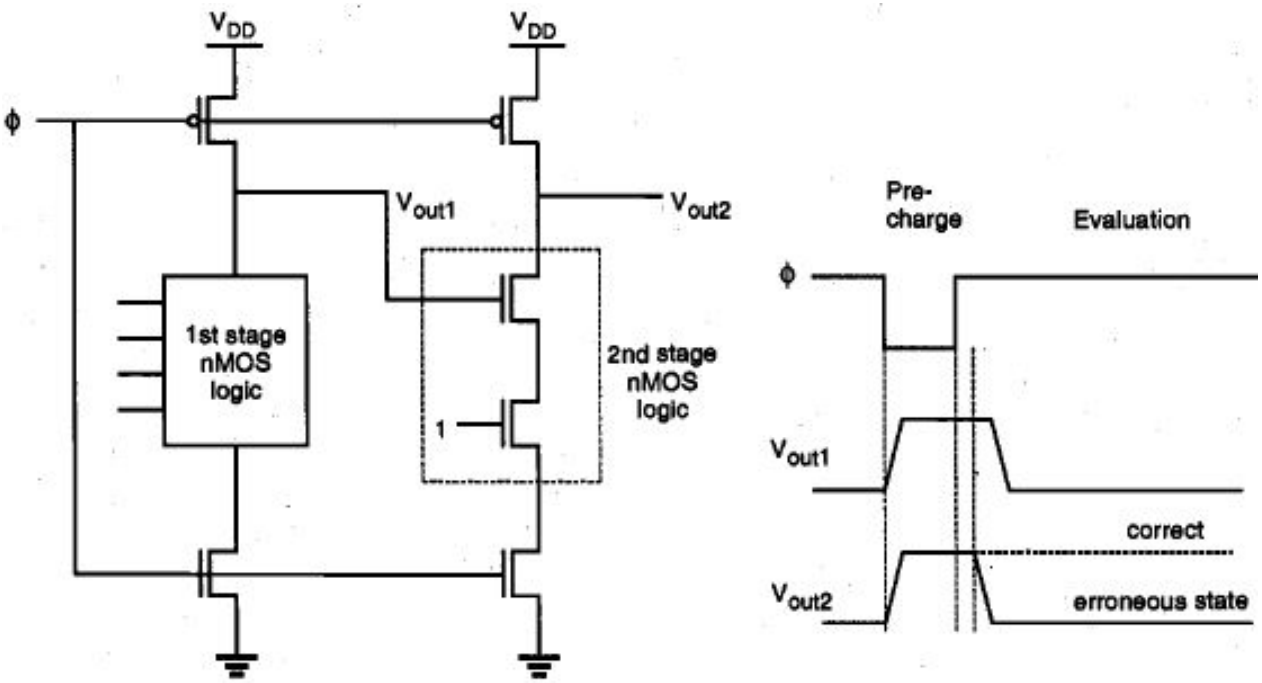


Figure 9.27. Illustration of the cascading problem in dynamic CMOS logic.

Cont…

When the evaluation phase begins, both output voltages Voutl and *Vout2* are logic-high. The output of the first stage (Vout1) eventually drops to its correct logic level after a certain time delay.
However, since the evaluation in the second stage is done concurrently, starting with the high value of Voutl at the beginning of the evaluation phase, the output voltage *Vout2* at the end of the evaluation phase will be *erroneously* low. Although the first stage output subsequently assumes its correct output value once the stored charge is drained, the correction of the second-stage output is not possible.

This example illustrates that dynamic CMOS logic stages driven by the same clock signal cannot be cascaded directly. This severe limitation seems to undermine all the other advantages of dynamic CMOS logic, such as low power dissipation, large noise margins, and low transistor count. Alternative clocking schemes and circuit structures must be developed to overcome this problem.

Domino CMOS Logic

Remember that the problem in cascading conventional dynamic CMOS stages occurs when one or more inputs of a stage make a 1 to 0 transition *during* the evaluation phase, as illustrated in Fig. 9.27.

On the other hand, if we build a system by cascading domino CMOS logic gates as shown in Fig. 9.29, all input transistors in subsequent logic blocks will be turned off during the precharge phase, since all buffer outputs are equal to 0. During the evaluation phase, each buffer output can make at most one transition (from 0 to 1),

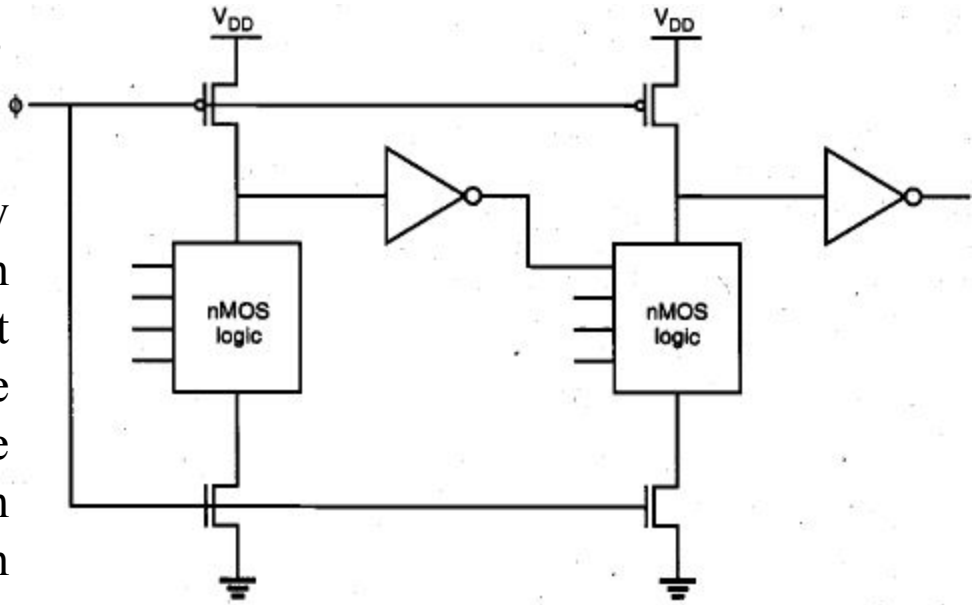
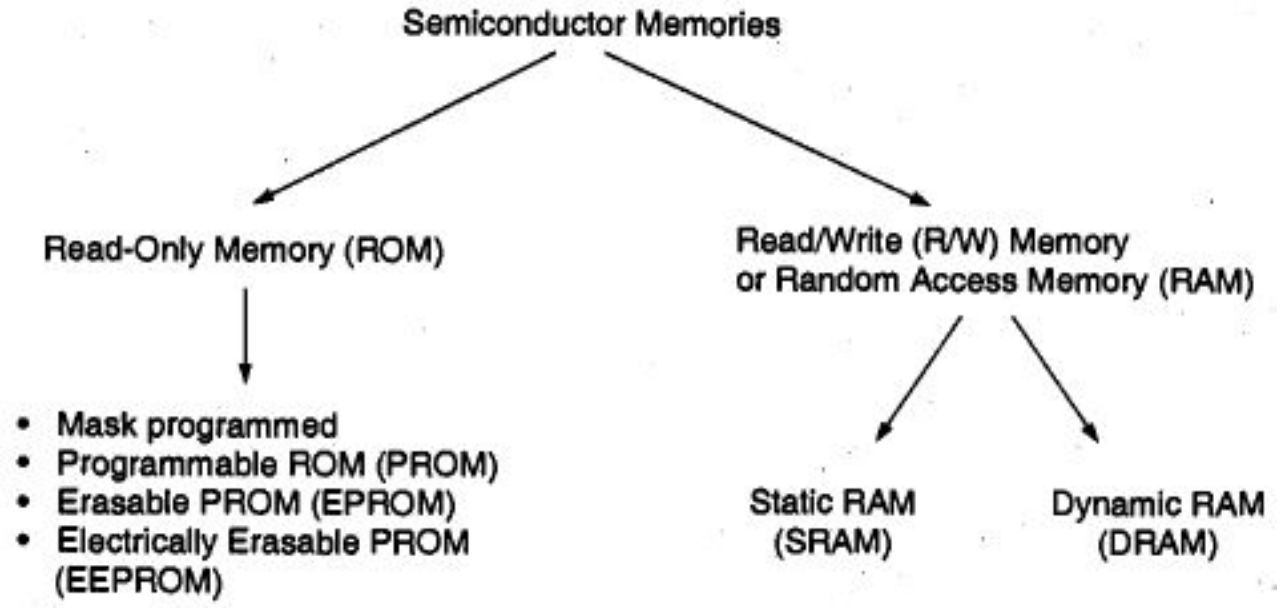


Figure 9.29. Cascaded domino CMOS logic gates.

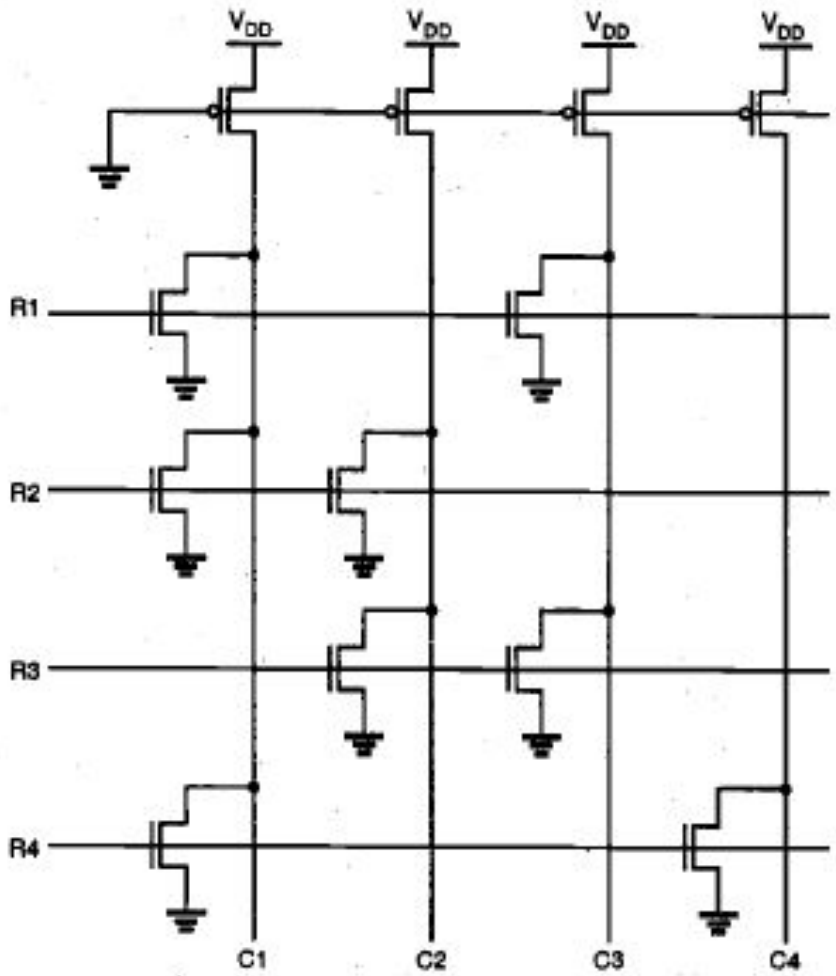
and thus each input of all subsequent logic stages can also make at most one (0 to 1) transition. In a cascade structure consisting of several such stages, the evaluation of each stage ripples the next stage evaluation, similar to a chain of dominos falling one after the other. The structure is hence called *domino CMOS logic.*

Semiconductor **Memories**



Overview of semiconductor memory types.

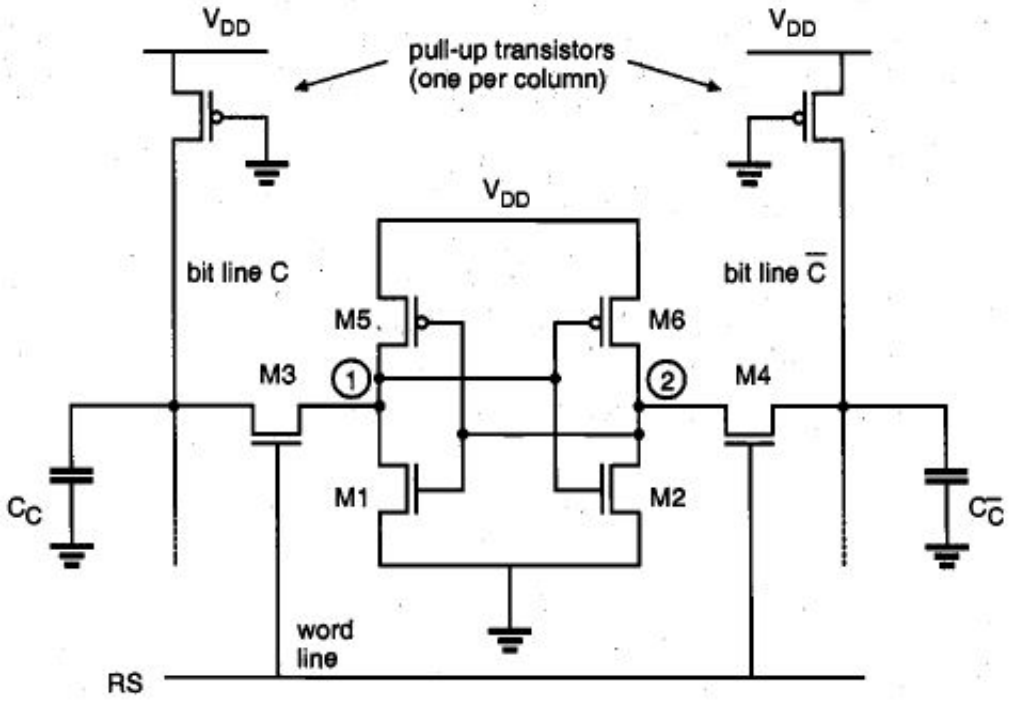
Read-Only Memory (ROM) Circuits



R1	R2	R3	R4	C1	C2	C3	C4
1	0	0	0	0	1	0	1
0	1	0	0	0	0	1	1
0	0	1	0	1	0	0	1
0	0	0	1	0	1	1	0

Example of a 4-bit x 4-bit NOR-based ROM array .

6T – *CMOS SRAM Cell Design Strategy*



Circuit topology of the CMOS SRAM cell.

To determine the (W/L) ratios of the transistors in a typical CMOS SRAM cell as shown in Fig. a number of design criteria must be taken into consideration. The two basic requirements which dictate the (W/L) ratios are:

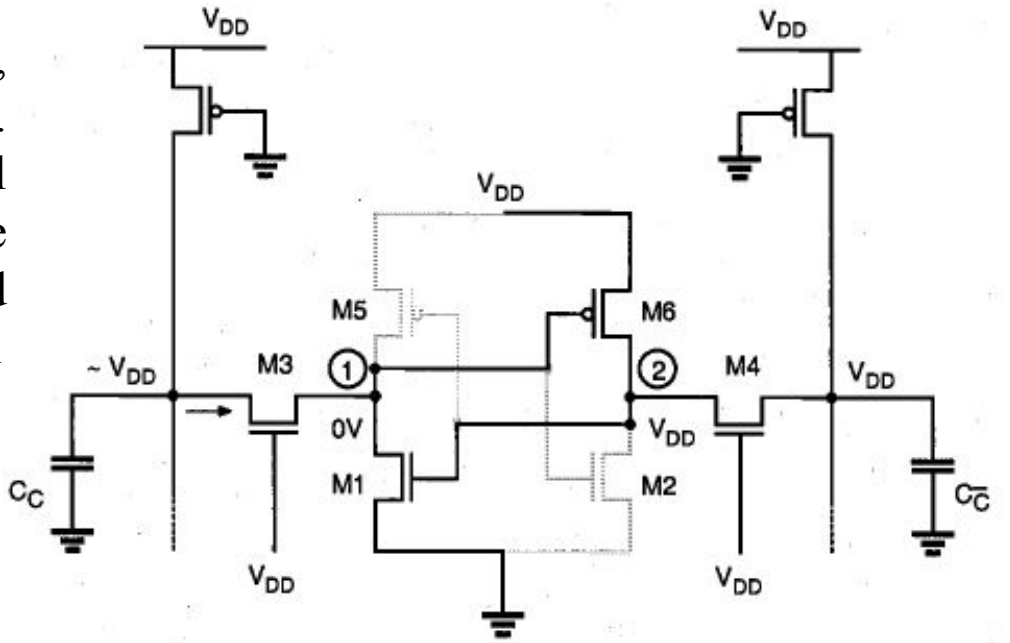
(a) the data-read operation should not destroy the stored information in the SRAM cell, and

(b) the cell should allow modification of the stored information during the data-write phase.

Voltage levels in the SRAM cell at the beginning of the "read" operation

Consider the data read operation first, assuming that a logic "0" is stored in the cell. The voltage levels in the CMOS SRAM cell at the beginning of the "read" operation are depicted in Fig. Here, the transistors M2 and M5 are turned off, while the transistors M1 and M6 operate in the linear mode.

Thus, the internal node voltages are V1 = 0 and V2 = *VDD before* the cell access (or pass) transistors M3 and M4 are turned on. The active transistors at the beginning of the data-read operation are highlighted in Fig.



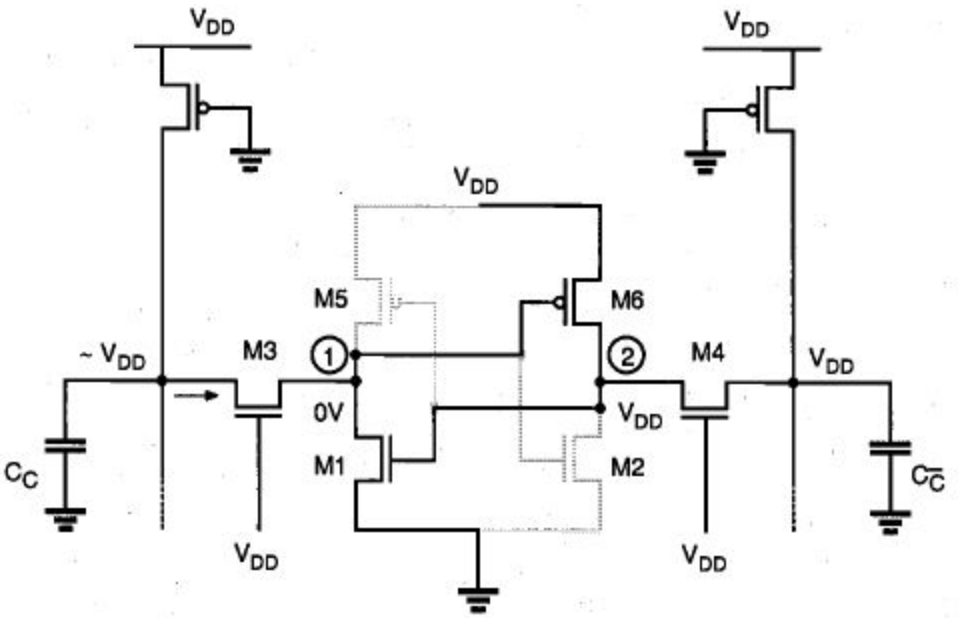
Voltage levels in the SRAM cell at the beginning of the "read" operation.

After the pass transistors M3 and M4 are turned on by the row selection circuitry, the voltage level of column $\overline{C}$ will not show any significant variation since no current will flow through M4. On the other half of the cell, however, M3 and M1 will conduct a nonzero current and the voltage level of column C will begin to drop slightly. Note that the column capacitance C_C is typically very large; therefore, the amount of decrease in the column voltage is limited to a few hundred millivolts during the read phase.

Cont…

The key design issue for the data-read operation is then to guarantee that the voltage V1, does not exceed the threshold voltage of M2, so that the transistor M2 remains turned off during the read phase, i.e.,

$$V_{1,max} \leq V_{T,2}$$



Voltage levels in the SRAM cell at the beginning of the "read" operation.

We can assume that after the access transistors are turned on, the column voltage Vc remains approximately equal to *VDD*. Hence, M3 operates in saturation while M1 operates in the linear region.

$$\frac{k_{n,3}}{2}\left(V_{DD}-V_1-V_{T,n}\right)^2 = \frac{k_{n,1}}{2}\left(2\left(V_{DD}-V_{T,n}\right)V_1-V_1^2\right)$$

Combining this equation with the above equation results in:

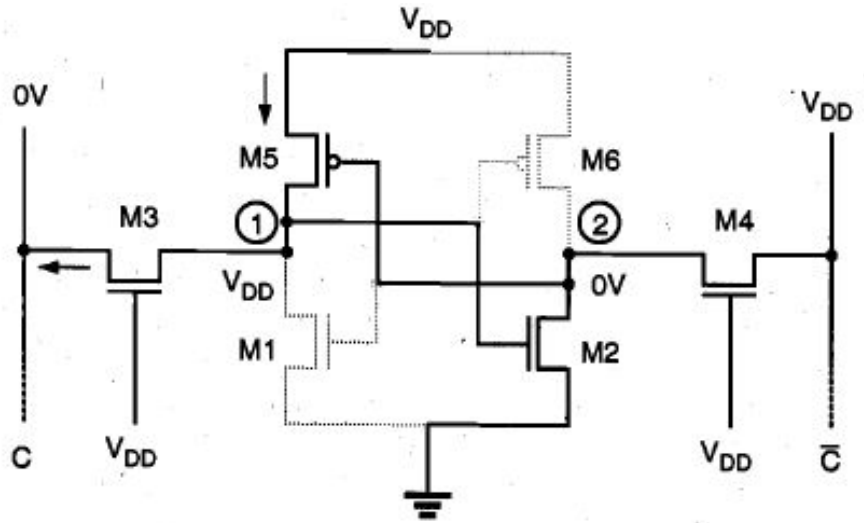
$$\frac{k_{n,3}}{k_{n,1}} = \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1} < \frac{2\left(V_{DD}-1.5V_{T,n}\right)V_{T,n}}{\left(V_{DD}-2V_{T,n}\right)^2}$$

The upper limit of the aspect ratio found above is actually more conservative, since a portion of the drain current of M3 will also be used to charge-up the parasitic node capacitance of node (1).

To summarize, the transistor M2 will remain in cut-off during the read "0" operation if above condition is satisfied.
A symmetrical condition also dictates the aspect ratios of M2 and M4.

Voltage levels in the SRAM cell at the beginning of the "write" operation

Now consider the write "0" operation, assuming that a logic "1" is stored in the SRAM cell initially. Figure shows the voltage levels in the CMOS SRAM cell at the beginning of the data-write operation. The transistors M1 and M6 are turned off, while the transistors M2 and M5 operate in the linear mode. Thus, the internal node voltages are V1 = *VDD* and *V2*= 0 *V before* the cell access (or pass) transistors M3 and M4 are turned on.



Voltage levels in the SRAM cell at the beginning of the "write" operation.

The column voltage V_C is forced to logic "0" level by the data-write circuitry; thus, we may assume that V_C is approximately equal to 0 V. Once the pass transistors M3 and M4 are turned on by the row selection circuitry, we expect that the node voltage V_2 remains *below* the threshold voltage of M1, since M2 and M4 are designed according to condition (10.5). Consequently, the voltage level at node (2) would not be sufficient to turn on M1. To change the stored information, i.e., to force V_1 to 0 V and V_2 to V_{DD}, the node voltage V_1 *must be reduced below* the threshold voltage of M2, so that M2 turns off first. When $V_1 = V_{T,n}$, the transistor M3 operates in the linear region while M5 operates in saturation.

Cont…

$$\frac{k_{p,5}}{2}\left(0 - V_{DD} - V_{T,p}\right)^2 = \frac{k_{n,3}}{2}\left(2\left(V_{DD} - V_{T,n}\right)V_{T,n} - {V_{T,n}}^2\right) \qquad (10.6)$$

Rearranging this condition results in:

$$\frac{k_{p,5}}{k_{n,3}} < \frac{2\left(V_{DD} - 1.5\,V_{T,n}\right)V_{T,n}}{\left(V_{DD} + V_{T,p}\right)^2}$$

$$\frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_3} < \frac{\mu_n}{\mu_p} \cdot \frac{2\left(V_{DD} - 1.5\,V_{T,n}\right)V_{T,n}}{\left(V_{DD} + V_{T,p}\right)^2} \qquad (10.7)$$

To summarize, the transistor M2 will be *forced* into cut-off mode during the write "0" operation if condition (10.7) is satisfied. This will guarantee that M1 subsequently turns on, changing the stored information. Note that a symmetrical condition also dictates the aspect ratios of M6 and M4.

SRAM Data '1' Read operation

1) let $Q = 1$ & $\overline{Q} = 0$

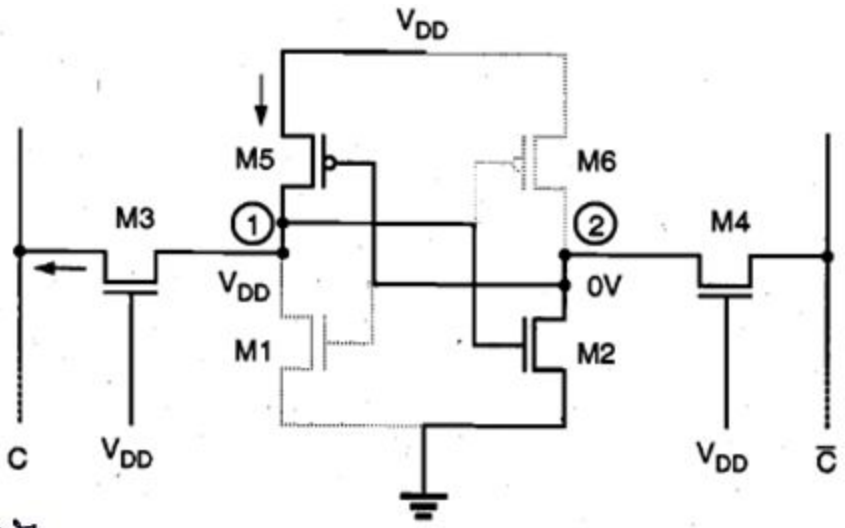
2) WL = 1

3) Bit & $\overline{Bit}$ ⇒ o/p lines

4) Precharge cap to V_{DD}

→ 5) $\overline{Bit}$ = Volt ↓

6) Bit & $\overline{Bit}$ → to sense amplifier.
& if $\overline{Bit}$ Value. ↓ then o/p = 1



SRAM Data '0' Read operation

1) let $Q = 0$ & $\overline{Q} = 1$

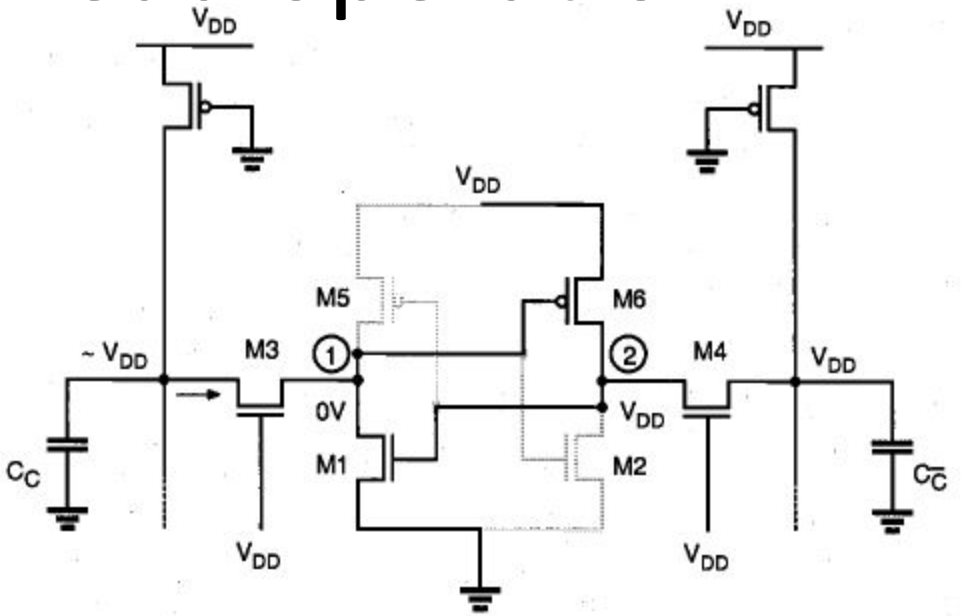
2) $WL = 1$

3) Bit & $\overline{Bit}$ $\Rightarrow$ o/p lines

4) Precharge cap to V_{DD}

→ 5) Bit = Volt ↓.

If Bit value ↓ then o/p = 0



Voltage levels in the SRAM cell at the beginning of the "read" operation.

SRAM Data '1' write operation

1) let $Q = 0$ & $\overline{Q} = 1$

2) $WL = 1$

3) Bit & $\overline{Bit}$ ⇒ i/p.

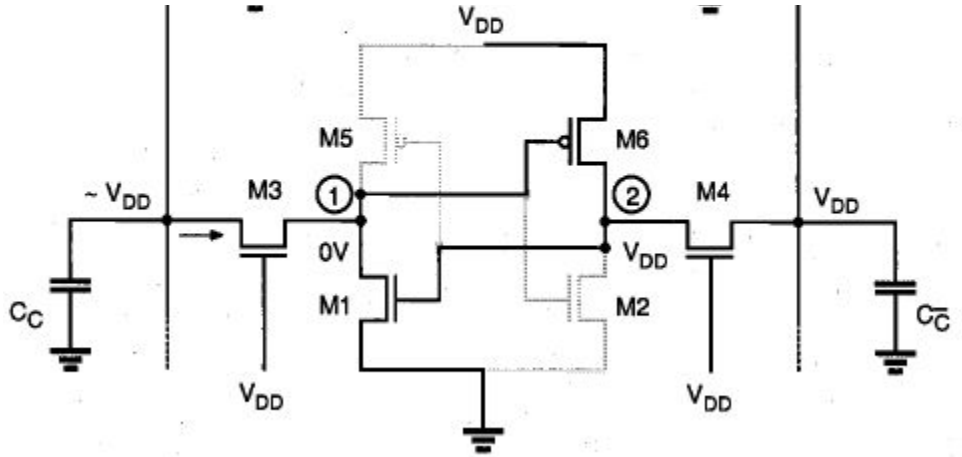
⇒ 4) $\overline{Bit}$ = Gnd

5) V_2 → decreases

now $V_2 < V_T$ of M_1

then M_1 = off

then M_5 = on



If M_5 = on then V_1 = high

$Q = 1$

Three-Transistor DRAM Cell

The operation of the three-transistor DRAM cell and its peripheral circuitry is based on a two-phase non-overlapping clock scheme. The precharge events are driven by φ1, whereas the "read" and "write" events are driven by φ2.

Every "data read" and "data write“ operation is preceded by a precharge cycle, which is initiated with the precharge signal PC going high. During the precharge cycle, the column pull-up transistors are activated, and the corresponding column capacitances C2 and *C3* are charged up to logic-high level.

With typical enhancement type nMOS pull-up transistors ($V_{TO} \approx 1.0$ V) and a power supply voltage of 5 V, the voltage level of both columns after the precharge is approximately equal to 3.5 V.

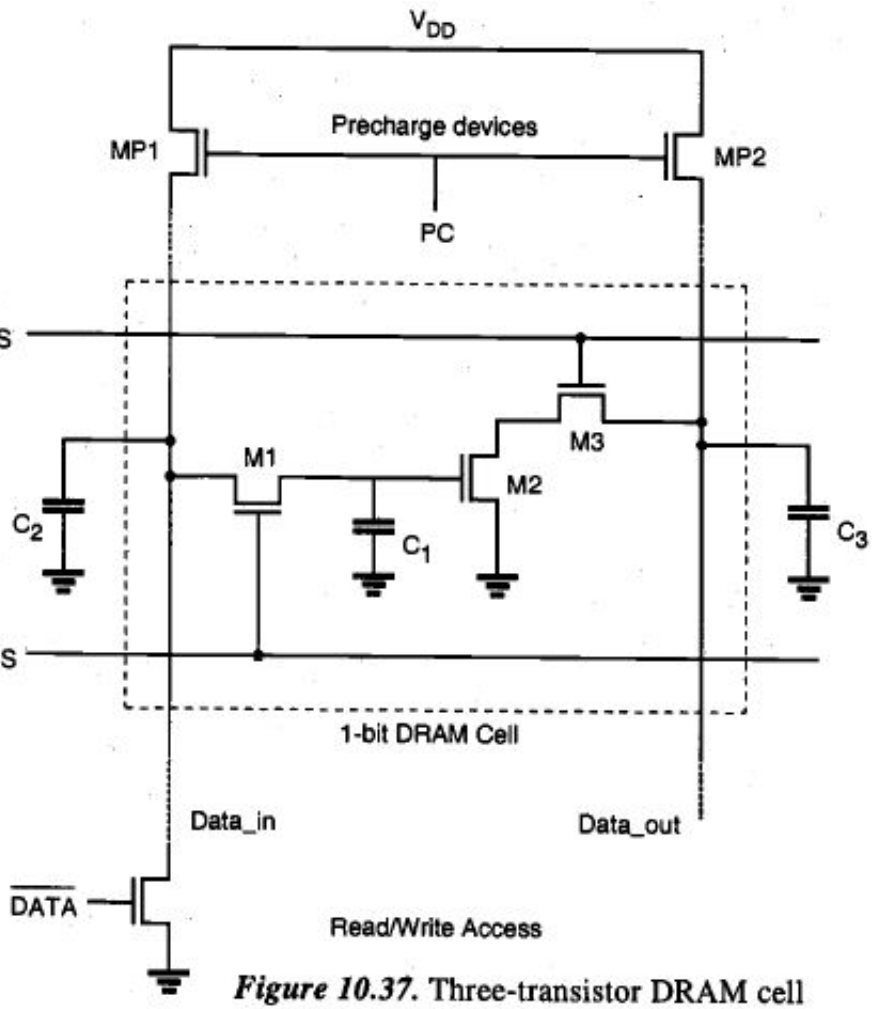
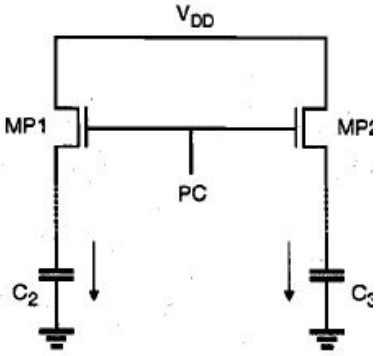


Figure 10.37. Three-transistor DRAM cell with the pull-up and read/write circuitry.

All "data read" and "data write" operations are performed during the active ϕ_2 phase, i.e., when PC is low. Figure 10.38 depicts the typical voltage waveforms associated with the 3-T DRAM cell during a sequence of four consecutive operations: write "1," read "1," write "0," and read "0." The four precharge cycles shown in Fig. 10.38 are numbered 1, 3, 5, and 7, respectively. Figure 10.39 illustrates the transient currents charging up the two columns (D_{in} and D_{out}) during a precharge cycle. The precharge cycle is effectively completed when both capacitance voltages reach their steady-state values. Note here that the two column capacitances C_2 and C_3 are at least one order of magnitude larger than the internal storage capacitance C_1.



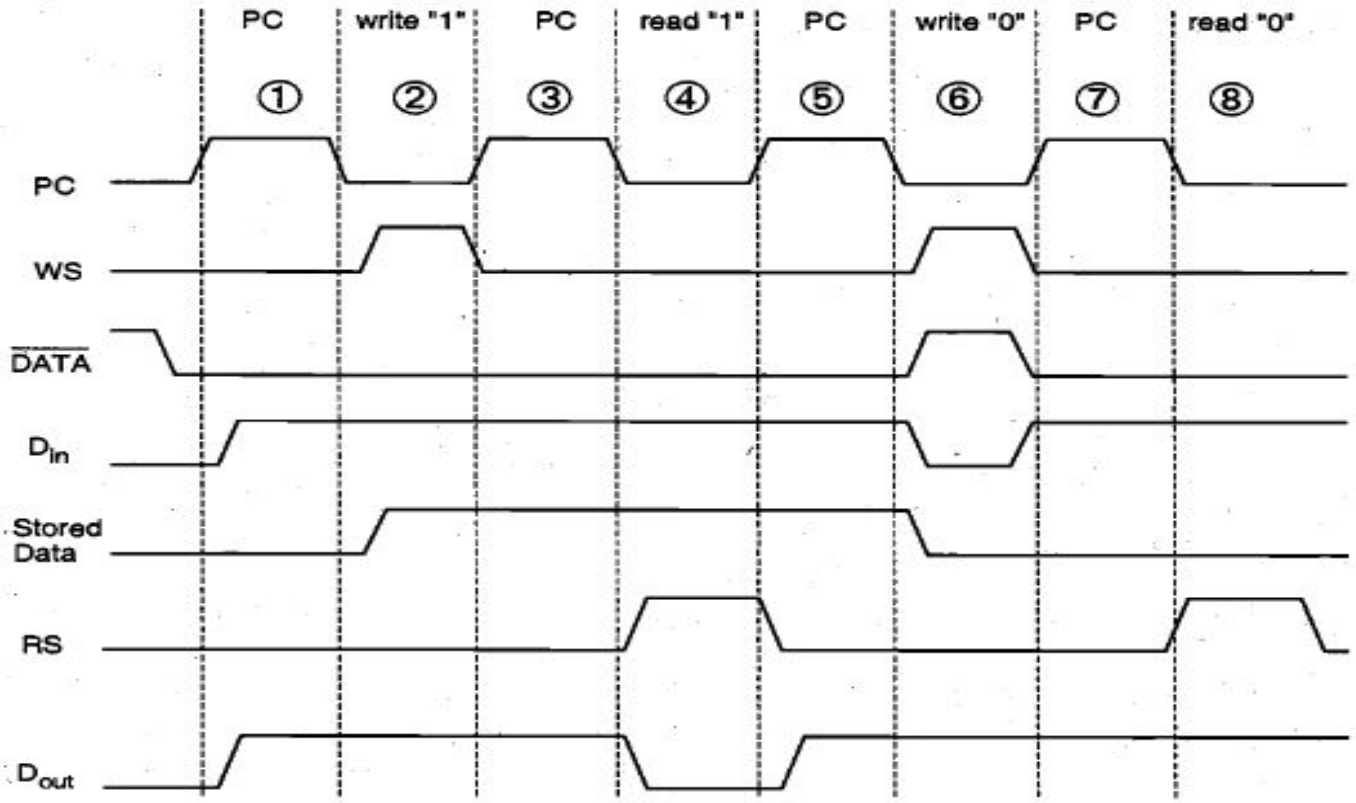


Figure 10.38. Typical voltage waveforms associated with the 3-T DRAM cell during four consecutive operations: write "1," read "1," write "0," and read "0."

3T DRAM Data Write operation

i) $W = 1$, $R = 0$

ii) $M_1 = ON$

$M_2 = M_3 = OFF$

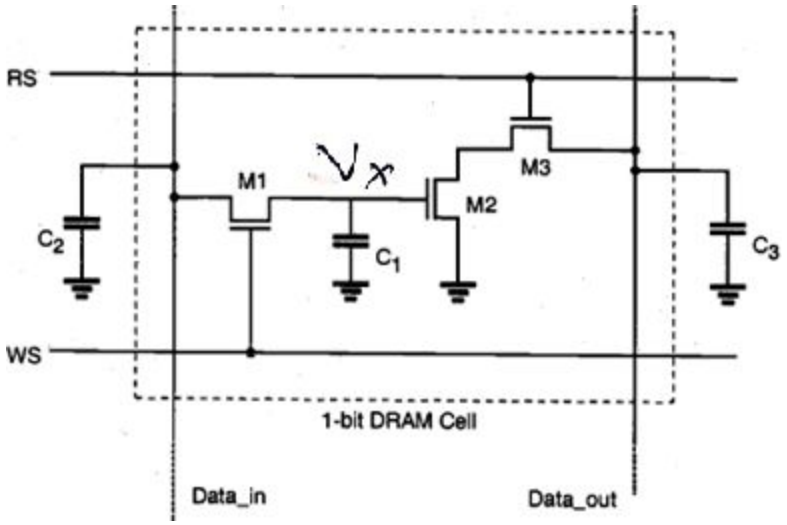
iii) Bit = I/p line for write

iv) $V_X = V_{DD} - V_T$ → when Bit = 1

v) $V_X = 0$ → when Bit = 0

vi) $\overline{Bit}$ → opposite of Bit

vii) $W = 0$



3T DRAM Data Read operation

1) $R = 1$, $W = 0$

2) $M_3 = ON$, $M_1 = Off$

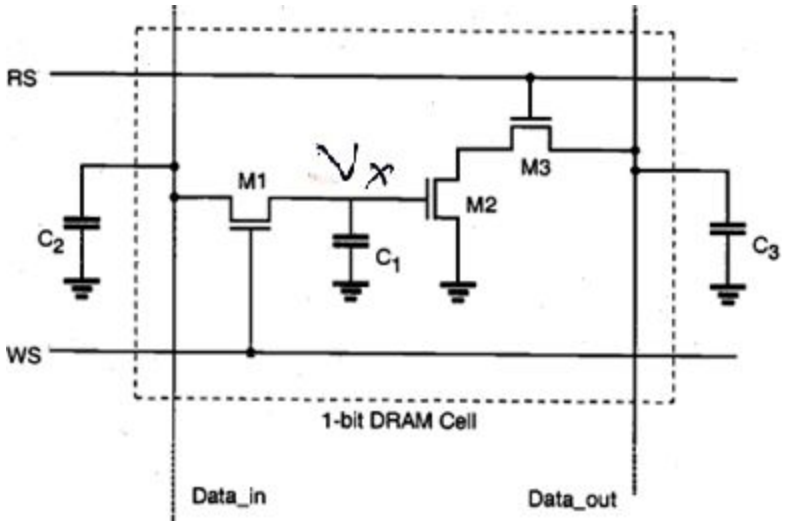
3) C_3 is precharged to Vdd for read

4) If $V_x = V_{DD} - V_{tn}$

$M_2 = ON$ then $M_3 = ON$

i.e., $\overline{Bit} = 0$ → sent to sense amplifier

Hence O/p = 1.

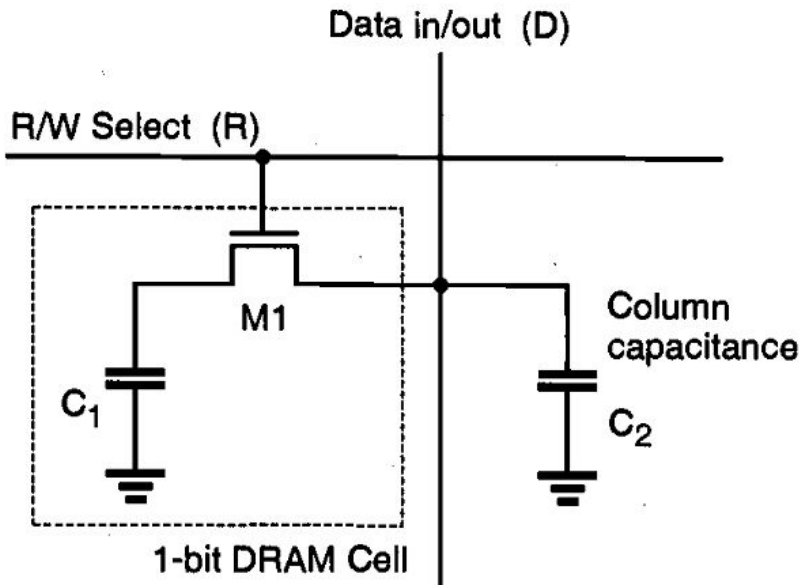


5) If $V_x = 0$

$M_2 = Off$

$\overline{Bit} = V_{DD}$ Precharged will remain as it is so O/p = 0

1T DRAM Cell



Read operation

1) $C_2 = \frac{V_{dd}}{2}$ (precharge)

2) WL = 1

M_1 = ON

node volt is $\frac{V_{dd}}{2}$

If C_1 has 0 V

node volt becomes '0'

or node volt $< \frac{V_{dd}}{2}$

Sense Amplifr senses

O/p to be '0'

If C_1 has 1 V

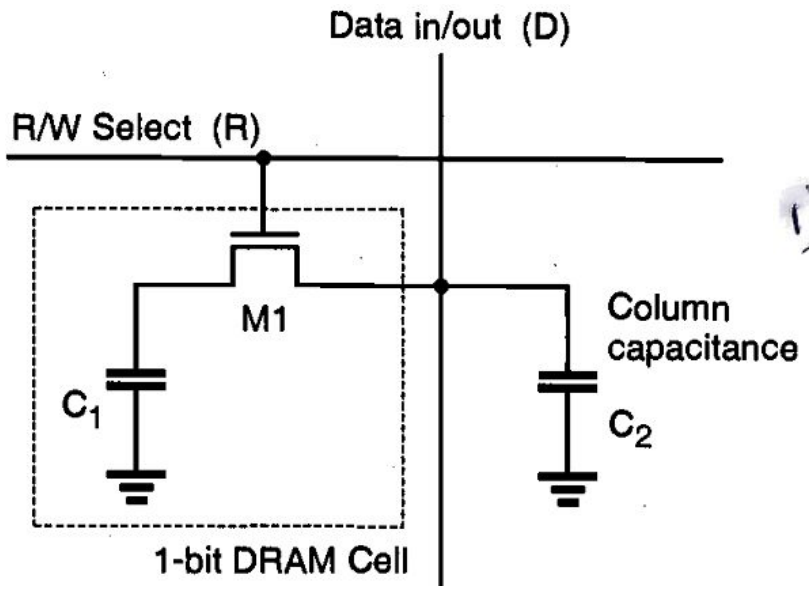
then node volt becomes $> \frac{V_{dd}}{2}$

If it is sent to sense amplifier

then O/p is read as 1

It will refresh the cell.

1T DRAM Cell



Write operation

1) Data line act as I/P we can place I/O to I/P line

2) WL = 1

3) If DL = 1 $C_1 \Rightarrow$ Vdd (charging)

3) If DL = 0 $C_1 \Rightarrow 0$ (discharging)

Reference

- **Sung-Mo Kang, Yusuf Leblebici:** "*CMOS DIGITAL INTEGRATED CIRCUITS Analysis and Design,"* 3rd Edition, McGraw Hill, 2003.
  - For Unit 4 – refer chapter 7 and 8
  - For Unit 5 – refer chapter 9 and 10