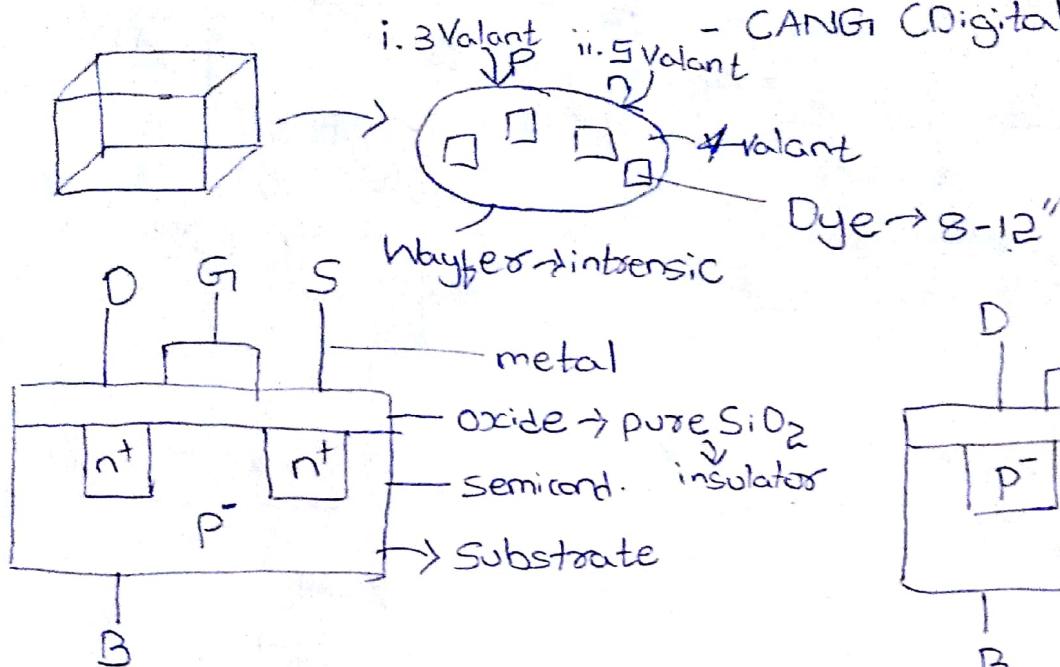


09/03/2021

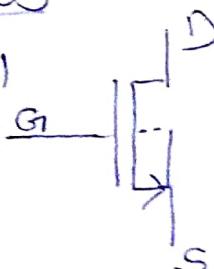
CMOS VLSI

- Harris & Banerji
- Dukonal
- CANGI (Digital IC)



npn - nMOS

- D ↑ potential
- S ↓ pot.
- B ↓↓ pot.



- G₁ = 0 ⇒ open switch

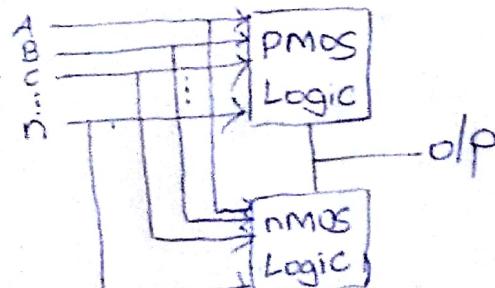
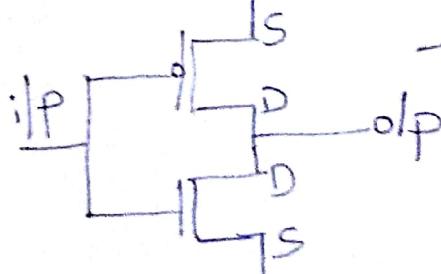
- G₁ = 0 ⇒ closed switch

- G₁ → +ve ⇒ D & S fb ⇒ e⁻ accumulate towards G₁ from P₁; V_D > V_G
- D +ve & G₁ +ve ⇒ D-fb & S-fb ⇒ e⁻ flow from S to D.
→ I flow from D to S.

i.e. Flow of I ∝ V_G.

V_D

→ Inverter



V_D

I/P

PMOS

nMOS

O/P

O/P

I/P

O/S

CS

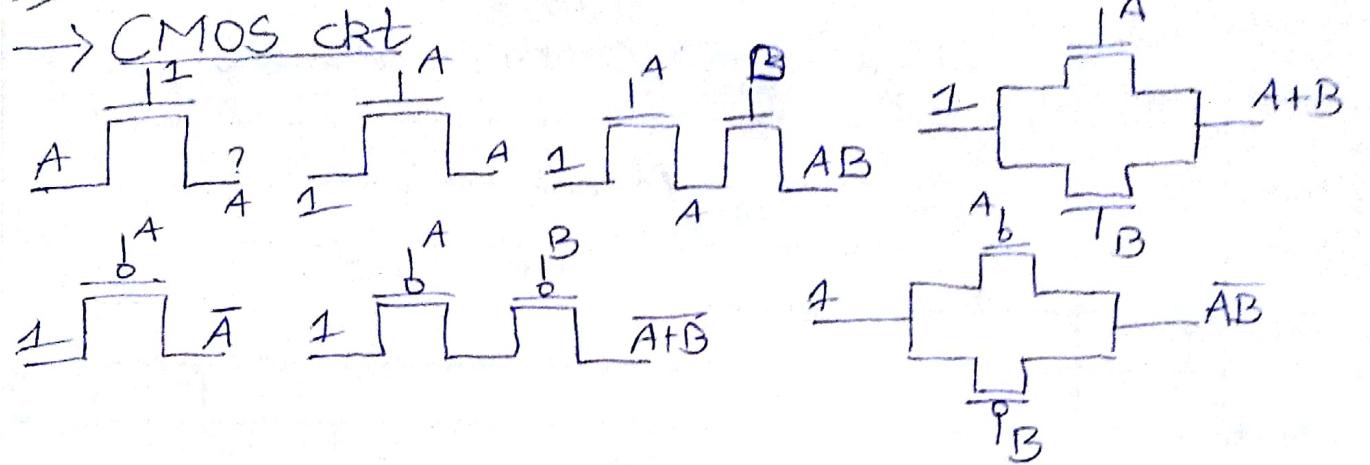
C/S

O/S

O

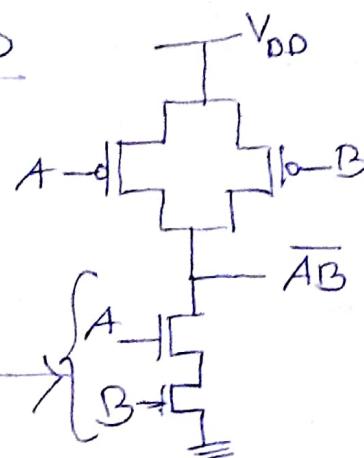
1

13/03/2021

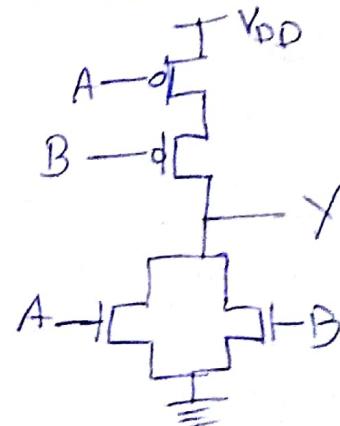


1. 2 ilp NAND

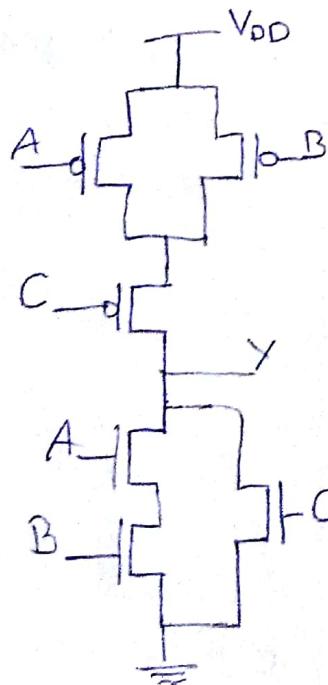
A	B	$Y = \overline{AB}$
0	0	1
0	1	0
1	0	0
1	1	0



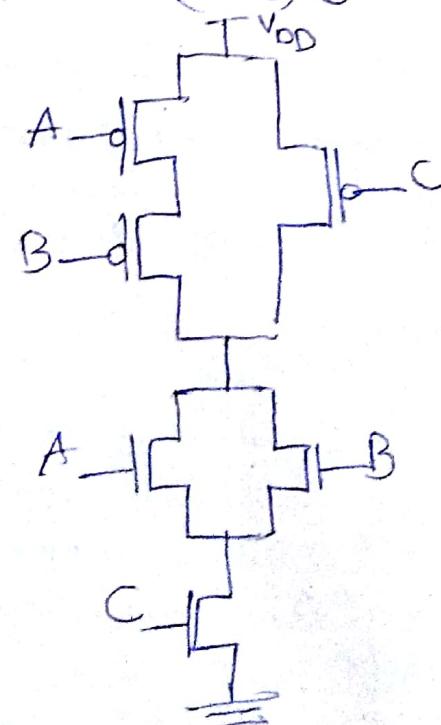
2. 2 ilp NOR $A+B$

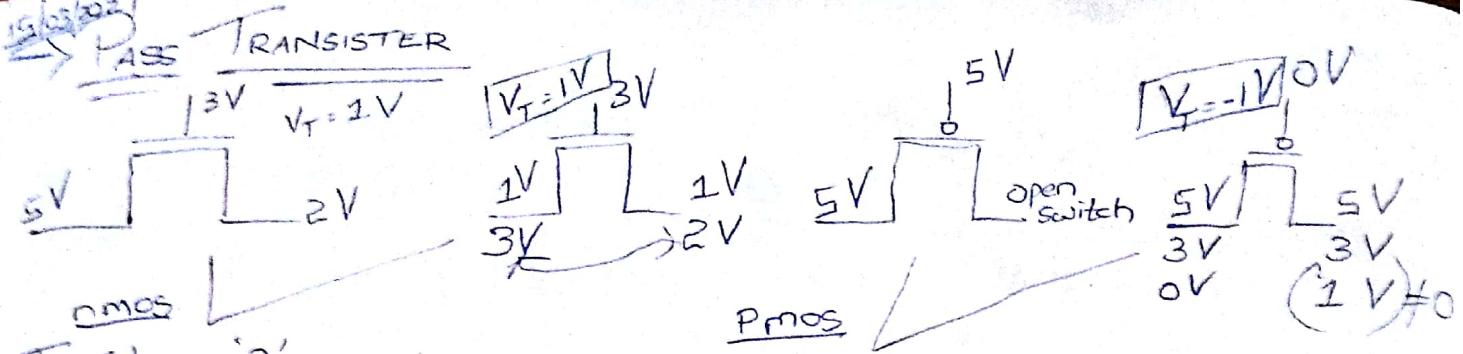


$$3. Y = \overline{\overline{A} \cdot B + C}$$



$$4. Y = \overline{(A+B)C}$$





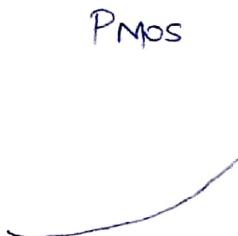
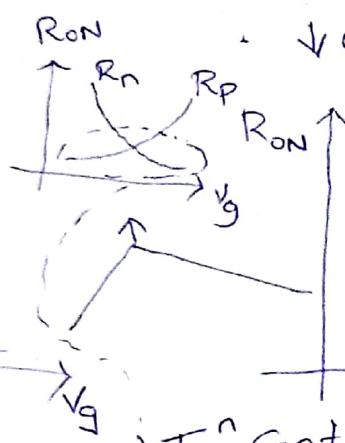
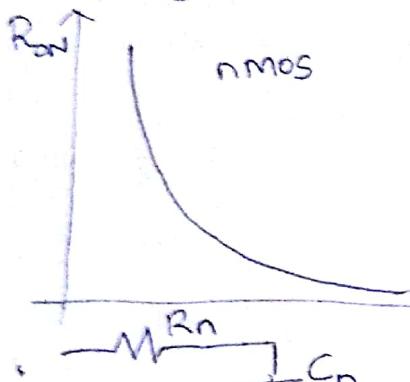
Tx Strong '0'
weak '1'

- So connected to GND

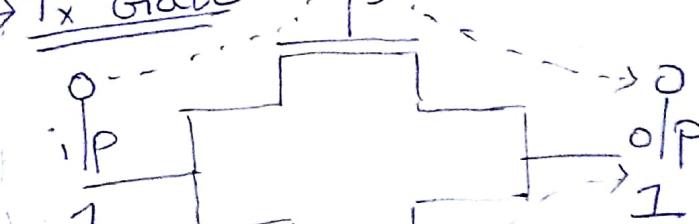
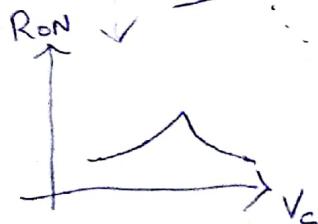
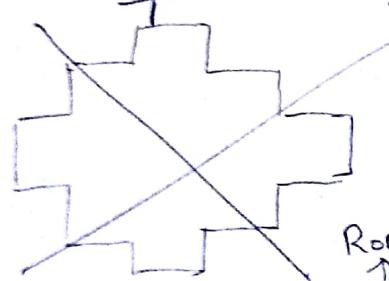
- ↑G Vtg. ↓dp

- Tx Strong 1
weak 0

- So connected to V_{DD}
 - $\downarrow G_1$ vtg. \uparrow op



$$R_p$$



$\frac{\partial}{\partial P}$

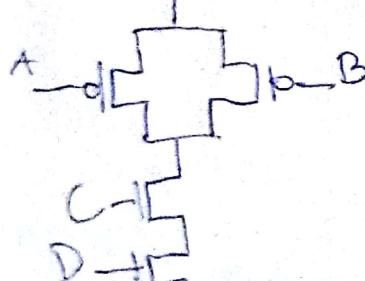
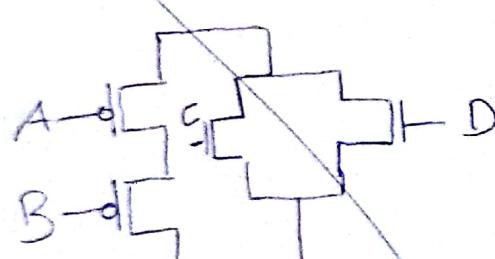
5

3 = T

3

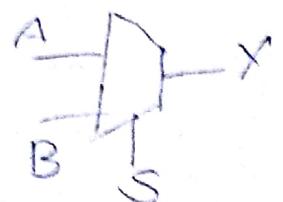
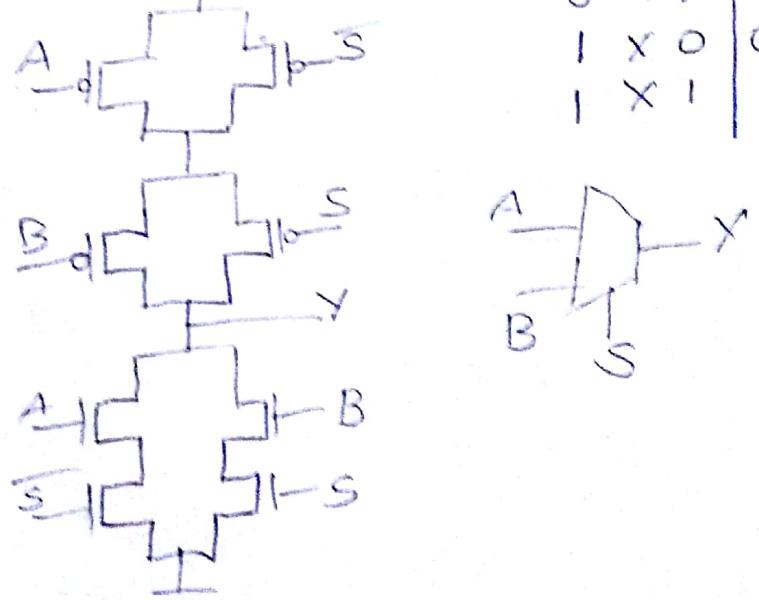
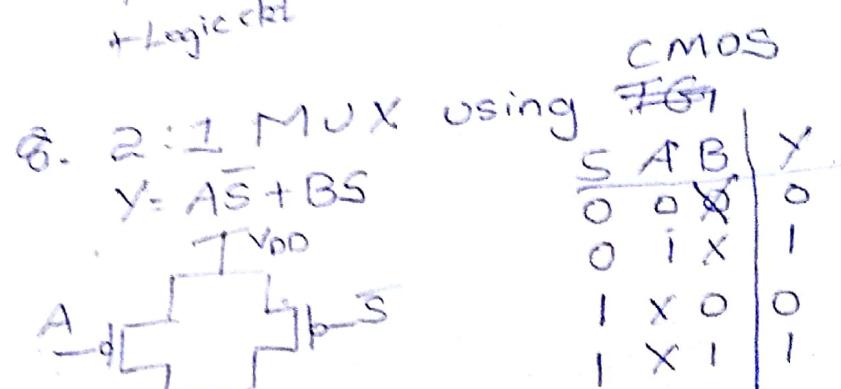
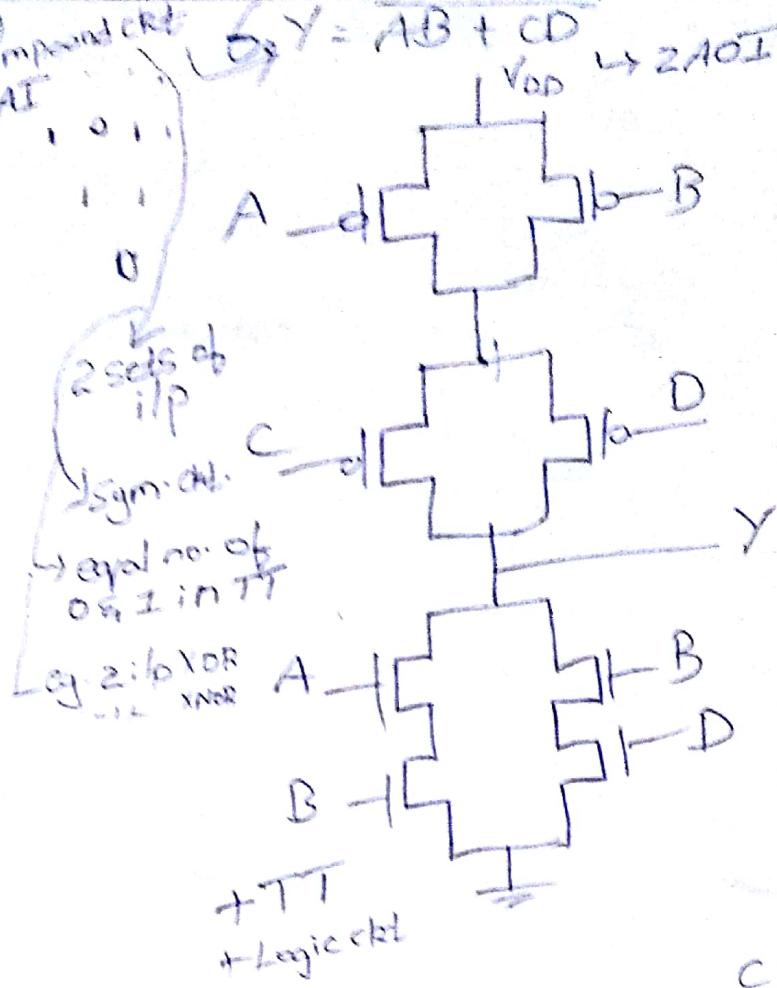
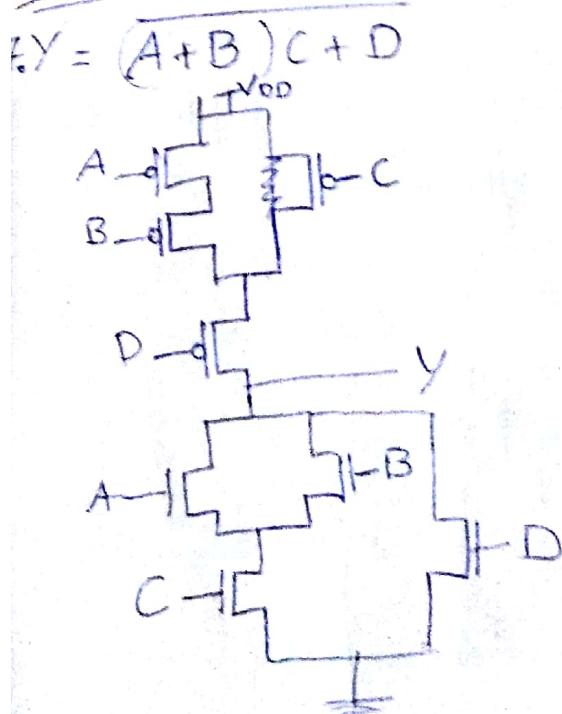
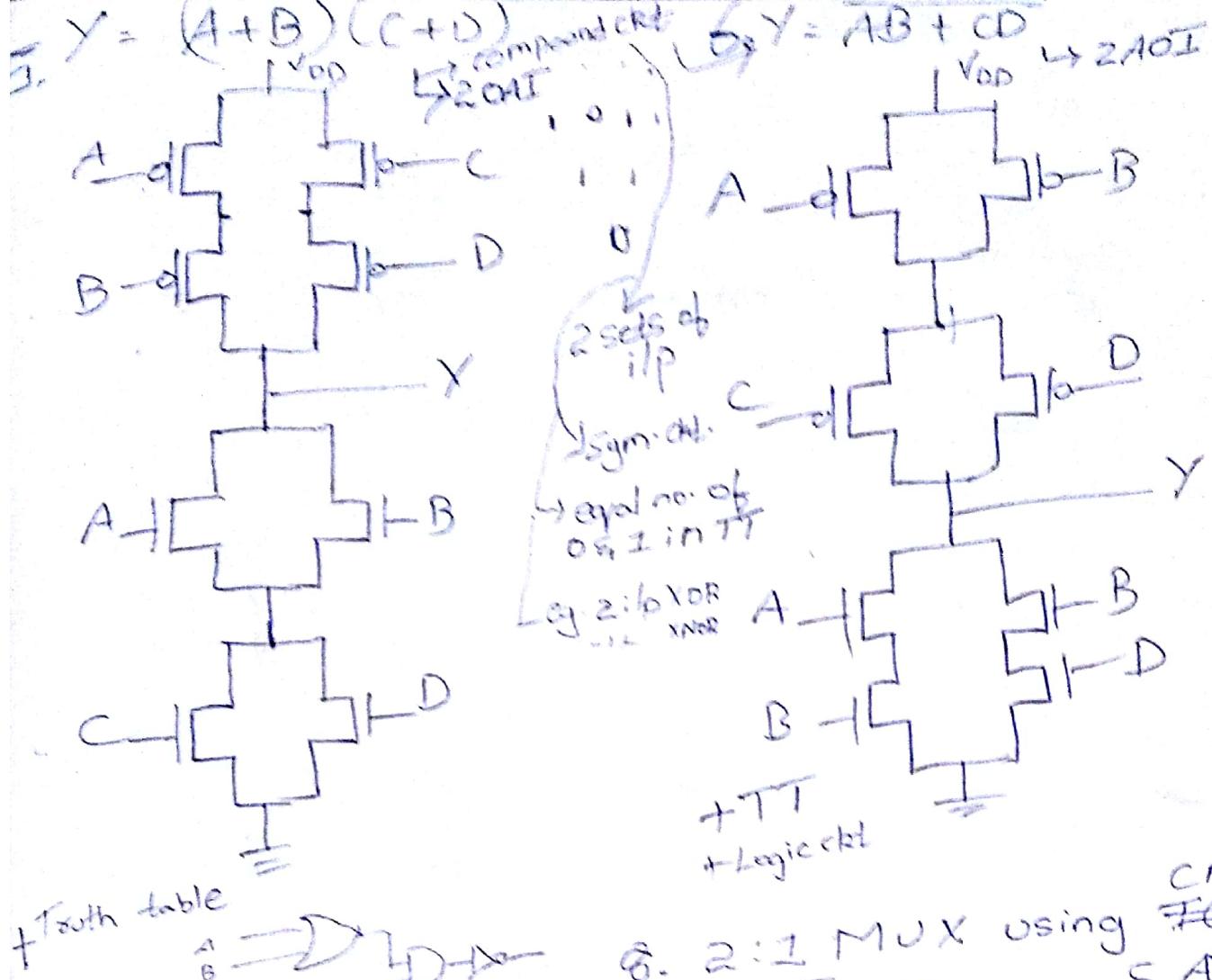
$$\frac{1}{T_2 C_p} \rightarrow -\frac{1}{11} \text{ cm}^2$$

$$= Y = \overline{(A+B)(C+D)}$$

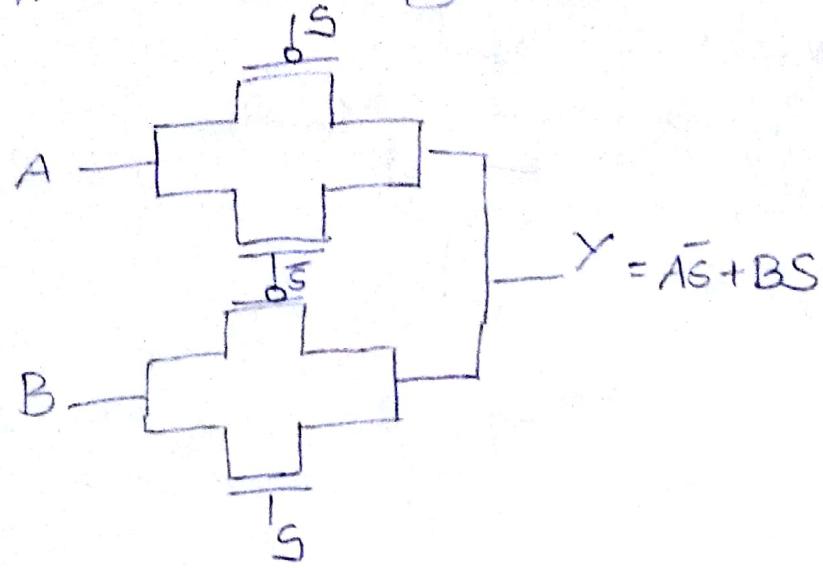


$$-Y = \overline{AB + CD}$$





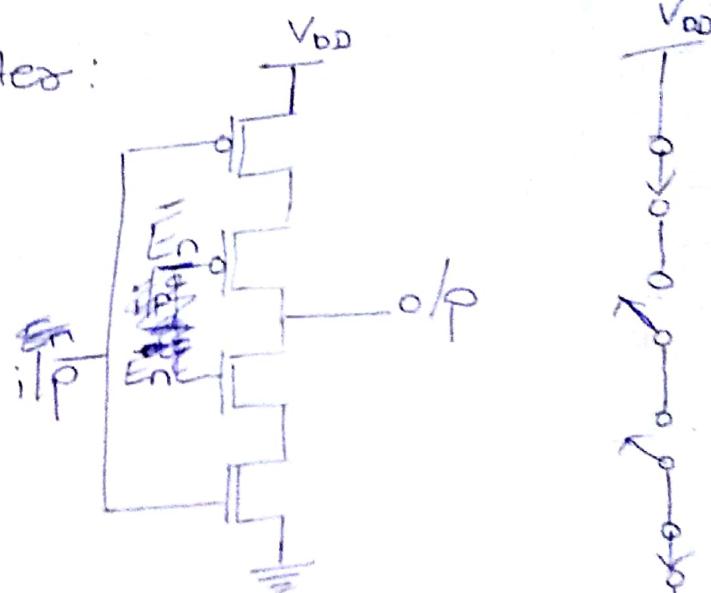
Q. 2:1 MUX using TG



⇒ Tri State Inverter:

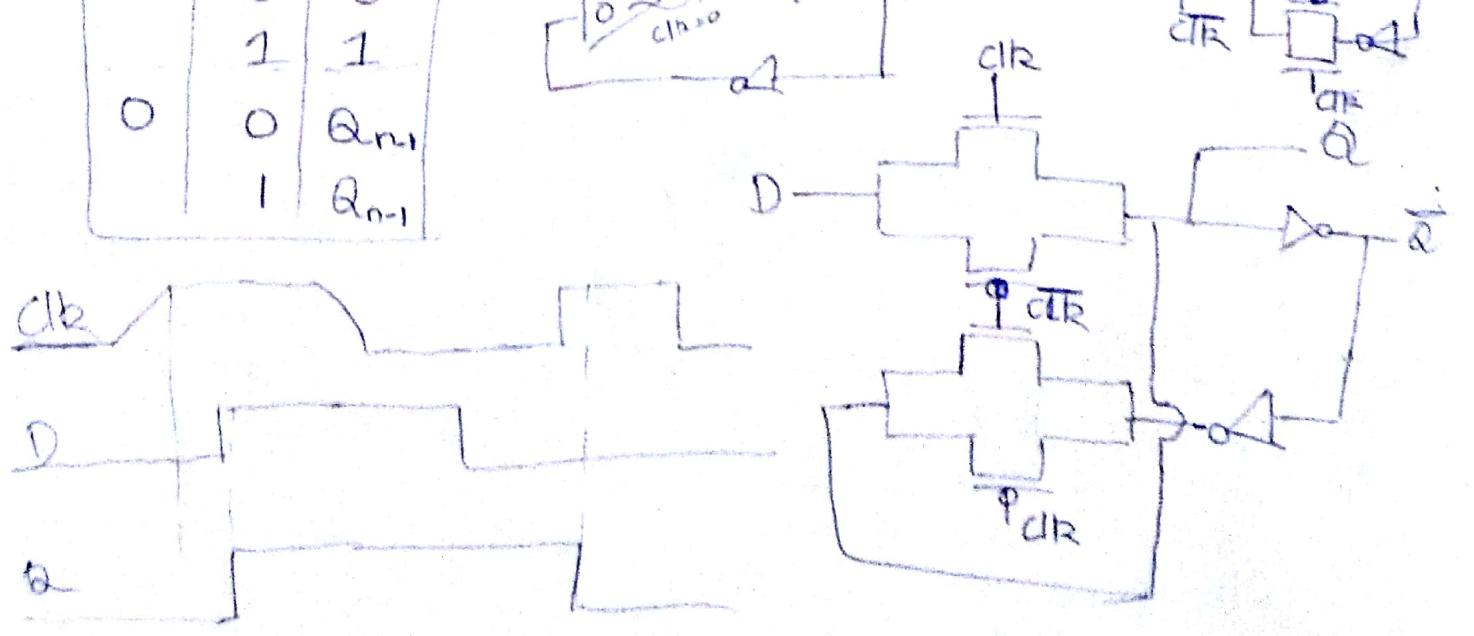
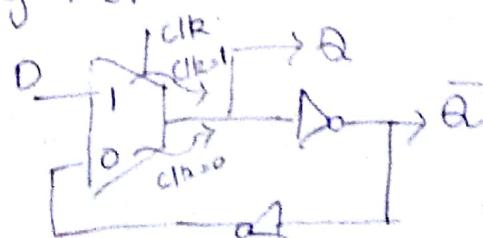


$E_n = D \rightarrow \text{inverted}$
 $E_n = \bar{D} \rightarrow \text{OC}$

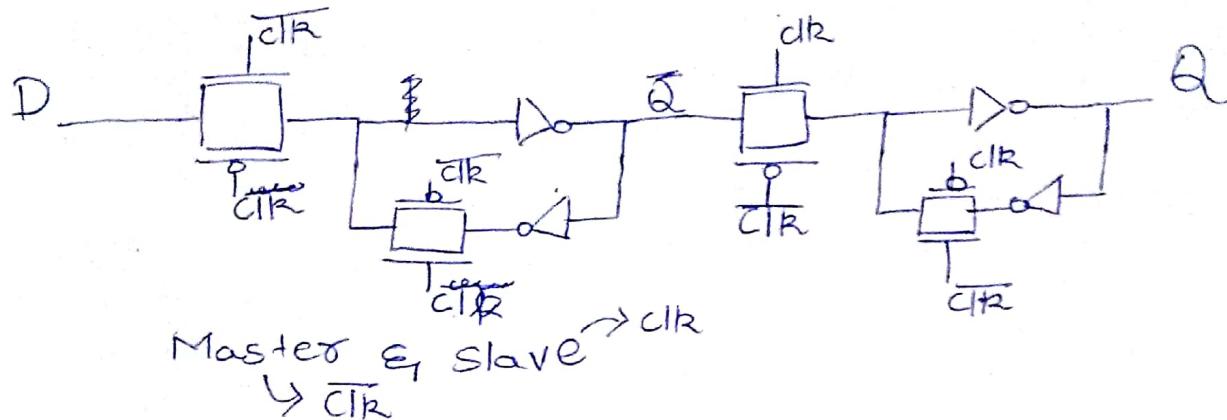
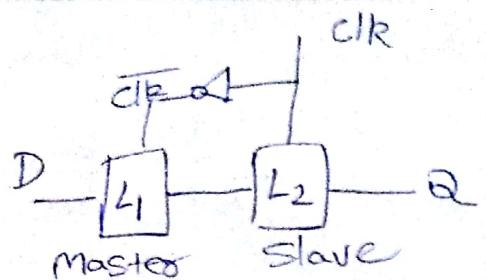
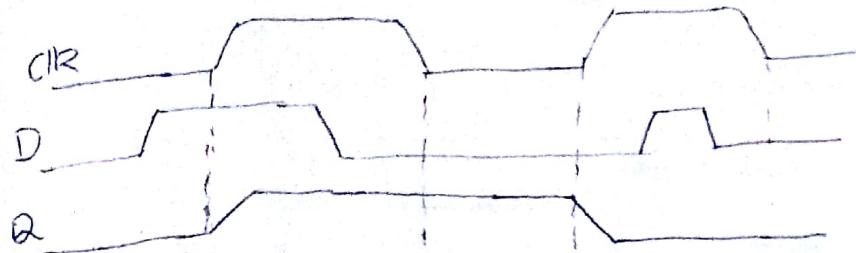


II. D Latch using TG

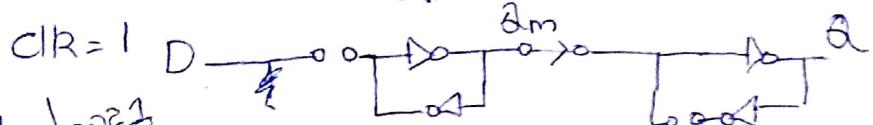
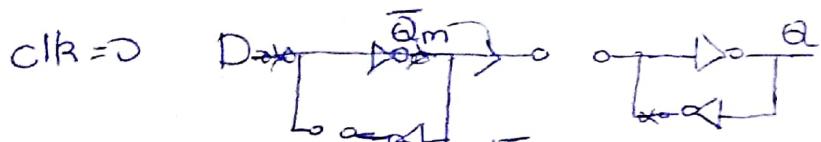
Clk	D	Q_n
1	0	0
1	1	1
0	0	Q_{n+1}
1	1	Q_{n+1}



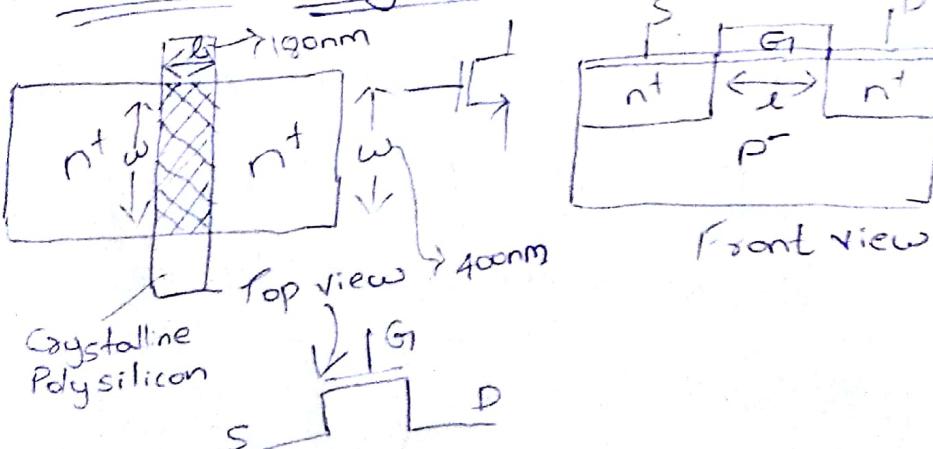
12. D flipflop (edge)

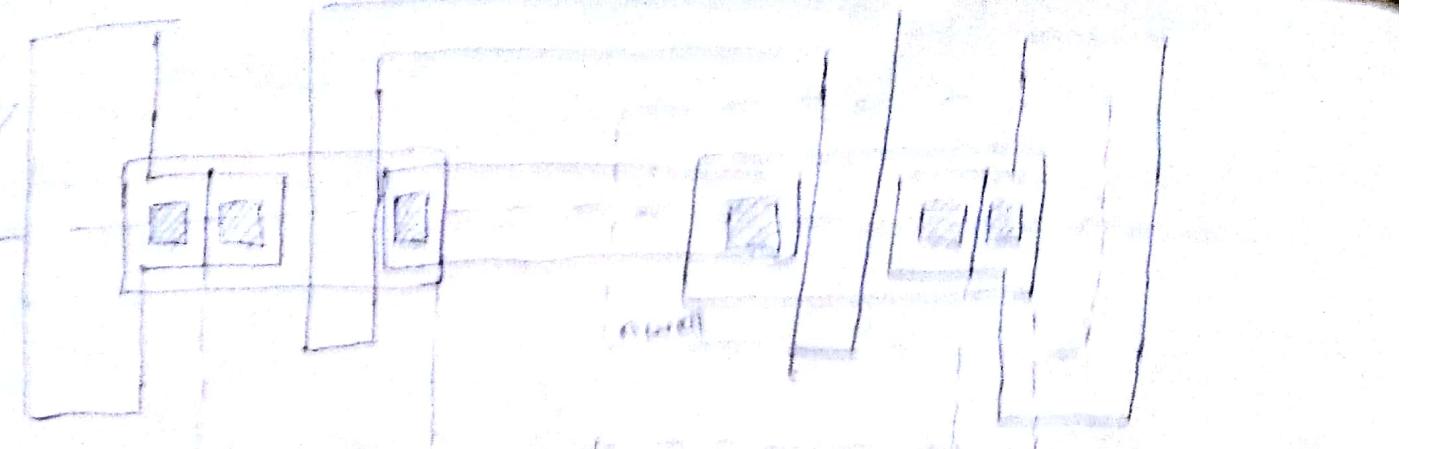


$CTR = 0 \quad D \rightarrow \bar{Q}_m$



10/03/2023
→ CMOS Layout : physical rep. of MOS.





1. SiO_2 + Si_3N_4 -> SiO_2 + Si_3N_4 + Si (etch)

(etch)

2. crystalline poly silicon



3. SiO_2 diffusion



4. SiO_2 diffusion



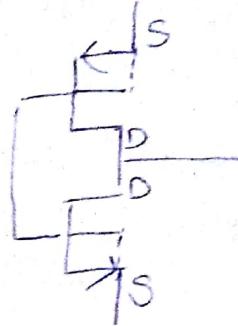
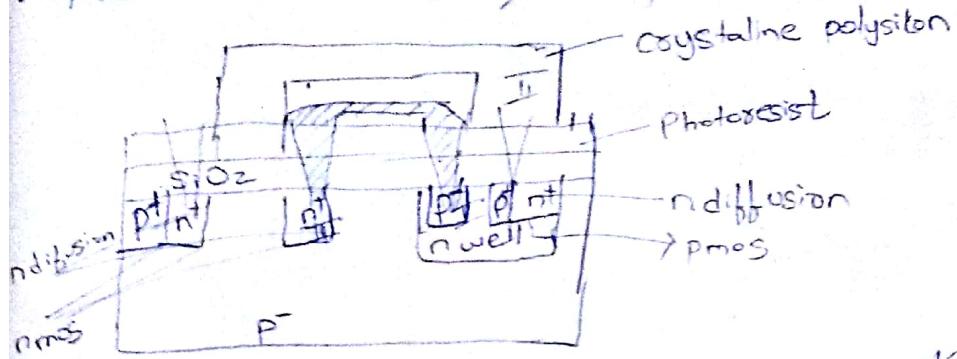
5. Al via contact: metal layer connected to lower SiO_2 layer (metal to SiO_2 diff.)



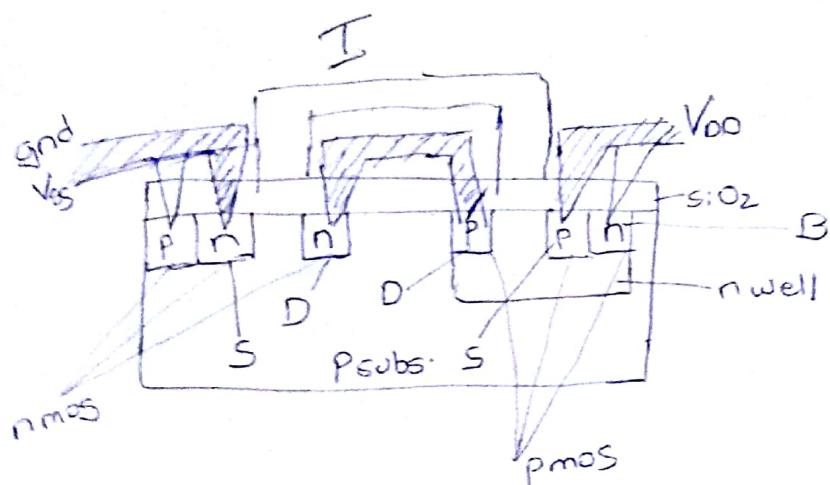
6. Metal layers (via \rightarrow metal to metal contact)



+ve Photoresist \Rightarrow exposed area soluble.



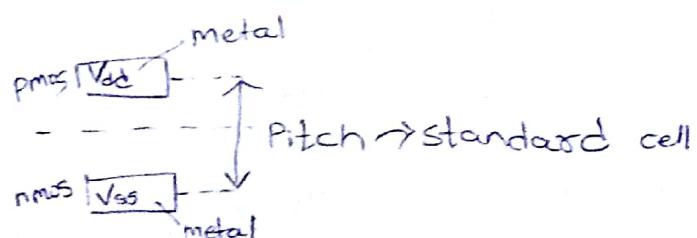
* Key step $\text{SiO}_2 + \text{Photo resist}$



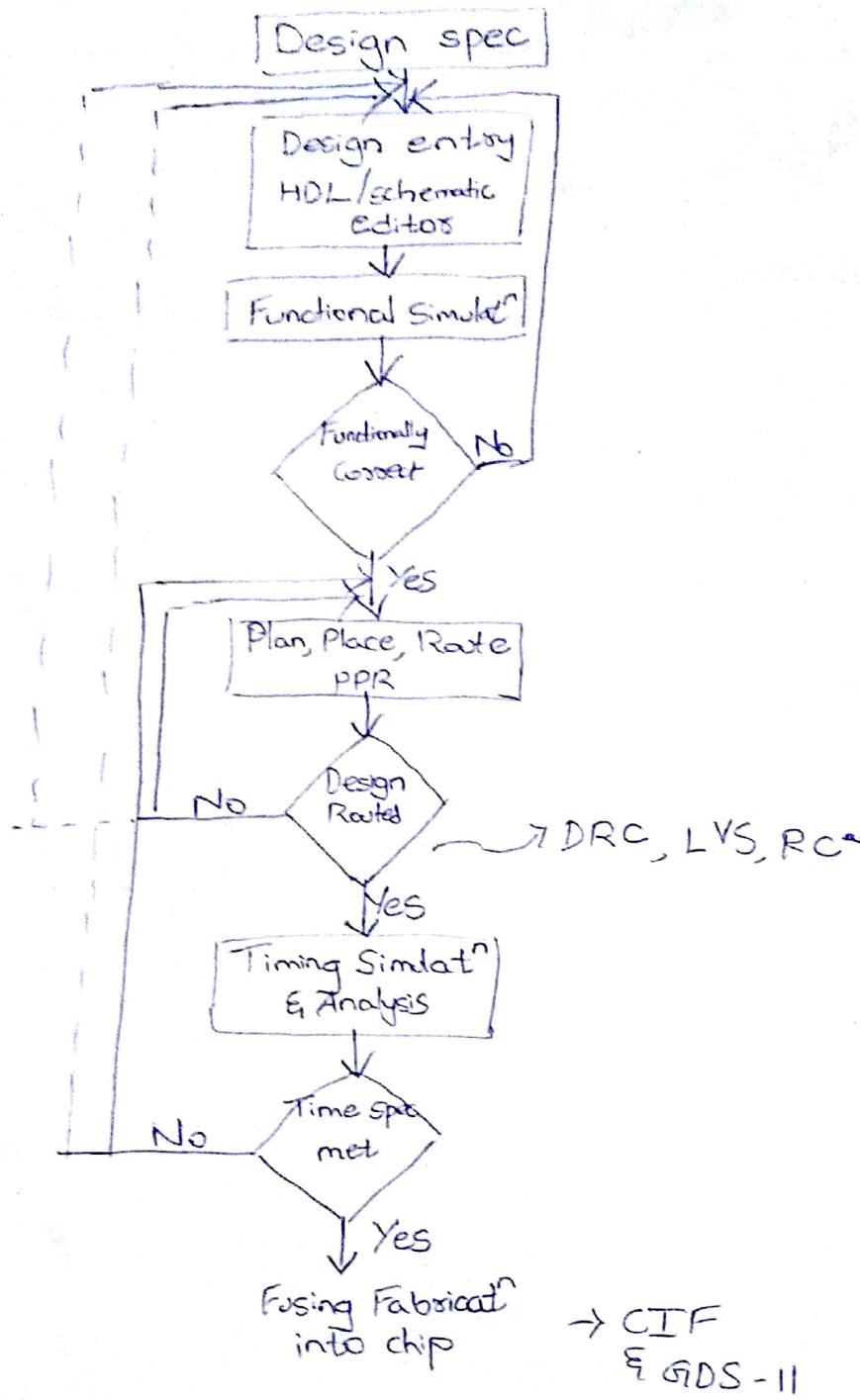
Layout Rules:

• Design rule check (DRC rule): $w \geq 400\text{nm}$, $\lambda \geq 180\text{nm}$

- min. area
- Square layout
- Th.: based on λ
- Above demarcation line pmos below: - - - - - nMOS



→ VLSI Design Flow :

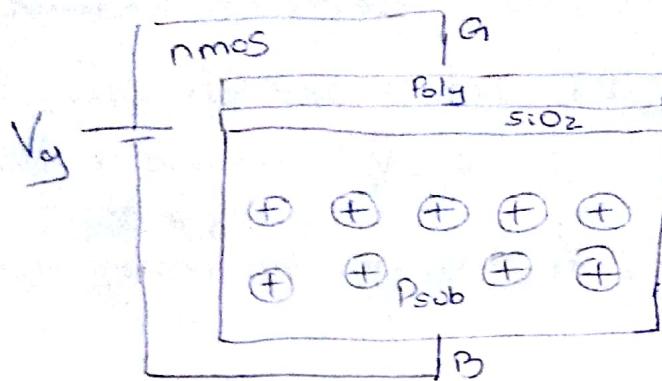


22/03/2021

2. MOS TRASISTER

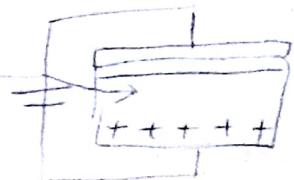
THEORY

Q1.



• $V_g = 0 \rightarrow$ deposition

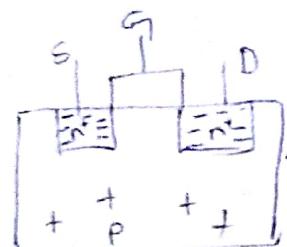
• $V_t > V_g > 0 \rightarrow$ maj. charge carries orient towards downwards leading to depletion region



• $V_g \geq V_t \rightarrow$ channel is formed by minority charge carriers
i.e. p region \rightarrow n region \rightarrow inversion



Q2.



i. $V_g = 0 = V_{DS} \rightarrow \sigma_b \Rightarrow I_D = 0 \rightarrow$ cutoff region

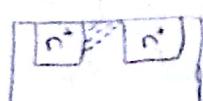
ii. $V_g \geq V_t > 0, V_{DS} = 0 \rightarrow I_D = 0 \because$ no pot. diff. \rightarrow ohmic linear or resistive

iii. $V_t > V_{DS} > 0, V_g = V_t \rightarrow I_D \neq 0 \rightarrow$ linear region $I_D \propto V_{DS}$ w.r.t V_{DS}

IV. $V_{DS} > V_t, V_g \geq V_t \rightarrow$ channel length modulation (pinch off).

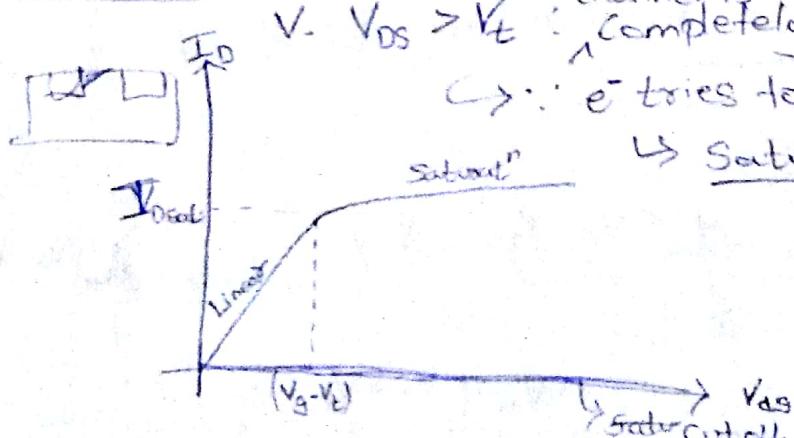
i.e. I_D is indep. of V_{DS}

& I_D is getting saturated.



V. $V_{DS} > V_t$: channel is completely pinched off, but $I_D \neq 0$ $\hookrightarrow \because e^-$ tries to drift (drift current)

\hookrightarrow Saturated.



Notes

→ Ideal I-V char.

- i. Cut off
- ii. Linear/Transistor mode
- iii. Saturation

$V_g > V_t$ $I_D = 0$ $V_g = 0$ $I_D = 0$ Deposit/ Accumulate
 $V_{ds} < V_t$, $I_D \propto V_{ds}$ Inversion

$V_{ds} = V_t$, $V_g > V_{ds} - V_t \rightarrow$ verge of pinched off

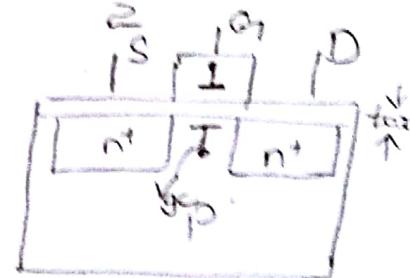
$V_{ds} = V_t$, $V_g > V_{ds} - V_t \rightarrow I_D \propto V_{ds}$

- Cut off : $V_{gs} < V_t$ $I_D = 0$
- Linear : $Q = CV$, $I = \frac{dQ}{dt}$ $\Rightarrow Q_{\text{channel}} = C_g (V_{gc} - V_t) \rightarrow \text{①}$ \rightarrow gate aperture

$$\therefore V_{gc} = \frac{V_{gs} + V_{ds}}{2} = V_g - \frac{V_s + V_d - V_t}{2}$$

$$= V_g - \frac{V_{ds}}{2}$$

$$V_{gc} = V_g - \frac{V_{ds}}{2} \rightarrow \text{②}$$



$\rightarrow \text{①} \Rightarrow Q_{\text{channel}} =$

$$C = \frac{\epsilon A}{d} \quad \& \quad \epsilon_{\text{ox}} = \epsilon_{\text{ox}} = 3.9 \epsilon_0$$

$$A = w \cdot l$$

$$d = t_{\text{ox}}$$

$$\therefore C_g = \frac{\epsilon_{\text{ox}} w l}{t_{\text{ox}}} = C_{\text{ox}} w l ; C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}}$$

Vel. of e^- moving from S to D $v = \mu E$
 $= \mu \frac{V_{ds}}{L}$

time for e^- to move from S to D $t = \frac{L}{v} = \frac{L}{\mu V_{ds}}$

Subs. ① to ④ in ③

$$I = \frac{C_{\text{ox}} w l (V_g - \frac{V_{ds}}{2} - V_t)}{\frac{L^2}{\mu V_{ds}}} = \frac{C_{\text{ox}} w l (V_g - V_t - \frac{V_{ds}}{2})}{L}$$

$$= C_{\text{ox}} w l \mu V_{ds} (V_g - V_t - \frac{V_{ds}}{2})$$

$$\boxed{I = \mu C_{ox} \frac{w}{L} \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}} \rightarrow \textcircled{A}$$

Saturation: $V_{ds} = V_{gs} - V_t$

$$\textcircled{A} \Rightarrow I = \mu C_{ox} \left(\frac{w}{L} \right) \left(\frac{V_{gs} - V_t}{2} \right)^2$$

$$\boxed{I_{Dsat} = \frac{\mu C_{ox} w}{L} (V_{gs} - V_t)^2}$$

$$\text{or } \boxed{I_{Dsat} = \frac{\beta}{2} (V_{gs} - V_t)^2} ; \beta = \mu_n C_{ox} \frac{w}{L} = \beta_n$$

mobility

\downarrow
nmos

$$\beta_p = \mu_p C_{ox} \frac{w}{L}$$

\downarrow
pmos

$$\text{i.e. } t_g > t_b \quad \begin{array}{l} \text{e}^- & \text{v} > \text{holes' v} \\ \text{v}_{e^-} = 2.5 v_h \end{array}$$

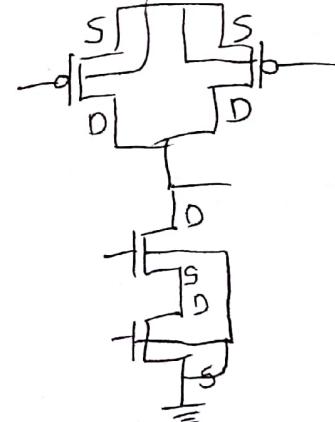
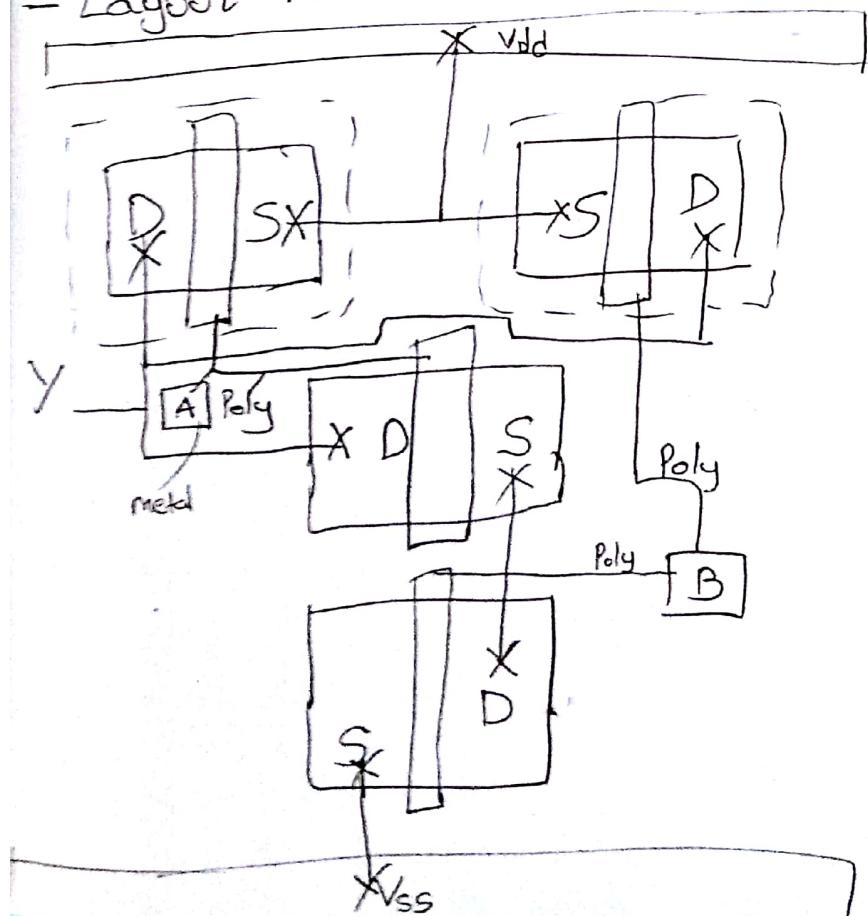
$$\text{w}_p = 2.5 w_n$$

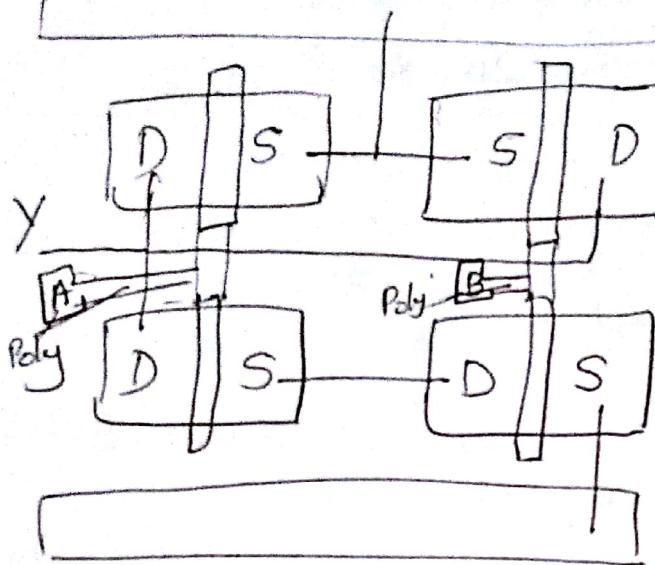
\downarrow
for $\mu_n = \mu_p$

$$\text{i.e. } t_g = t_b$$

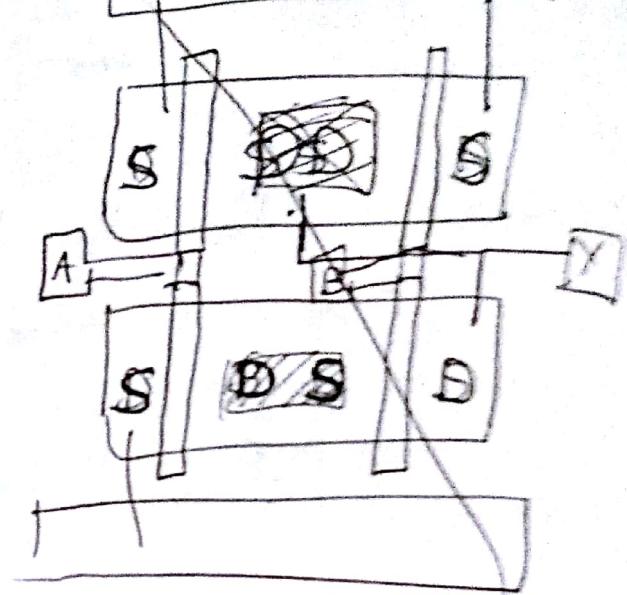
I C - 3

- Layout NAND:

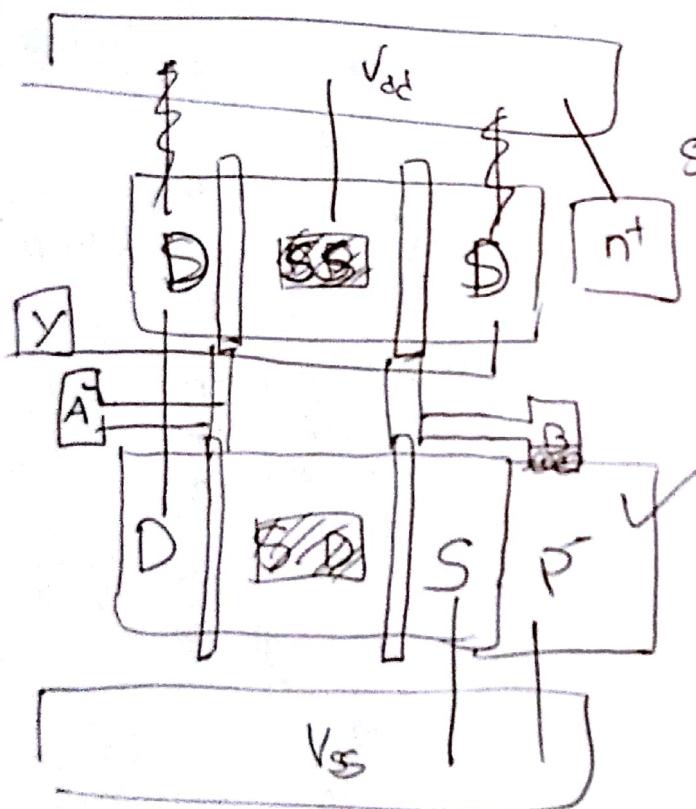




Abundant ↗



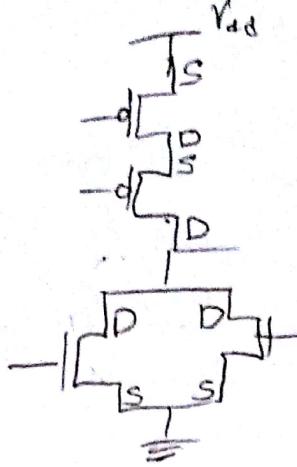
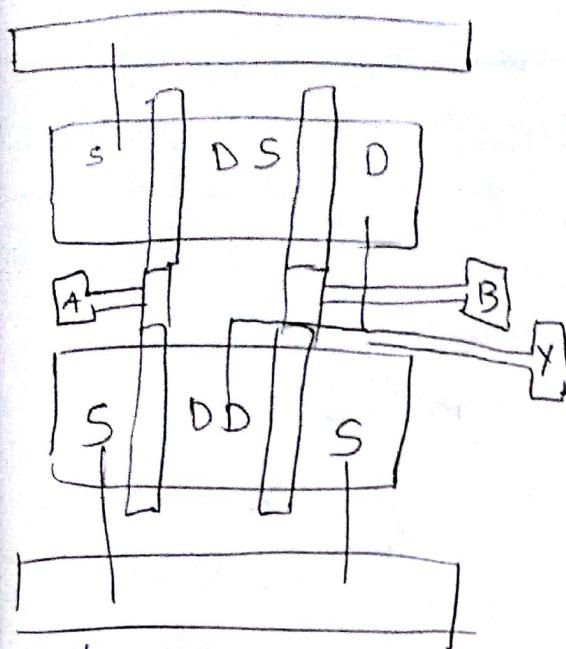
Shared ↗



shared



- Layout NOR



30/03/2021

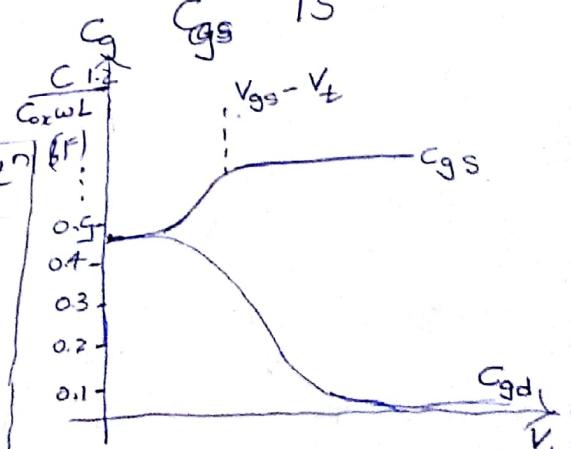
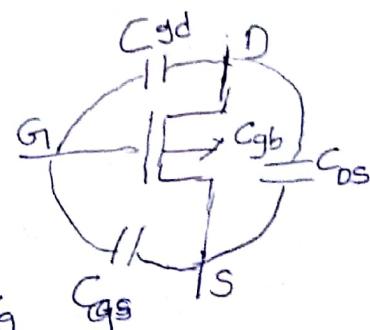
→ C-V Characteristics :

C_{gb} , C_{gs} , C_{gd} : → dominant
internal cap. → $1.5-2 \text{ fF}$

external cap. :

$$\left. \begin{array}{l} C_C \\ C_{in} \\ C_E \end{array} \right\} \uparrow \mu F$$

$$C_m = C_{gb} + C_{gs} + C_{gd}$$



C_{in}	Cutoff	Linear	Saturated
C_{gb}	C_0	$C_0/2$	$2C_0/3$
C_{gs}	0	$C_0/2$	0
C_{gd}	0	$C_0/2$	$2/3 C_0$
C_0	C_{gb}	$C_{gs} + C_{gd}$	$2/3 C_{gs}$

$$C_g = \frac{C_{ox} W L}{180 \text{ nm}} \quad ; \quad C_{ox} = \frac{\epsilon_{ox}}{L} \rightarrow \text{fixed}$$

$$= C_{perimeter} \quad \hookrightarrow 1.5-2 \text{ fF}$$

31/03/2021

→ DC Char. of CMOS Inverter

	Cutoff	Linear	Saturation
nMOS	$V_{gs} < V_{tn}$ $\Rightarrow V_{in} < V_{tn}$	$V_{gs} > V_{tn}$ $\Rightarrow V_{in} > V_{tn}$ $\& V_{ds} < V_{gs} - V_{tn}$ $V_{out} < V_{gs} - V_{tn}$	$V_{gs} > V_{tn}$ $\Rightarrow V_{in} > V_{tn}$ $\& V_{ds} \geq V_{gs} - V_{tn}$ $\Rightarrow V_{out} > V_{gs} - V_{tn}$
PMOS	$V_{gs} > V_{tp}$ $\Rightarrow V_{in} > V_{tp} + V_{dd}$	$V_{gs} < V_{tp}$ $\Rightarrow V_{in} < V_{tp} + V_{dd}$ $\& V_{ds} > V_{gs} - V_{tp}$ $\Rightarrow V_{out} > V_{in} - V_{tp}$	$V_{gs} < V_{tp}$ $\Rightarrow V_{in} < V_{tp} + V_{dd}$ $\& V_{ds} < V_{gs} - V_{tp}$ $\Rightarrow V_{out} < V_{in} - V_{tp}$

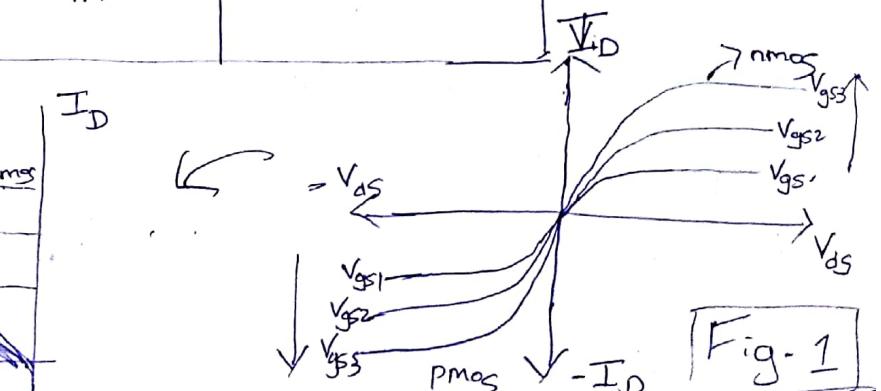
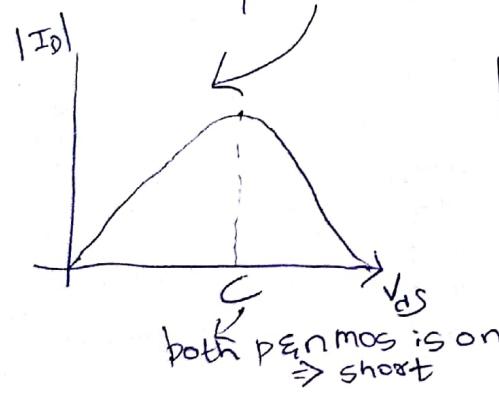
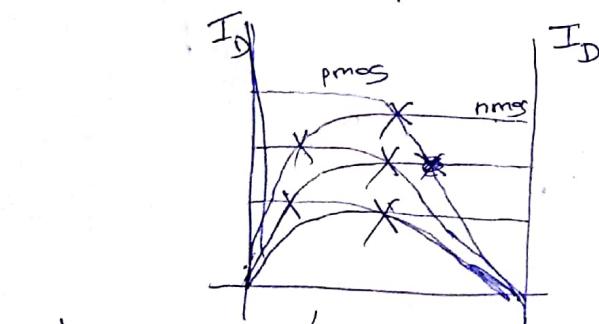
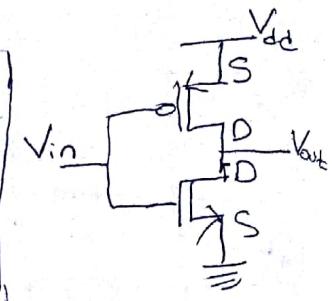


Fig-1

Region	i/p V/g	PMOS	nMOS	o/p V/g
A	$0 \leq V_{in} < V_{tn}$	lin.	cutoff	V_{dd}
B	$V_{tn} \leq V_{in} < \frac{V_{dd}}{2}$	lin.	Sat.	$V_{out} > \frac{V_{dd}}{2}$
C	$\frac{V_{dd}}{2}$	Sat.	Sat.	steep
D	$\frac{V_{dd}}{2} < V_{in} < V_{dd} - V_{tp}$	Sat.	lin.	$V_{out} < \frac{V_{dd}}{2}$
E	$V_{dd} - V_{tp} \leq V_{in} \leq V_{dd}$	cutoff	lin.	0

07/07/2021

→ Non-ideal IV effect (2, 4) (74)

1. Channel Length Modulation

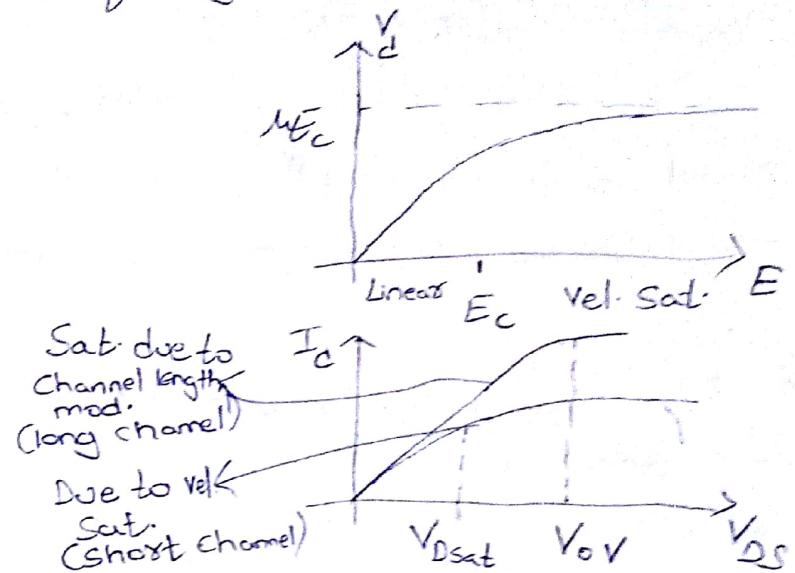
- During / after sat. region

- Slope of sat. region of Fig. 1

2. Velocity Sat. & 1.

- at Sat. region

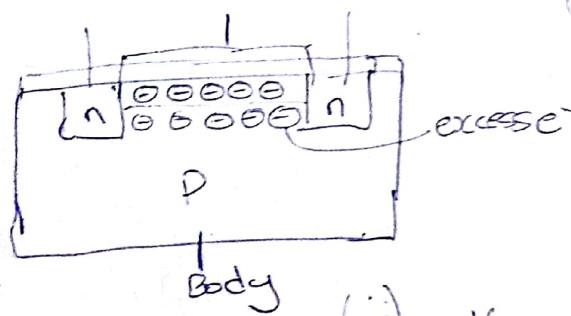
$$= \frac{V_{ds}}{\text{total length}}$$



3. Mobility Degradatⁿ (Surface Scattering)

- \because Vertical field $V_{gs} = \frac{V_{gs}}{t_{ox}}$
- \downarrow Oxide thickness \uparrow Scattering \uparrow

4. Body / Back Gate Effect.



(i). Source > 0 , Body $V_{bg} > 0$

- \Rightarrow leakage current
- $\Rightarrow e^-$ pull back to body
- \Rightarrow channel is dissolved
- To get back channel $\uparrow V_{gs}$
i.e. V_t is \uparrow

(ii). $V_{ss} = 0$, $V_B < 0$, $V_{ds} > 0$

- \Rightarrow Both rev. bias
- $\Rightarrow e^-$ move back towards channel
- i.e. channel is formed $< V_t$
- $\Rightarrow V_t \downarrow$

5. Leakage Current

- Juncⁿ leakage

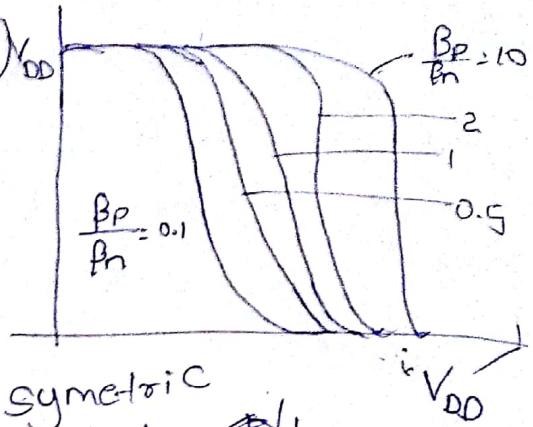
- Gate - \uparrow $\therefore \uparrow V_{gs} \Rightarrow e^-$ channel \leftrightarrow gate

- Subthreshold - \downarrow \therefore even though mos is turned off
i.e. $V_{gs} = 0$

→ Beta Ratio (2.5.2) (90)

$$\beta = \alpha \cos \frac{\omega}{L}$$

$$\gamma = \frac{\beta_p}{\beta_n} = 1 \Rightarrow t_b = t_{\bar{b}}$$



↳ normal skew inverter = skew symmetric

• $\gamma > 1 \rightarrow \beta_p > \beta_n \rightarrow \text{HI-skew inverter}$

• $\gamma < 1 \rightarrow \beta_p < \beta_n \rightarrow \text{LO-skew inverter}$

* Note

$$W\alpha/R$$

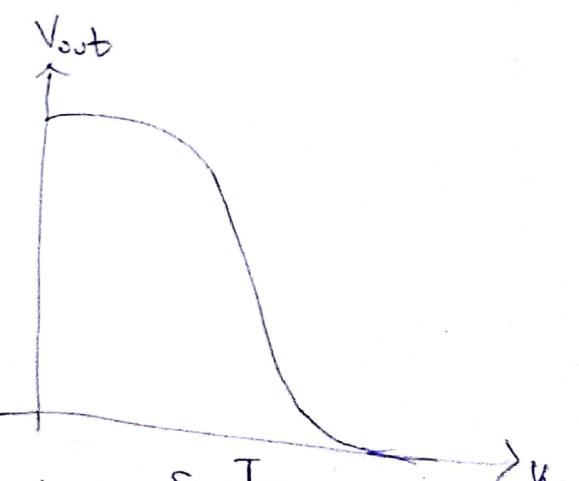
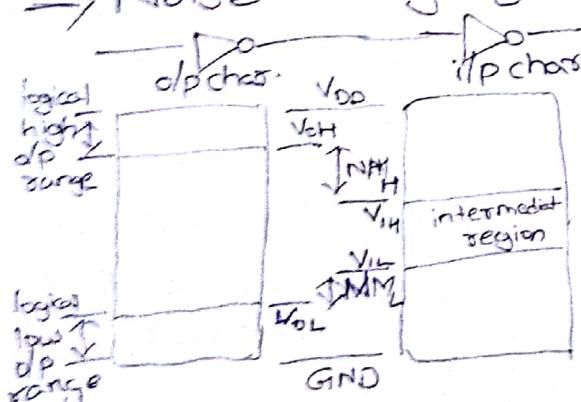
$$L \propto R \quad \& \quad W \propto C$$

- Changing $L \rightarrow$ changing R
- $W \Rightarrow C$

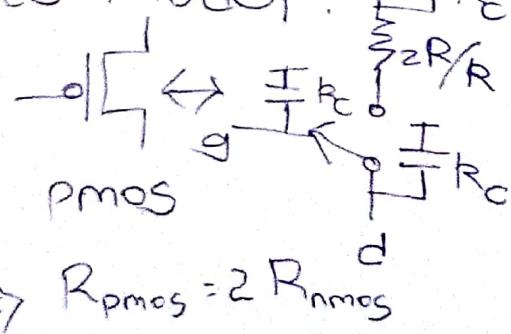
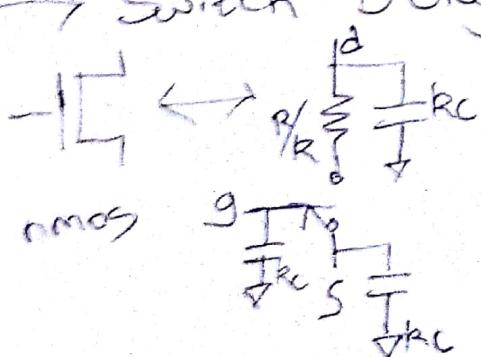
• 2 trans. in series \Rightarrow

obot 2021

→ Noise Margin (2.5.3) (91)

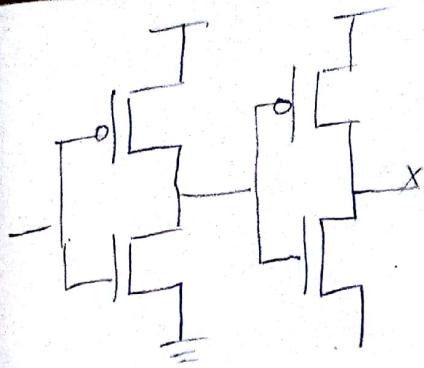


→ Switch Delay RC Model:

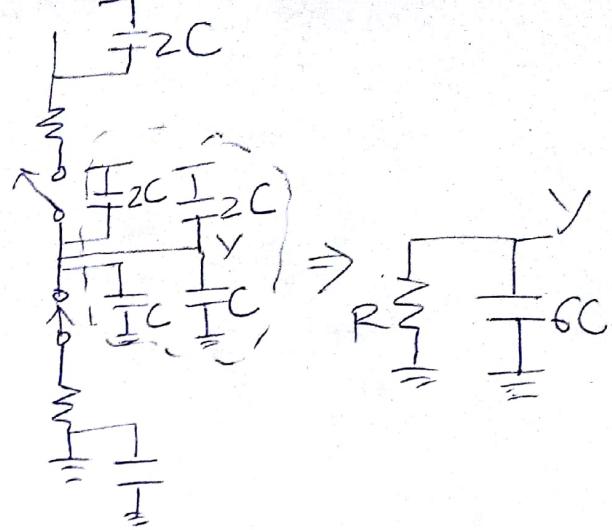


$$\Rightarrow R_{pmos} = 2 R_{nmos}$$

• To make R of PMOS, double the W of PMOS



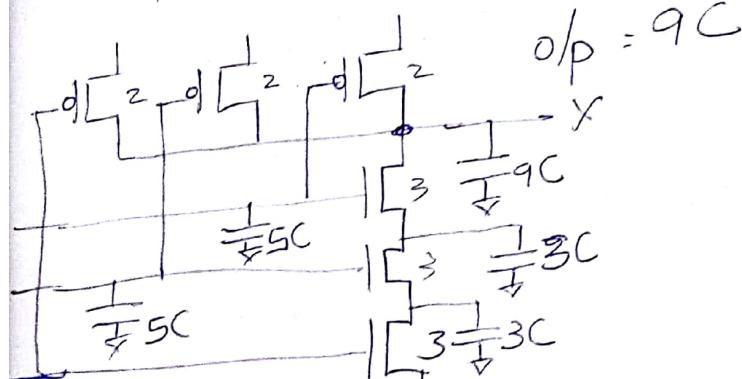
$$W_p = 2W_h$$



Fanout of 1
(FO1)

$$FO4 : [2C + C + 4(2C + C)] = 15C$$

- 3 i/p NAND i/p = 5C

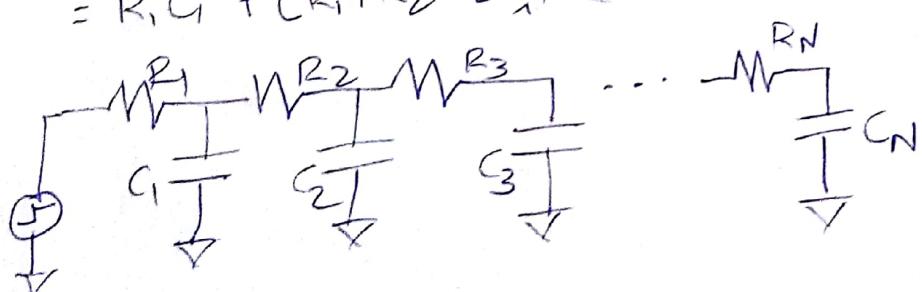


$\frac{1}{8}SC$ $\frac{1}{4}SC$ $\frac{1}{2}SC$

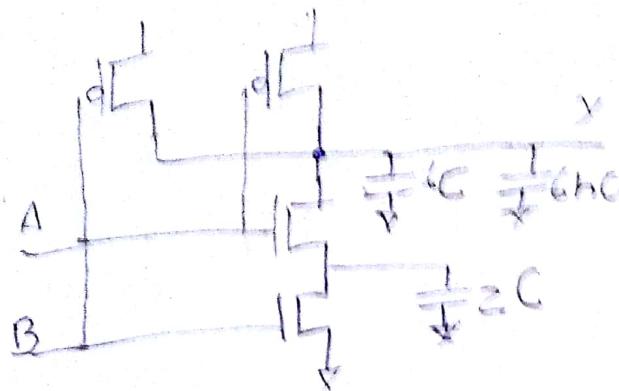
→ Elmore Delay Model 1

$$t_{pd} = \sum_{node_i} (R_{i-to-source} C_i)$$

$$= R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2 + R_3 + \dots + R_N) C_N$$



- 2:1P NAND with FO4



D → D_n
n copies

$$\frac{R}{(6+4h)C} \quad \frac{R_2}{R_2 + \frac{1}{2C}} \quad \frac{1}{(6+4h)C}$$

$$t_{pd} = (6+4h)RC \quad t_{pd} = (7+4h)RC$$

→ Linear Delay Model (4.4) (195)

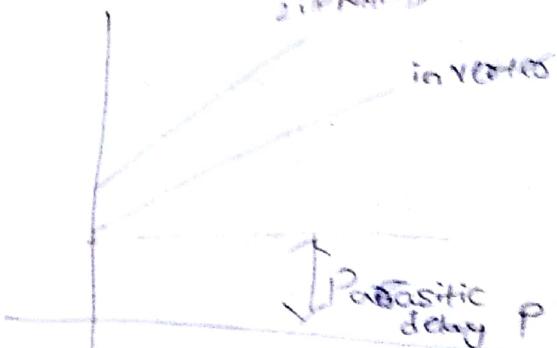
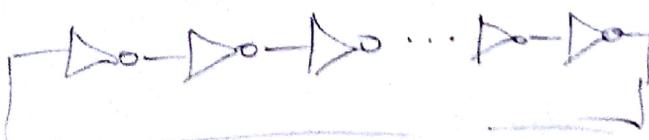
$$d = b + P \quad ; \quad b = gh$$

inverter
 $\frac{1}{2ND}$ part

3:1P NAND

$$d = \frac{days}{2}$$

eg. i. Ring Osc.



g : logical effort = 1

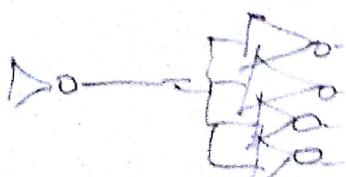
h : ele. eff. = 3/2 = 1

P : Parasitic = 1

d : Stage delay = 1 + 1 = 2

fosc : freq. = $\frac{1}{2ND} = \frac{1}{2N} = \frac{1}{4N}$

ii. FO4 inv.

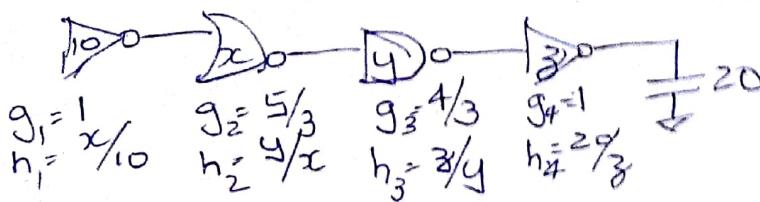


$$g = 1 \\ h = 4 \\ P = 5 \\ d = 5$$

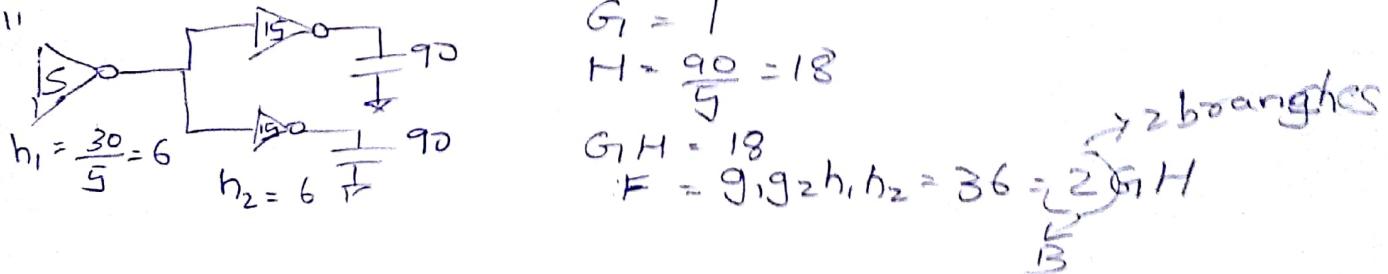
= Multi Stage Logic N/W

- Path Logical Effort : $G_i = \prod g_i \rightarrow g_1, g_2, g_3, g_4$
- " Ele. - " : $H = \frac{\text{Con paths}}{\text{Cin path}}$
- Path Effort $F = \prod b_i = \prod g_i h_i = GH$

eg i:



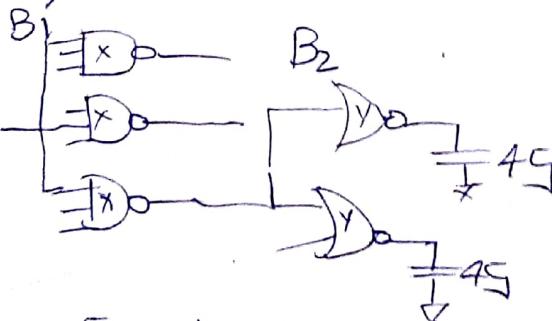
eg ii:



Branching effort: $B = \prod b_i$, $b = \frac{\text{Con path} + \text{Copp path}}{\text{Con path}}$, $F = BGH$

- Path eff. delay = $D_F = \sum b_i$
 - Path para. delay = $P = \sum p_i$
 - Path Delay = $D = \sum d_i = D_F + P$
 - min. delay of N stage path = $D = NF^{\frac{1}{N}} + P$ \uparrow same effort
- \hookrightarrow i.e. when each stage has same delay = $F^{\frac{1}{N}}$

eg iii.



$$g_1 = 4/3 \quad g_2 = 5/3 \quad g_3 = 5/3$$

$$G = 100/27$$

$$H = 45/8$$

$$B = 3 \times 2 = 6$$

$$F = BGH = 125$$

$$f = (125)^{1/3} = 5$$

$$D = B(f) + P = 15 + 7 = 22$$

$$P = \sum p_i = 2 + 3 + 2 = 7$$

each delay = 5 $\rightarrow d_3, d_2, d_1$

$$h_3 = 45/y \quad g_3 = 5/3$$

$$d_3 = h_3 g_3 \Rightarrow 5 = \frac{45}{y} \times \frac{5}{3} \Rightarrow y = 15$$

$$\cancel{h_2 = \frac{15}{x} \quad g_2 = 5/3}$$

$$d_2 = h_2 g_2 \Rightarrow 5 = \frac{15}{x} \times \frac{5}{3} \Rightarrow x = 5$$