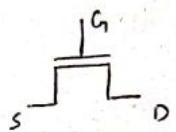
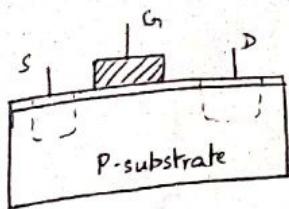
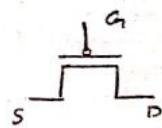
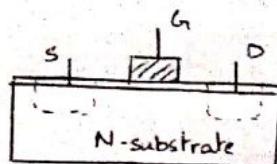


N type -

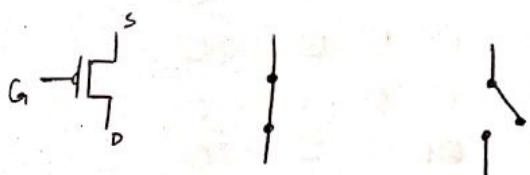
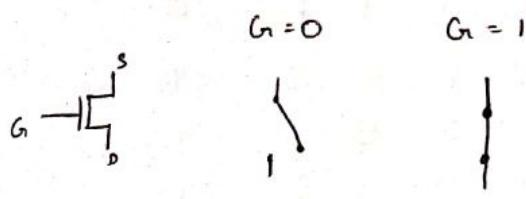


Pull Up Because Up.

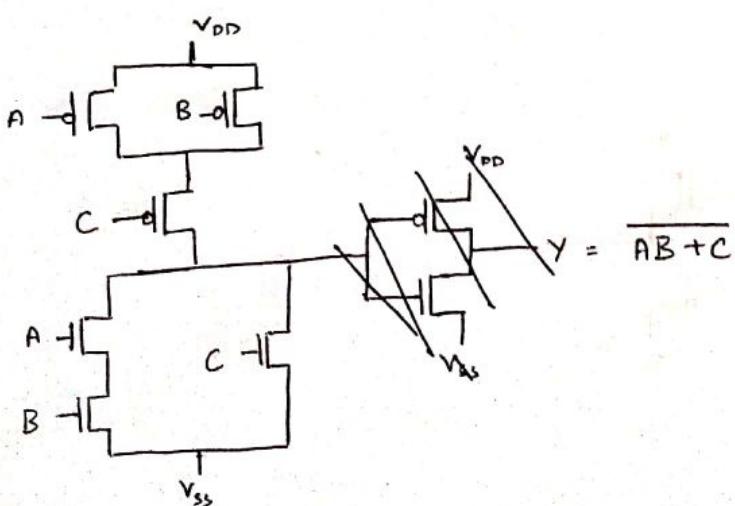
P type -



Pull Up Down

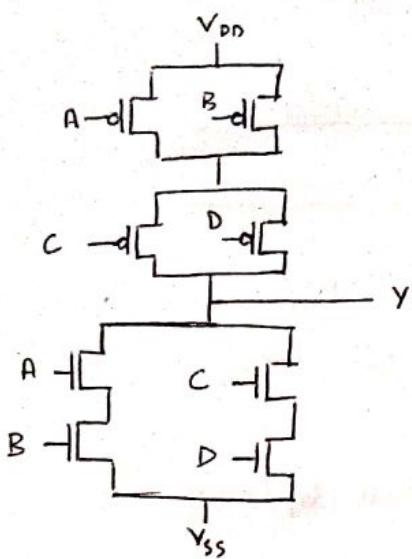


$$Y = \overline{AB + C}$$



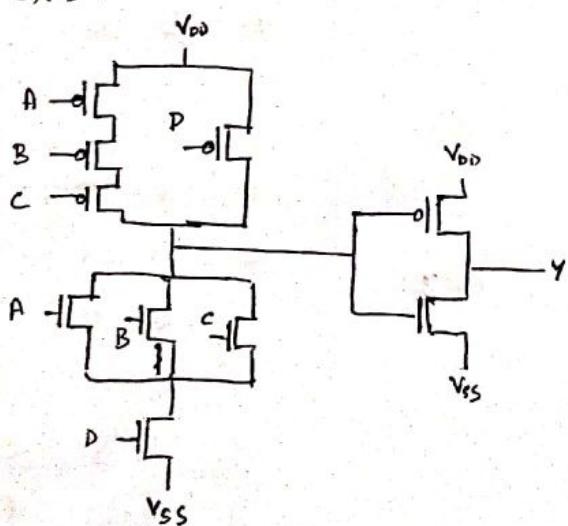
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

$$Y = \overline{AB} + CD$$

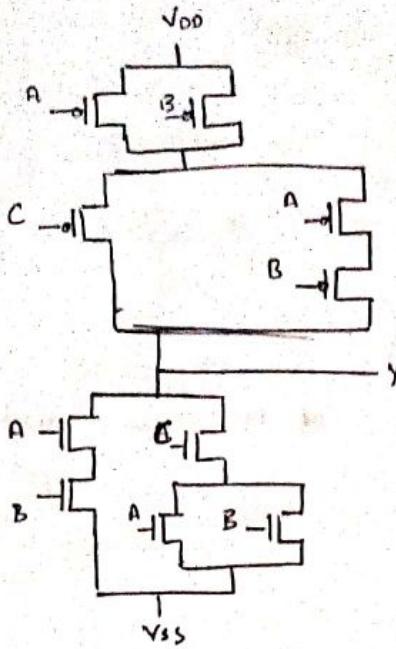


A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

$$Y = (A+B+C).D$$



$$y = AB + C(A+B)$$



Write the CMOS transistor level for 3 input XOR gate.

$$y = A \oplus B \oplus C.$$

$$= (\overline{AB} + \overline{A}\overline{B})C + \overline{C}(A\overline{B} + \overline{A}B).$$

$$= (\overline{AB} \cdot \overline{A}\overline{B})C + \overline{C}(A\overline{B} + \overline{A}B).$$

$$= (\overline{A} + B)(\overline{A} + \overline{B}).C + \overline{C}A\overline{B} + \overline{A}\overline{B}\overline{C}$$

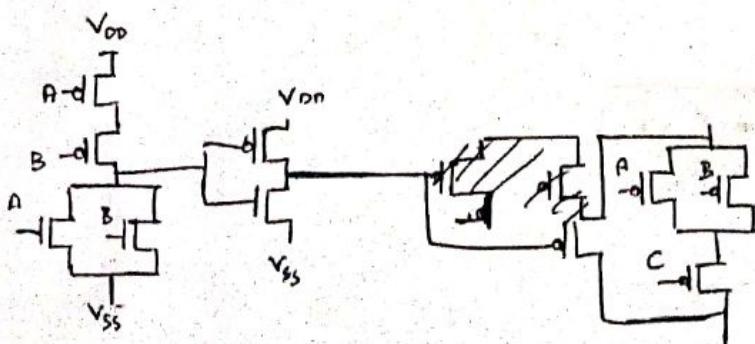
$$= \overline{A}\overline{B}C + BAC + \overline{C}A\overline{B} + \overline{A}\overline{B}\overline{C}$$

$$= A(\overline{BC} + \overline{B}\overline{C}) + \overline{A}\overline{C}$$

$$\text{XNOR} \Rightarrow (\overline{AB} + AB)C + (\overline{A}\overline{B} + AB)\overline{C}$$

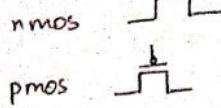
$$= \overline{\overline{AB} + AB + C} = \overline{(\overline{A} + B)} + AB + C$$

$$= \overline{(\overline{A} + B)} \cdot (\overline{AB + C})$$

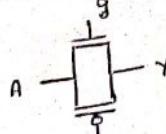
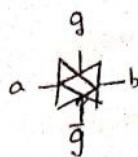


Pass transistor and Transmission Gate -

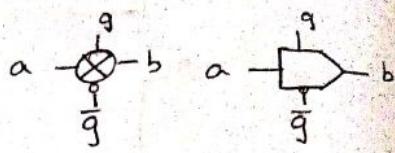
Pass transistor -



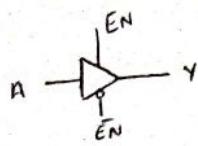
transmission gate



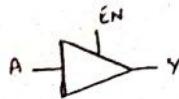
acts like a buffer.



Tristate buffer -



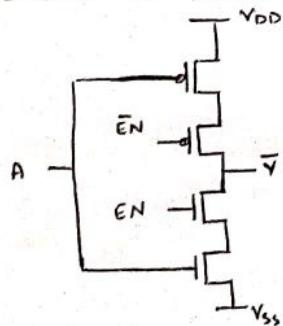
(or)



EN / EN̄	A	Y
1/0	1	1
1/0	0	0
0/1	1	Z
0/1	0	Z

④ No clue, read it yourself.

CMOS - circuit in terms of tristate inverter buffer. ④ doesn't make sense, read it.

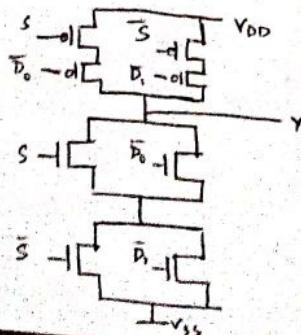


Circuit for $Y = \bar{S}D_0 + SD_1$

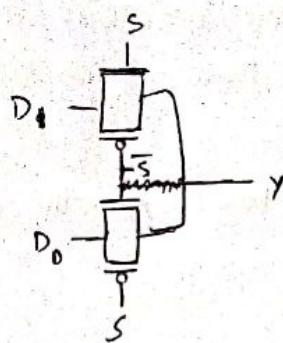
S	D ₀	D ₁
0	X	-
1	-	X

$$\bar{Y} = \overline{\bar{S}D_0 + SD_1}$$

$$= (\bar{S}D_0 \cdot \bar{S}D_1) = (S + \bar{D}_0) \cdot (\bar{S} + \bar{D}_1)$$



MUX



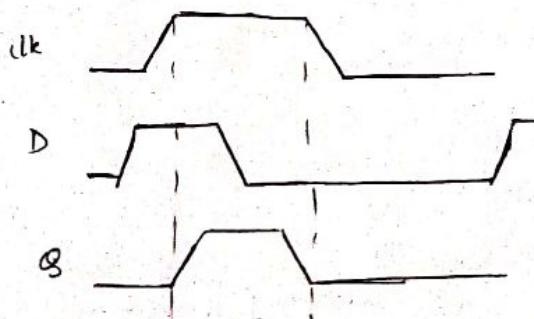
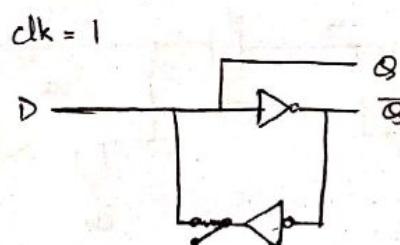
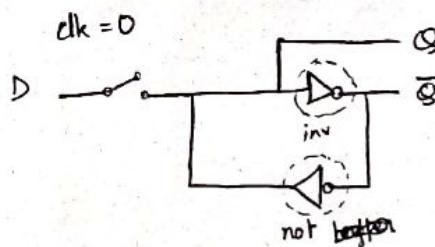
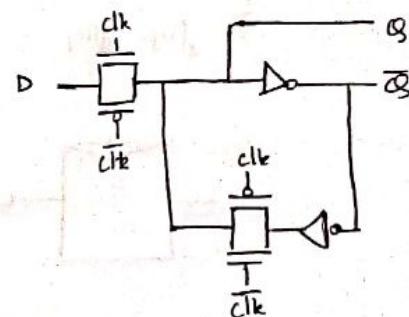
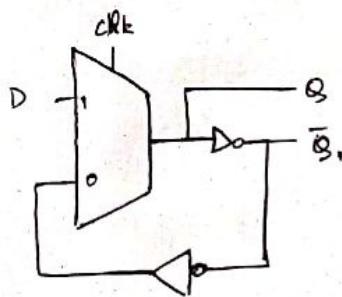
16/11/19

Latches and Flip-Flops -

Latches - level triggered.

Flip-flop - edge triggered.

CMOS + pre level sensitive D-latch -



Latches are building blocks of sequential circuits and it can be built from logic gates.

Latches continuously check its input and changes its output correspondingly.

Latches are based on the enable function input.

Latches are level triggered.

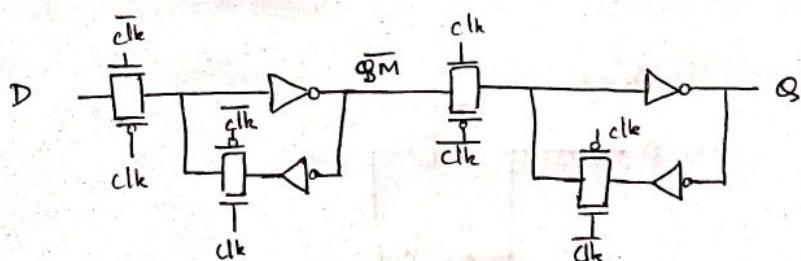
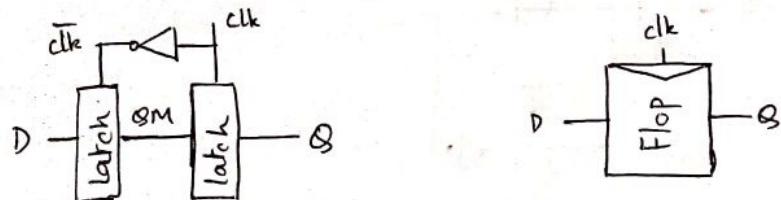
Flip-flops are the building blocks of sequential circuits but it can be built from latches.

Flip flop works based on the clock pulse.

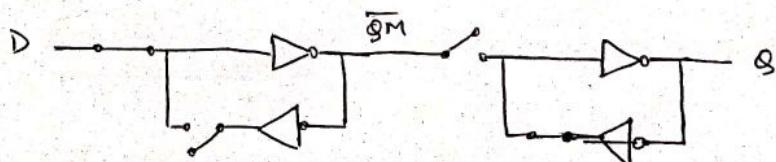
Flip flops are edge triggered

Flip flop -

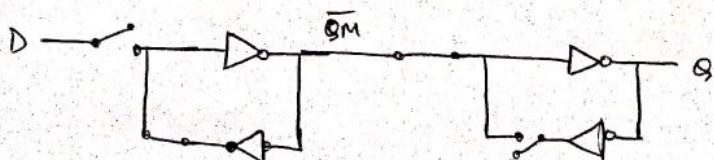
CMOS positive edge triggered D flip flop -



when $\text{clk} = 0$

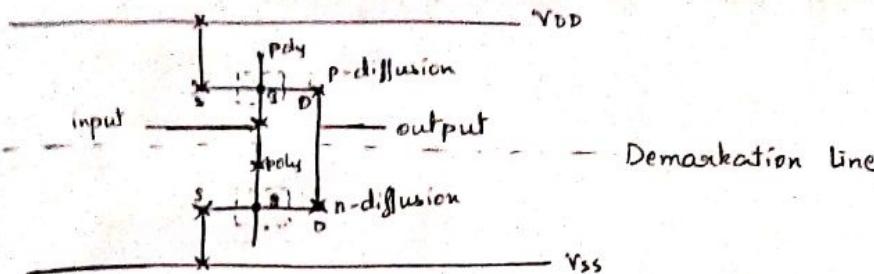
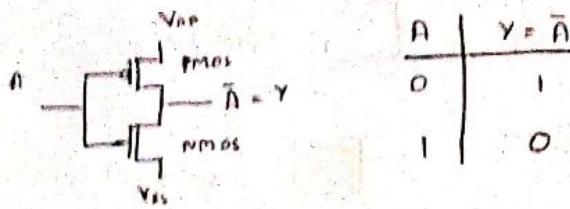


when $\text{clk} = 1$



Stick Diagram -

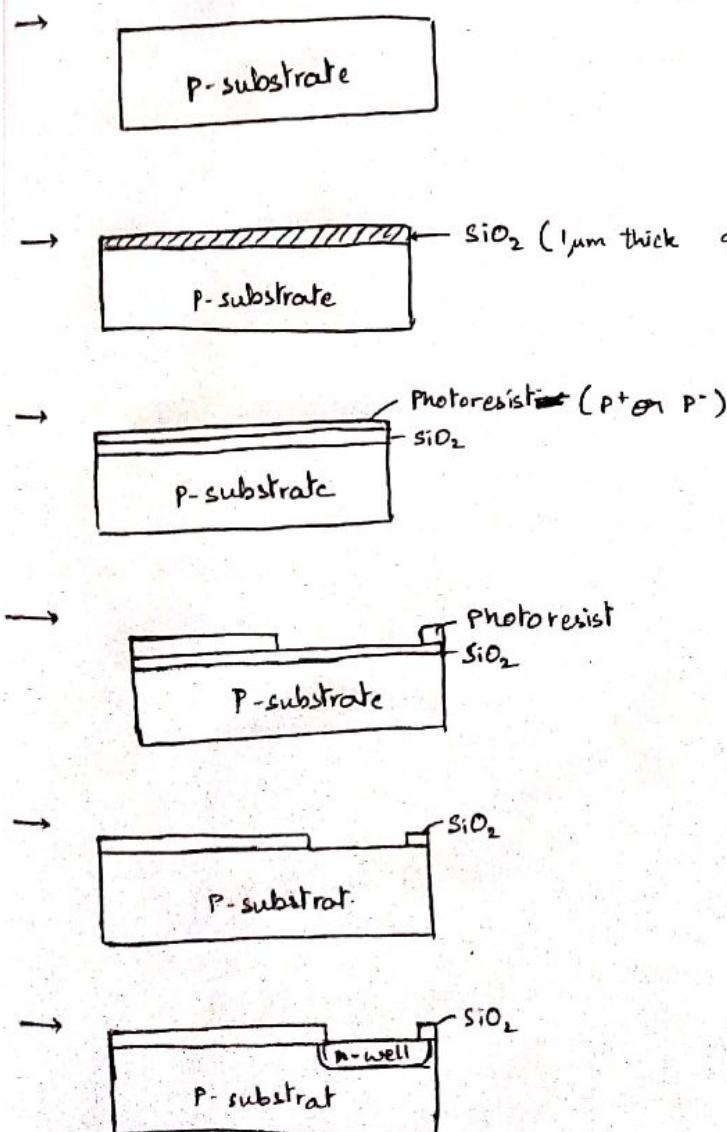
for example inverter -

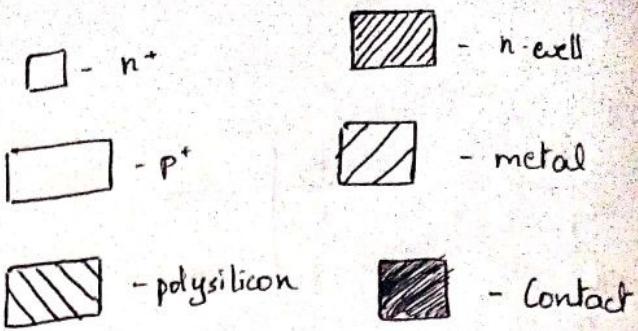
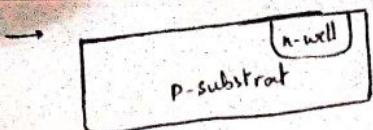


17.11.19

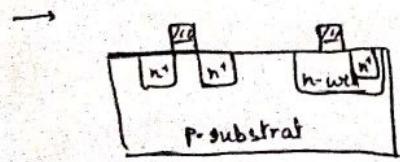
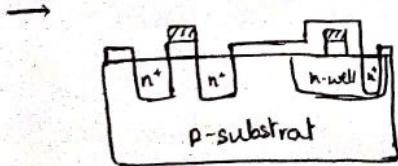
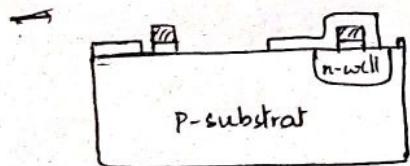
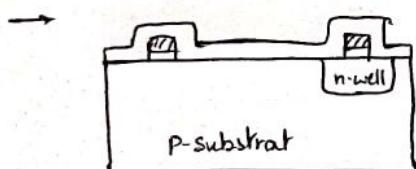
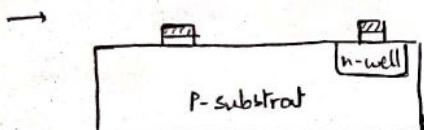
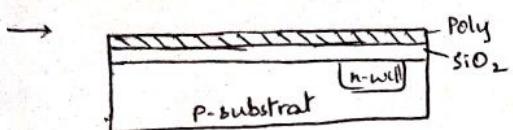
Fabrication Process -

Cross section while manufacturing the n-well.

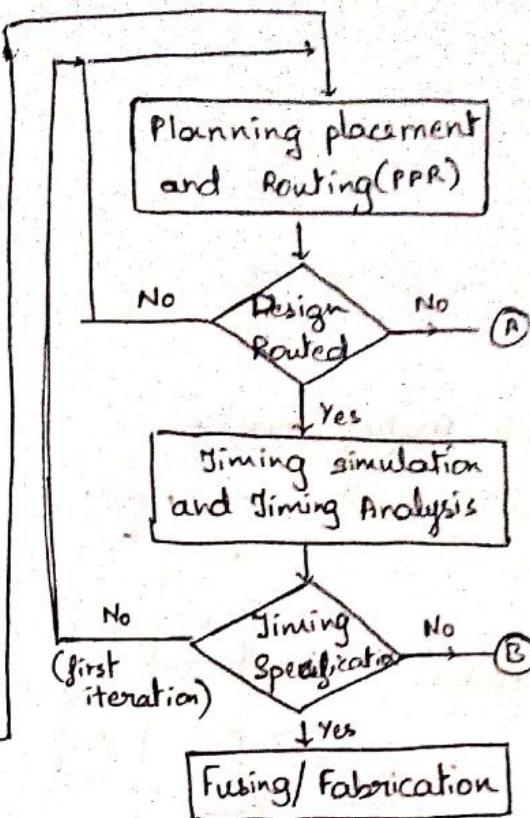
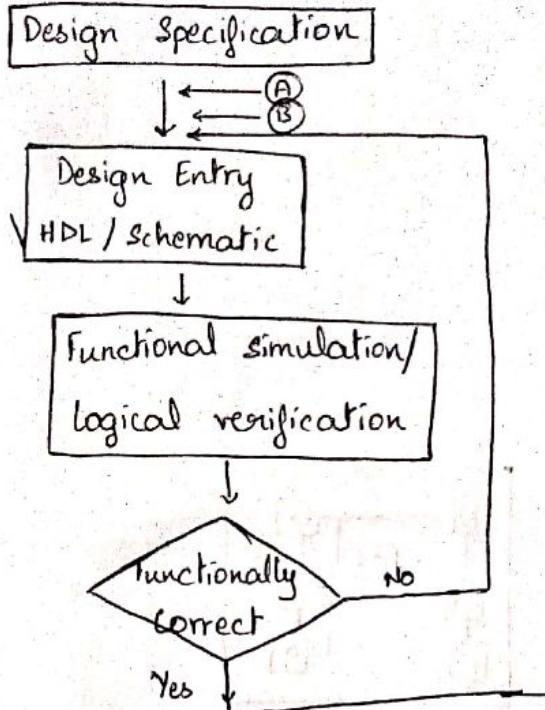




Cross section while manufacturing polysilicon and n-diffusion.



VLSI Design Flow -



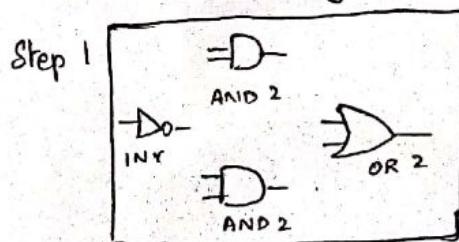
Design specification -

- Algorithm to be implemented in detail with mathematical representation.
- No. of i/p and o/p in the design and no. of bits in each of them.
- No. of bits used for internal arithematical operation.
- No. of clock signals to be used in the design.
- Max. clock frequency to be used.
- Area of the chip - small
- Power dissipation in the chip.

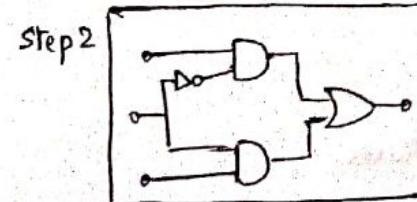
Design Entry -

No. of sub blocks to be used.

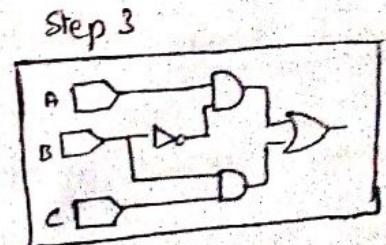
→ Schematic entry -



Components are invoked.



Interconnection is done b/w components



Naming of i/p and o/p.

→ HDL entry

VHDL

Verilog HDL

Functional Simulation -

Two types of errors

→ logical error

→ Human error.

Planning placement and Routing (PPR) -

→ Wire length minimization

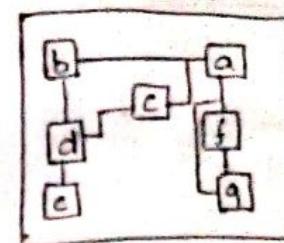
→ Delay minimization

→ Power minimization

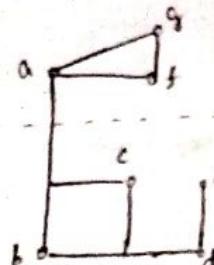
→ Via minimization (Route)



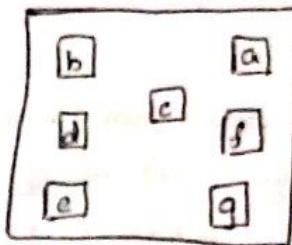
Example of
floor planning



Example of
routing



Example of circuit
partitioning



Example of
placement

Fusing/Fabrication into the chip -

→ Full custom → ASIC

→ Semicustom

cell based design

array based design - FPGA

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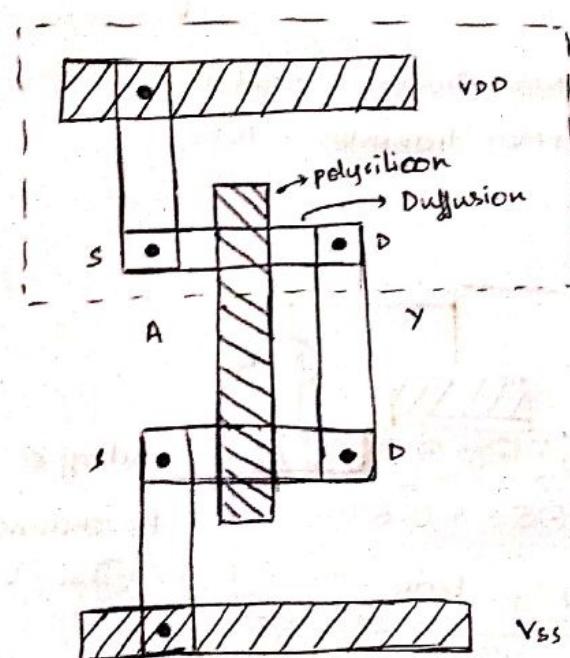
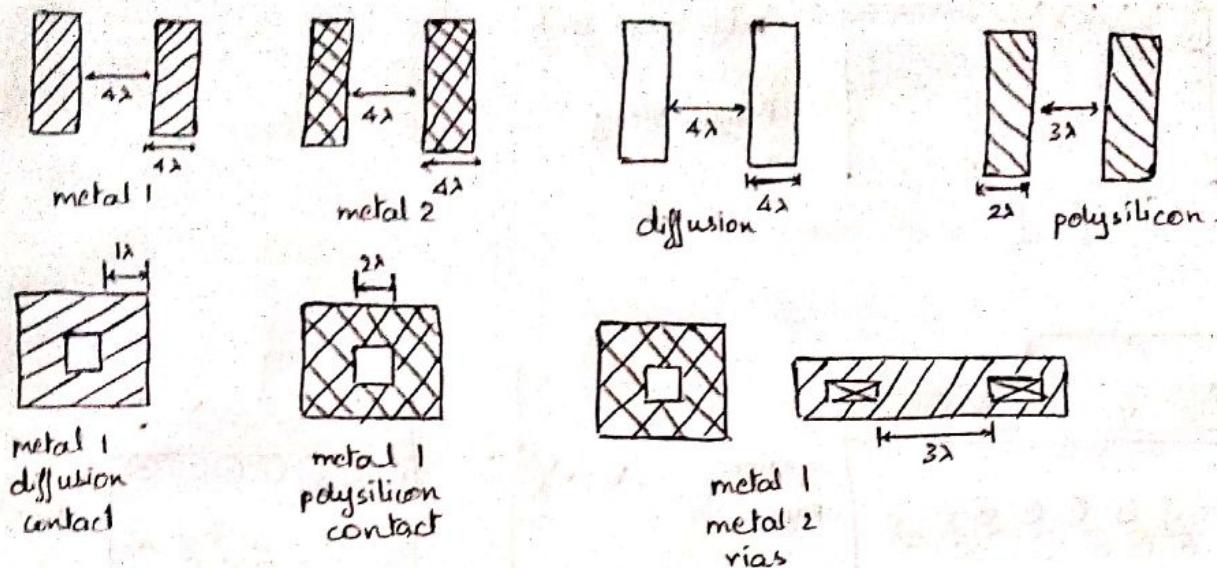
Layout Design Rules -

Lambda based design Rules

Design rules for layouts with 2 metal layers in an n-well process.
Metal and diffusion having minimum width and spacing of 1λ .

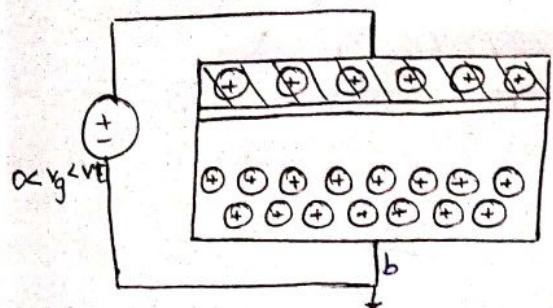
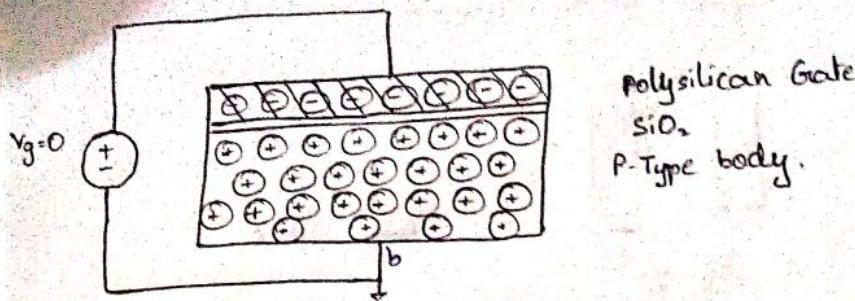
Contacts are $2\lambda \times 2\lambda$ and must be surrounded by 1λ - above and below

- Polysilicon - 2λ width.
- Branched formation - poly overlay - diffusion - 2λ , spacing - 1λ .
- Poly and contacts spacing - 3λ - from other poly @ contact.



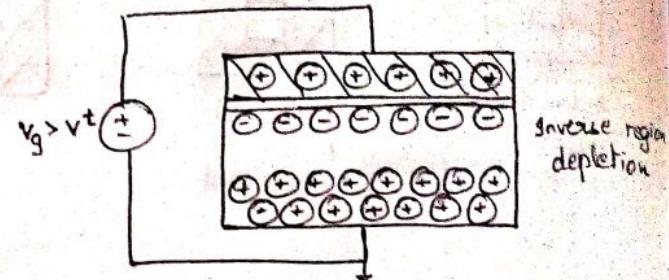
MOS TRANSISTOR THEORY

24/11/14

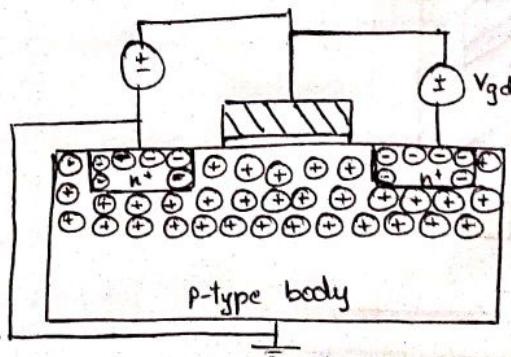


NMOS transistor - Electrons.

PMOS transistor - Holes.



$V_{gs} = 0$

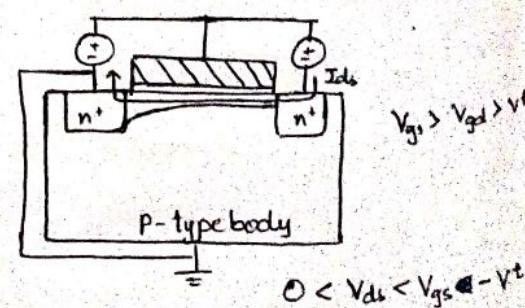
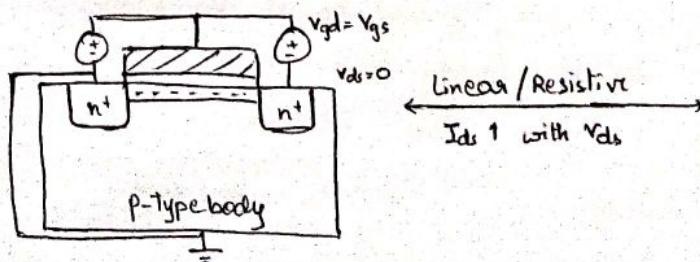


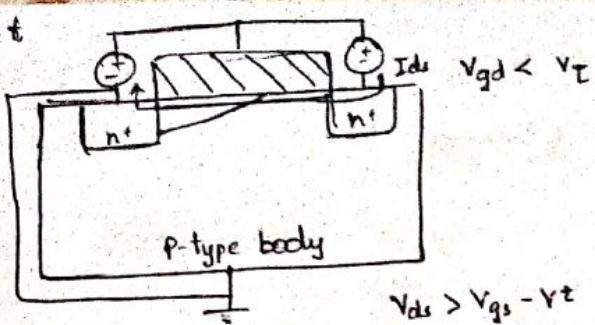
Cut off \Rightarrow

No channel.

$$I_{ds} = 0.$$

$V_{gs} > V_t$





Saturation channel pinched off.

NMOS transistor demonstration cut off, linear, saturation, region of operation.

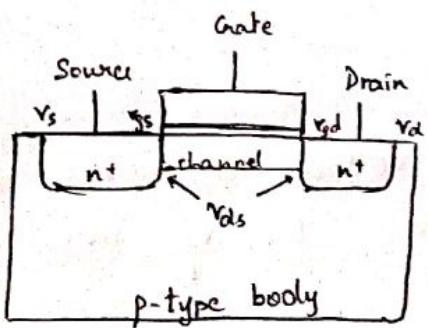
$V_{gs} = 0$ Cut off

$V_{gs} > V_t$ Linear
 $V_{ds} < V_{gs} - V_t$

$V_{gs} > V_t$ Saturation
 $V_{ds} > V_{gs} - V_t$

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Ideal I-V Characteristics -

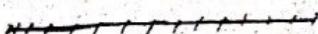


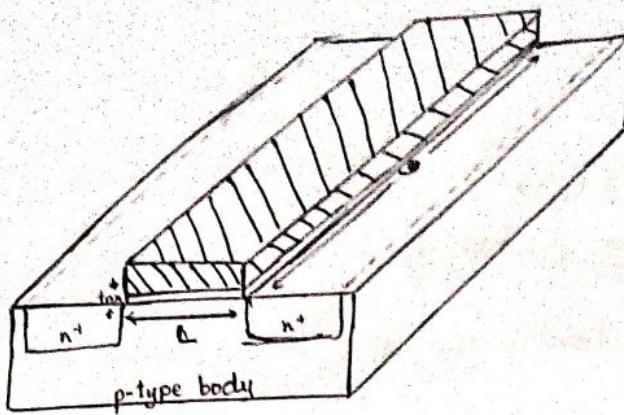
The charge on each plate of the capacitor is $q = CV$, where the charge in the channel generated

$$Q_{\text{channel}} = C_g (V_{gc} - V_t) \quad (i)$$

where C_g = capacitance of the gate to the channel. $(V_{gc} - V_t)$ = amount of

voltage attracting charge to the channel behind the minimum required to the invertor the invert from P to n. The gate voltage is referenced to the channel, which is not grounded. If the source is at V_s and drain is at V_d , average $V_c = (V_s + V_d)/2$ \Rightarrow The mean difference between the gate to the channel potential $V_{gc} = V_{gs} - V_{ds}/2$





We can model the gate as a parallel plate capacitor with capacitance \propto area over thickness. If gate has length L and width w and oxide thickness t_{ox} , the capacitance is .

$$C_g = \frac{\epsilon_{ox} WL}{t_{ox}} - (ii)$$

where ϵ_{ox} is the permittivity given by $\epsilon_{ox} = 3.9 \epsilon_0$ (for SiO_2) . and $\epsilon_0 \rightarrow$ permittivity of the free space.

$$\epsilon_0 = 8.854 \times 10^{-12} \text{ F/m.}$$

The $\frac{\epsilon_{ox}}{t_{ox}} = C_{ox}$

The constant of velocity $v = \mu E$ - (iii).

$\mu \rightarrow$ mobility. The electric field E is the voltage difference b/w drain and source , divided by channel length i.e., $E = \frac{V_{ds}}{L}$ - (iv) .

The time required for carriers to cross the channel is the channel length divided by the carrier velocity. \therefore Current b/w source and drain is the total amount of charge divided by the time required to cross.

$$I_{ds} = \frac{Q_{\text{channel}}}{L/v} = \frac{C_g (V_{gc} - V_t)}{L/v}$$

$$= \frac{\epsilon_{ox} \frac{WL}{t_{ox}} (V_{gc} - V_t)}{L/\mu E} = \frac{C_{ox} WL (V_{gc} - V_t)}{L/\mu \frac{V_{ds}}{L}}$$

$$= \frac{C_{ox} w \mu V_{ds} (V_{gc} - V_t)}{L}$$

$$= \mu C_{ox} \frac{w}{L} \left(V_{gc} - V_t - \frac{V_{ds}}{2} \right) V_{ds} - (v)$$

$$I_{ds} = \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} \quad \text{--- (vi)}$$

where $\beta = \mu C_{ox} \frac{W}{L}$

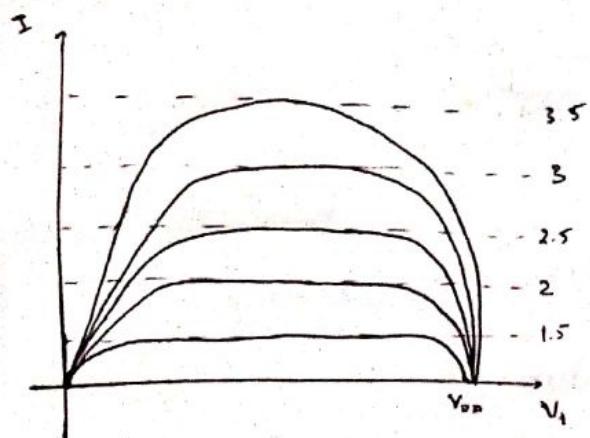
eqn (v) $V_{gs} > V_t$ but V_{ds} is relatively small, it is called linear/resistive region, because $\frac{V_{ds}}{2} \ll V_{gs} - V_t$.

If $V_{gs} > V_{dsat} = V_{gs} - V_t$, the channel is no longer inverted in the vicinity of the drain, we called it pinch off region.

$$I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2 \quad \text{--- (vii)} \quad ; \quad V_{gs} = V_{ds} = V_{DD}$$

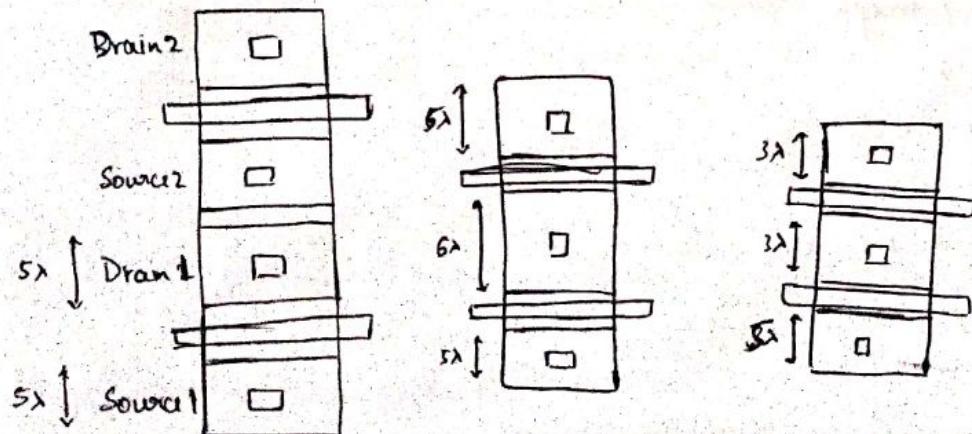
$$I_{ds} = \frac{\beta}{2} (V_{DD} - V_t)^2 \quad \text{--- (viii).}$$

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cut off} \\ \frac{\beta}{2} (V_{gs} - V_t - \frac{V_{ds}}{2}) V_{ds} & V_{gs} > V_t \quad \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{gs} > V_t \quad \text{saturation} \end{cases}$$

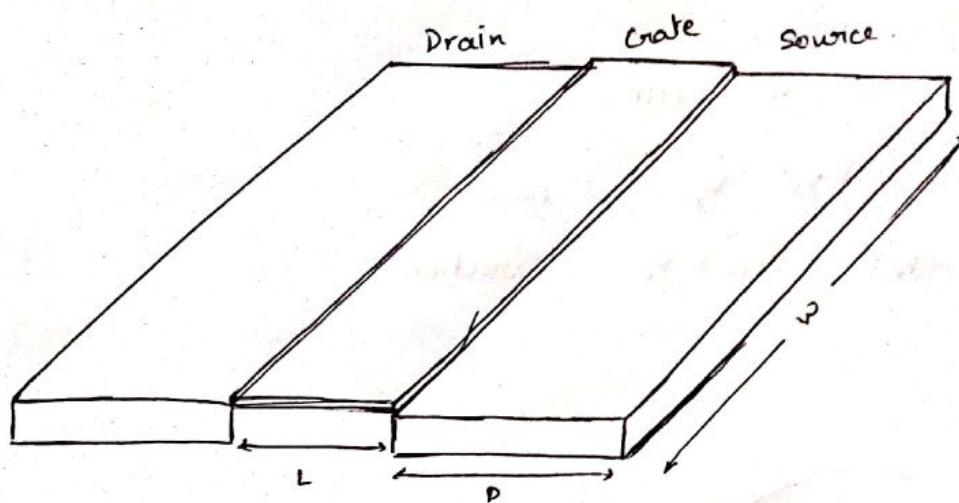


30/11/19

C-V characteristics -



Parameter	Cut off	Linear	Saturation
C_{gb}	C_0	0	0
C_{gs}	0	$C_0/2$	$2C_0/3$
C_{gd}	0	$C_0/2$	$2C_0/3$



The area is $A_S = W \cdot D$

The perimeter is $P_S = 2W + 2D$.

The total source of parasitic capacitance is

$$C_{sb} = A_S C_{jbs} + P_S C_{jbssw} \quad - (i)$$

C_{jbs} has unit of capacitance/area.

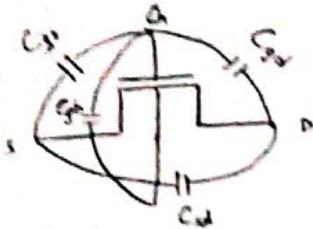
C_{jbssw} has unit of capacitance/length

$$C_{jbs} = C_J \left(1 + \frac{V_{sb}}{\Psi_0} \right)^{m_f} \quad - (ii).$$

C_J - Junction capacitance at zero bias.

$$\Psi_0 = V_T \ln \frac{N_A N_D}{\eta^2} \quad - (iii).$$

V_T → thermal voltage from thermodynamics.

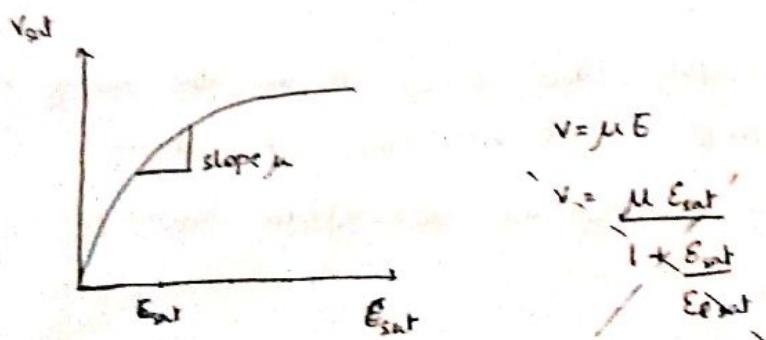
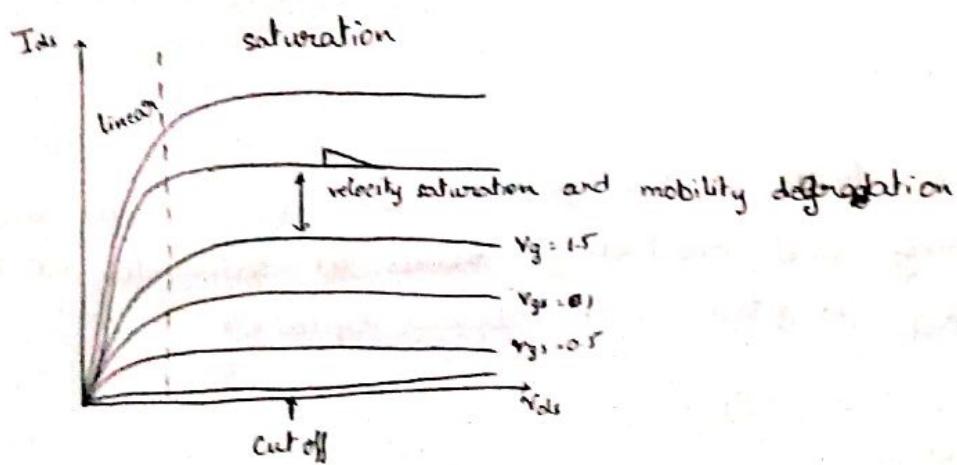


$$C_{BS} = C_S \left(1 + \frac{V_{th}}{4\phi_b} \right)^{-M_{Jaw}}$$

ability

Non ideal I V Characteristics -

- Velocity saturation and mobility degradation.
- Channel length modulation.
- Body effect.
- Sub threshold conduction.
- Junction leakage.
- Tunneling.
- Temperature dependence.
- Geometry dependence.



$$v = \mu E$$

$$v = \frac{\mu E_{sat}}{1 + \frac{E_{sat}}{E_{DSat}}}$$

$$V_{sat} = \mu E_{sat}$$

$6 - 10 \times 10^6 \text{ cm/s}$ for electron (NMO)

$4 - 8 \times 10^6 \text{ cm/s}$ for holes (PMOS)

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left(\frac{V_{GS} - V_t}{2} \right)^2$$

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left(V_{GS} - V_t - \frac{V_{DS}}{2} \right) V_{DS}$$